General Information 1

Operational Amplifiers 2

Voltage Comparators 3

Special Functions 4

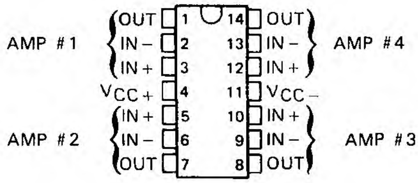
Product Previews 5

Mechanical Data 6

D2997, MARCH 1987

- Low Input Bias Current
  Typically 50 pA
- Low Input Noise Current
  Typically 0.01 pA/$\sqrt{Hz}$
- Low Total Harmonic Distortion
- Low Supply Current . . . Typically 8 mA
- Wide Gain Bandwidth . . . Typically 3 MHz
- High Slew Rate . . . Typically 13 V/μs
- Pin Compatible with the LM348

D, J, OR N PACKAGE
(TOP VIEW)



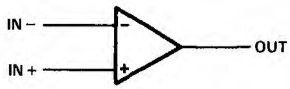
description

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347J	LF347N
	5 mV	LF347BD	LF347BJ	LF347BN

D packages are available taped and reeled. Add "R" suffix to the device type. (e.g. LF347DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . 18 V
Supply voltage, V_{CC-} . . . . −18 V
Differential input voltage, V_{ID} . . . . ±30 V
Input voltage (see Note 1) . . . . ±15 V
Duration of output short circuit . . . . Unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, J package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	[illegible] mW	7.6 mW/°C	61°C	[illegible] mW
J	680 mW	8.2 mW/°C	67°C	656 mW
N	680 mW	N/A	N/A	680 mW

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		LF347 MIN	LF347 TYP	LF347 MAX	LF347B MIN	LF347B TYP	LF347B MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	$T_A = 25°C$		5	[illegible]		3	[illegible]	mV
			Full range			13			7	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			18			18		µV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25°C$		25	100		25	100	pA
			$T_J = 70°C$			4			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25°C$		50	200		50	200	pA
			$T_J = 70°C$			8			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	[illegible]		±12	[illegible]		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25°C$	25	[illegible]		50	[illegible]		V/mV
			Full range	15			25			
r_i	Input resistance	$T_J = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \le 10$ kΩ		70	[illegible]		80	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	[illegible]		80	100		dB
I_{CC}	Supply current				8	11		8	11	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/µs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

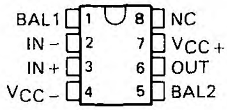
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

WIDE-BANDWIDTH JFET-INPUT OPERATIONAL AMPLIFIER

D2997, MARCH 1987

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Voltage**
  Typically 18 nV/√Hz
- **Low Input Noise Current**
  Typically 0.01 pA/√Hz
- **Low Supply Current . . . Typically 1.8 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Internally Trimmed Offset Voltage**
  Typically 10 mV
- **High Slew Rate . . . Typically 13 V/μs**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **Pin Compatible with Standard 741**

P, D, OR JG PACKAGE
(TOP VIEW)



NC—No internal connection

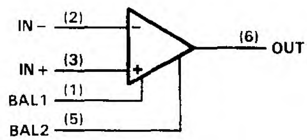
description

This device is a low-cost, high-speed, JFET-input operational amplifier with an internally trimmed input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents. It uses the same offset voltage adjustment circuits as the 741.

The LF351 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF351 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF351	D,JG,P	−0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (ie., LF351DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- Supply voltage, V_{CC+} .... 18 V
- Supply voltage, V_{CC-} .... −18 V
- Differential input voltage, V_{ID} .... ±30 V
- Input voltage (see Note 1) .... ±15 V
- Duration of output short circuit .... Unlimited
- Continuous total power dissipation .... 500 mW
- Operating temperature range .... 0°C to 70°C
- Storage temperature range .... −65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package .... 300°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package .... 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	T_A = 25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10		μV/°C
I_{IO}	Input offset current†	V_{IC} = 0	T_J = 25°C		25	100	pA
			T_J = 70°C			4	nA
I_{IB}	Input bias current†	V_{IC} = 0	T_J = 25°C		50	200	pA
			T_J = 70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	[illegible]		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
[illegible]	Common-mode rejection ratio	$R_S \leq$ 10 kΩ		70	[illegible]		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				1.8	3.4	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

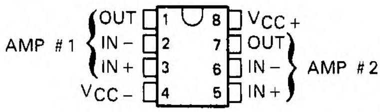
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2997, MARCH 1987–REVISED MAY 1988

- Low Input Bias Current
  Typically 50 pA
- Low Input Noise Current
  Typically 0.01 pA/√Hz
- Low Input Noise Voltage
  Typically 18 nV/√Hz
- Low Supply Current . . . Typically 3.6 mA
- High Input Impedance
  Typically 10^{12} Ω
- Internally Trimmed Offset Voltage
- Wide Gain Bandwidth . . . Typically 3 MHz
- High Slew Rate . . . Typically 13 V/μs

D, JG, OR P PACKAGE
(TOP VIEW)



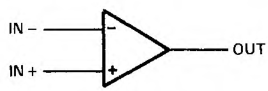
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF353 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF353	D,JG,P	0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. LP353DR)

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10\ k\Omega$	$T_A = 25°C$		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10\ k\Omega$			10		μV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25°C$		25	100	pA
			$T_J = 70°C$			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25°C$		50	200	pA
			$T_J = 70°C$			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	$T_A = 25°C$	25	100		V/mV
			Full range	15			
r_i	Input resistance	$T_J = 25°C$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100\ \Omega$		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

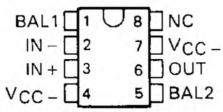
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2997, MARCH 1987—REVISED MAY 1988

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Supply Current . . . Typically 2.0 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner . . . Typically 50 Hz**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

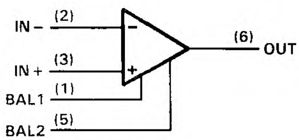
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411C can be used in applications such as high-speed integrators, digital-to-analog converters, *sample-and-hold* circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CJG	LF411CP

D package is available taped and reeled. Add "R" suffix to device type. (e.g. LF411CDR)

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ, T_A = 25°C			0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	V_{IC} = 0	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	[illegible]		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ		70	[illegible]		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70			dB
I_{CC}	Supply current				2	3.4	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

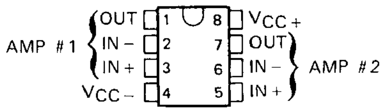
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

·7, MARCH 1987—REVISED MAY 1988

- Low Input Bias Current
  Typically 50 pA
- Low Input Noise Current
  Typically 0.01 pA/$\sqrt{Hz}$
- Low Supply Current . . . Typically 4.5 mA
- High Input Impedance
  Typically $10^{12}\ \Omega$
- Internally Trimmed Offset Voltage
- Wide Gain Bandwidth . . . Typically 3 MHz
- High Slew Rate . . . Typically 13 V/μs

D, JG, OR P PACKAGE
(TOP VIEW)



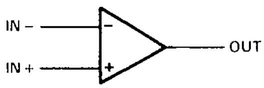
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF412C	D,JG,P	0°C to 70°C	3 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. LF412CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} .... 18 V
Supply voltage, V_{CC-} .... −18 V
Differential input voltage, V_{ID} .... ±30 V
Input voltage (see Note 1) .... ±15 V
Duration of output short circuit .... Unlimited
Continuous total power dissipation .... 500 mW
Operating temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package .... 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ, T_A = 25°C			1	3	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	V_{IC} = 0, See Note 3	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0, See Note 3	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				4.5	6.8	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

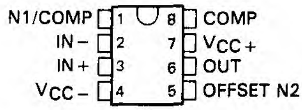
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

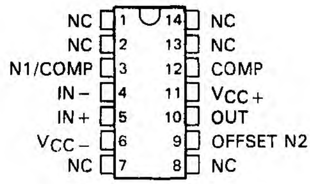
LM101A, LM201A, LM301A HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- No Latch-Up
- Wide Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as uA709
- Designed to be Interchangeable with National Semiconductor LM101A and LM301A

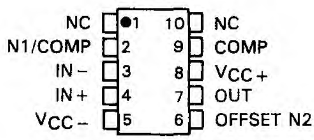
D, JG, OR P PACKAGE
(TOP VIEW)



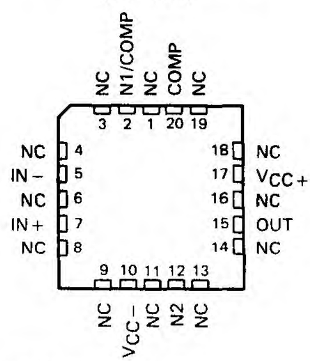
LM101A
W FLAT PACKAGE
(TOP VIEW)



LM101A
U FLAT PACKAGE
(TOP VIEW)



LM101A
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



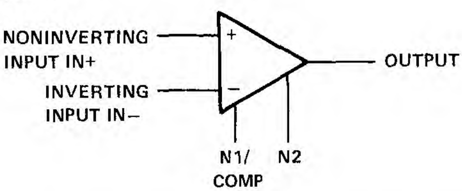
NC—No internal connection

description

The LM101A, LM201A, and LM301A are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices. The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are protected to withstand short circuits at the output. The external compensation of these amplifiers allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 7, to null out the offset voltage.

The LM101A is characterized for operation over the full military temperature range of −55°C to 125°C, the LM201A is characterized for operation from −25°C to 85°C, and the LM301A is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM301AD	–	LM301AJG	LM301AP	–	–
−25°C to 85°C	2 mV	LM201AD	–	LM201AJG	LM201AP	–	–
−55°C to 125°C	2 mV	–	LM101AFK	LM101AJG	–	LM101AU	LM101AW

The D package is available taped and reeled. Add the suffix R to the device type. (i.e., LM301ADR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM101A	LM201A	LM301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM201A only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG (LM101A)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (LM201A, LM301A)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

electrical characteristics at specified free-air temperature, C_C = 30 pF (see Note 5)

PARAMETER		TEST CONDITIONS†		LM101A, LM201A			LM301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0 V	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage	V_O = 0 V	Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, V_O = 0, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM101A is −55°C to 125°C, for LM201A is −25°C to 85°C, and for LM301A is 0°C to 70°C.

NOTES: 5. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for LM101A and LM201A, and $V_{CC\pm}$ = ±5 V to ±15 V for LM301A. All typical values are at $V_{CC\pm}$ = ±15 V.

6. For LM101A and LM201A, $V_{CC\pm}$ = ±20 V. For LM301A, $V_{CC\pm}$ = ±15 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

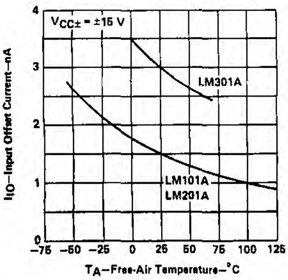


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

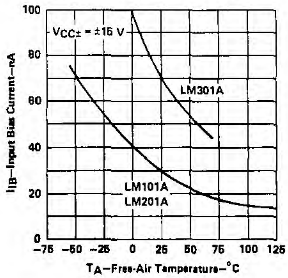


FIGURE 2

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

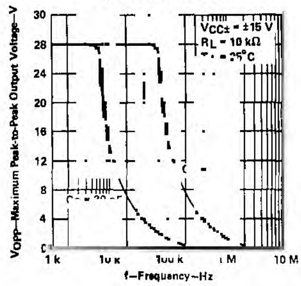


FIGURE 3

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

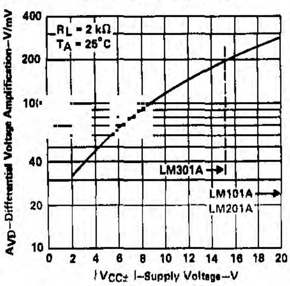


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

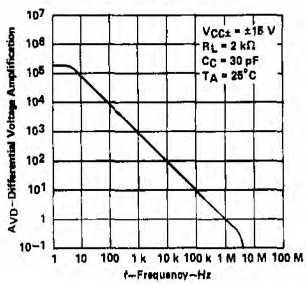


FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

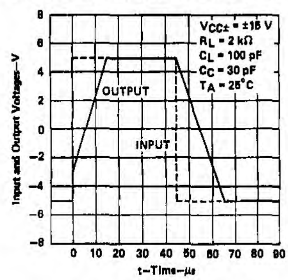
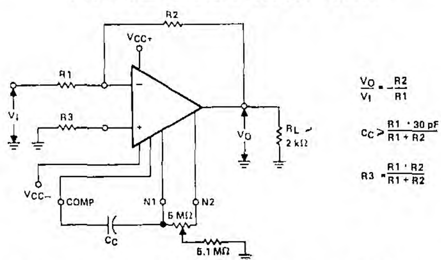


FIGURE 6

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C > \frac{R1 \cdot 30\ pF}{R1 + R2}$$

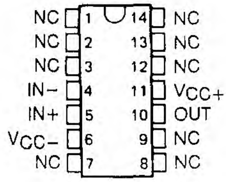
$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 7. INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

D962, DECEMBER 1970—REVISED JUNE 1988

- Low Input Currents
- No Frequency Compensation Required
- Low Input Offset Parameters
- Short-Circuit Protection
- No Latch-Up
- Wide Common-Mode and Differential Voltage Ranges

LM107 . . . J OR W PACKAGE
(TOP VIEW)



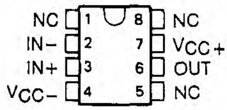
description

The LM107, LM207, and LM307 are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

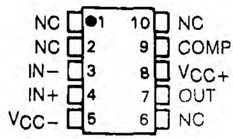
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The LM107 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM207 is characterized for operation from −25°C to 85°C, and the LM307 is characterized for operation from 0°C to 70°C.

LM107 . . . JG PACKAGE
LM207, LM307 . . . D, JG, OR P PACKAGE
(TOP VIEW)

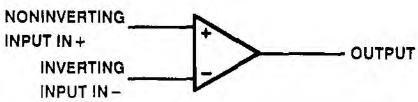


LM107 . . . U FLAT PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM307D	—	LM307JG	LM307P	—	—
−25°C to 85°C	2 mV	LM207D	—	LM207JG	LM207P	—	—
−55°C to 125°C	2 mV	—	LM107J	LM107JG	—	LM107U	LM107W

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM307DR)

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

	LM107	LM207	LM307	UNIT
Supply voltage V_{CC+} (see Note 1)	22	22	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM207 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
J (LM107)	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG (LM107)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (LM207, LM307)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	–
P	500 mW	N/A	N/A	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM107, LM207			LM307			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_O = 0$	Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	$T_A = -55°C$ to 25°C			0.02	0.2				nA/°C
		$T_A = 25°C$ to MAX			0.01	0.1				
		$T_A = 0°C$ to 25°C						0.02	0.6	
		$T_A = 25°C$ to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm15$ V, $R_L = 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm15$ V, $R_L = 2$ kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, $V_O = 0$, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

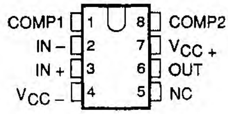
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM107 is −55°C to 125°C, for LM207 is −25°C to 85°C, and for LM307 is 0°C to 70°C.

NOTES: 5. Unless otherwise noted $V_{CC\pm} = \pm5$ V to ±20 V for LM107 and LM207, and $V_{CC\pm} = \pm5$ V to ±15 V for LM307. All typical values are at $V_{CC\pm} = \pm15$ V.

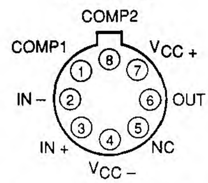
6. For LM107 and LM207, $V_{CC\pm} = \pm20$ V. For LM307, $V_{CC\pm} = \pm15$ V.

- **Input Offset Current . . . 200 pA Max at 25°C for LM108, LM108A**
- **Input Bias Current . . . 2 nA Max at 25°C for LM108, LM108A**
- **Supply Current . . . 600 μA Max at 25°C for LM108, LM108A**
- **Input Offset Voltage . . . 500 μV Max at 25°C for LM108A, LM308A**
- **Offset Voltage Temperature Coefficient . . . 5 μV/°C Max for LM108A, LM308A**
- **Supply Voltage Range . . . ± 2 V to ± 18 V**
- **Applications:**
  - **Integrators**
  - **Transducer Amplifiers**
  - **Analog Memories**
  - **Light Meters**
- **Designed To Be Interchangeable with National LM108 Series and Linear Technology LM108 Series**

P PACKAGE
(TOP VIEW)

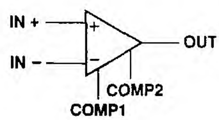


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L package) is in electrical contact with the case.

symbol



description

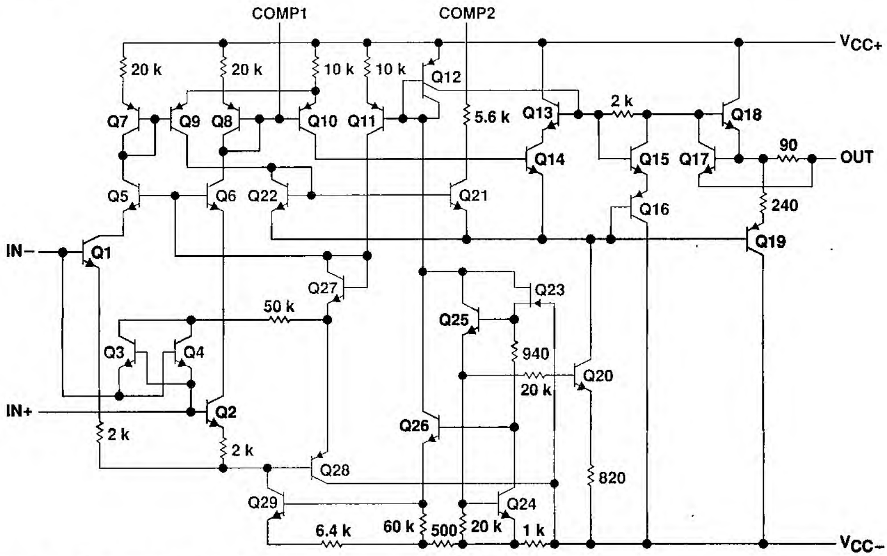
The LM108 series of precision operational amplifiers is particularly well-suited for high-source-impedance applications requiring low input offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the input offset and bias currents of the LM108 series do not vary significantly with temperature. Advanced design, processing, and testing techniques make this series a superior choice over previous devices. For applications requiring higher performance, see the LT1008 and LT1012.

The LM108 and LM108A are characterized for operation over the full military temperature range of –55°C to 125°C. The LM308 and LM308A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE	
		METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.5 mV	LM308AL	[illegible]
	7.5 mV	LM[illegible]	[illegible]
–[illegible] to 125°C	0.5 mV	LM[illegible]	[illegible]AP
	2 mV	LM[illegible]	LM108P

schematic



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1):	LM108, LM108A	20 V
	LM308, LM308A	18 V
Supply voltage, V_{CC-} (see Note 1):	LM108, LM108A	−20 V
	LM308, LM308A	−18 V
Input voltage range, V_I (see Note 2)		±15 V
Differential input current (see Notes 3 and 4)		±10 mA
Duration of output short-circuit at (or below) 25°C (see Note 5)		unlimited
Operating free-air temperature, T_A:	LM108, LM108A	−55°C to 125°C
	LM308, LM308A	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package		260°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or either power supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±20 V (*unless otherwise noted*)

PARAMETER		TEST CONDITIONS	T_A†	LM108A			LM108			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		0.7	2	mV
			Full range			1			3	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1	5		3	15	μV/°C
I_{IO}	Input offset current		25°C		0.05	0.2		0.05	0.2	nA
			Full range			0.4			0.4	
α_{IIO}	Temperature coefficient of input offset current		Full range		0.5	2.5		0.5	2.5	pA/°C
I_{IB}	Input bias current		25°C		0.5	2		0.5	2	nA
			Full range			3			3	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±13.5			±13.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		50	300		V/mV
			Full range	40			25			
r_i	Input resistance		25°C	30	70		30	70		MΩ
CMRR	Common-mode rejection ratio		Full range	96			85			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.6		0.3	0.6	mA
			125°C		0.15	0.4		0.15	0.4	

†Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM308A MIN	LM308A TYP	LM308A MAX	LM308 MIN	LM308 TYP	LM308 MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		2	7.5	mV
			Full range			[illegible]			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2	5		6	30	µV/°C
I_{IO}	Input offset current		25°C		0.2	1		0.2	1	nA
			Full range			1.5			1.5	
α_{IIO}	Temperature coefficient of input offset current		Full range		2	10		2	10	pA/°C
I_{IB}	Input bias current		25°C		1.5	7		1.5	7	nA
			Full range			10			10	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±14			±14			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		25	[illegible]		V/mV
			Full range	60			15			
r_i	Input resistance		25°C	10	40		10	40		MΩ
CMRR	Common-mode rejection ratio		Full range	96			80			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.8		0.3	0.8	mA

†Full range is 0°C to 70°C.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

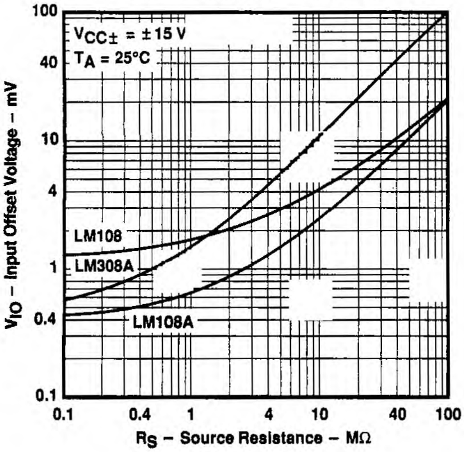


FIGURE 1

TEMPERATURE COEFFICIENT
OF EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

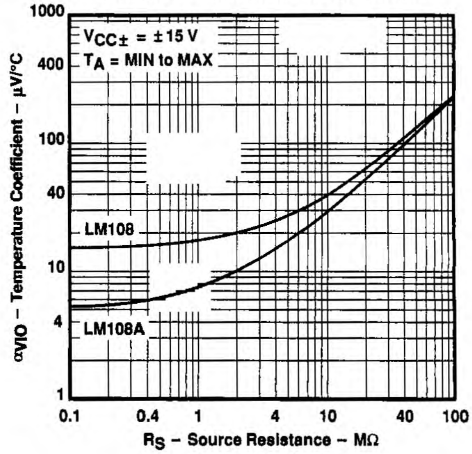


FIGURE 2

LM108, LM108A
INPUT BIAS and OFFSET CURRENTS
vs
FREE-AIR TEMPERATURE

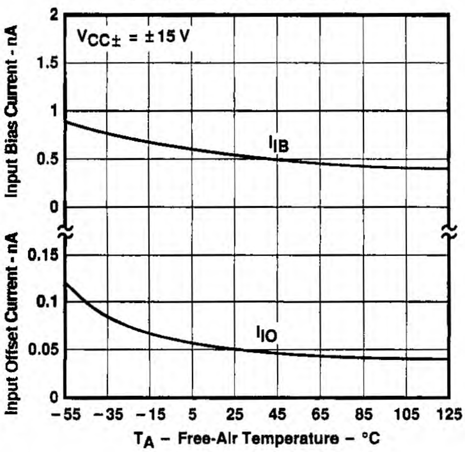


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

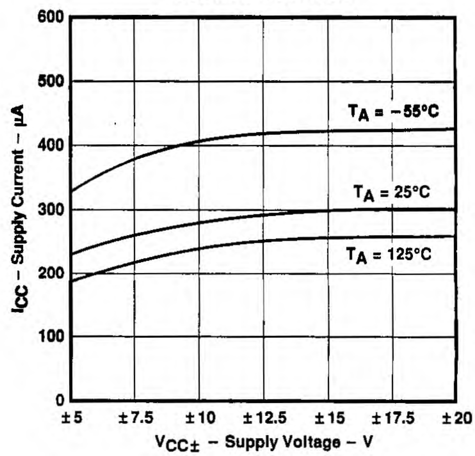


FIGURE 4

†Data above 70°C, below 0°C, or from $V_{CC\pm}$ = ±18 V to ±20 V are applicable to LM108 and LM108A devices only.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

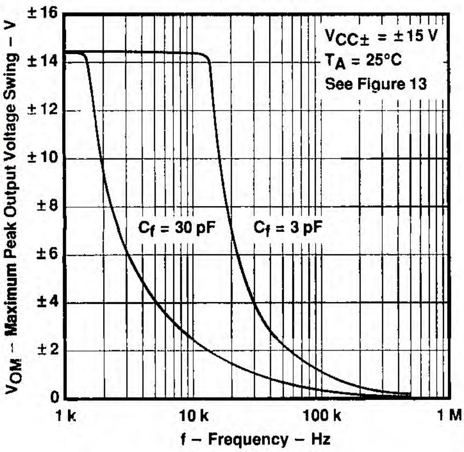


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

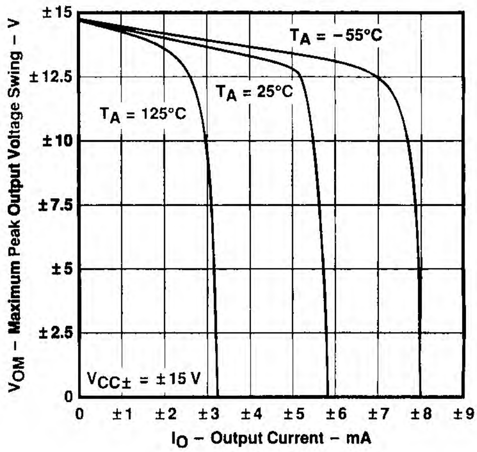


FIGURE 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

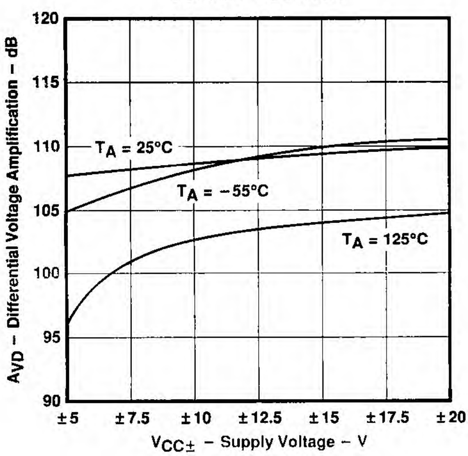


FIGURE 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE DELAY
vs
FREQUENCY

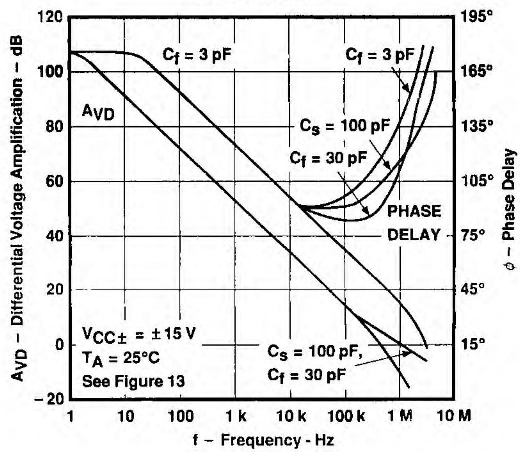


FIGURE 8

†Data above 70°C, below 0°C, or from $V_{CC\pm}$ = ±18 V to ±20 V are applicable to LM108 and LM108A devices only.

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

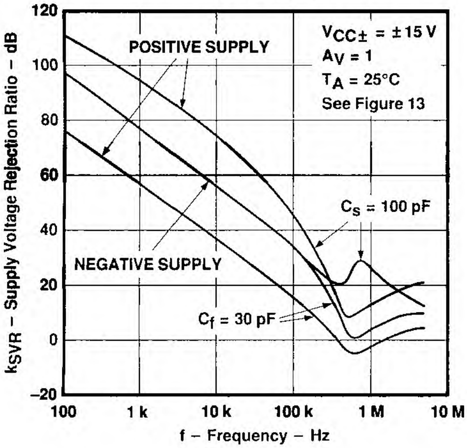


FIGURE 9

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

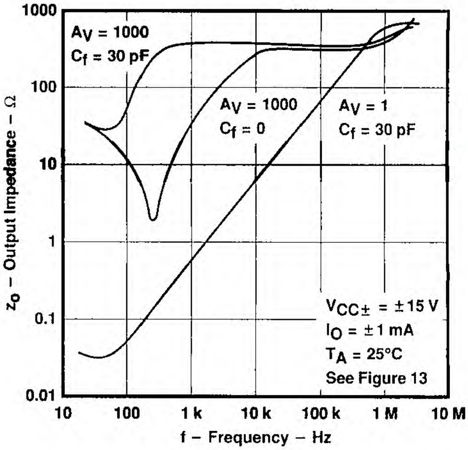


FIGURE 10

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

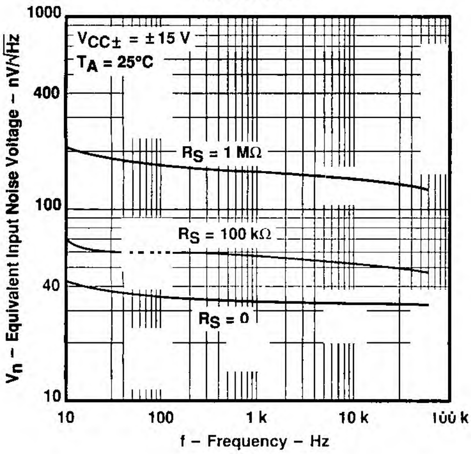


FIGURE 11

VOLTAGE FOLLOWER
PULSE RESPONSE

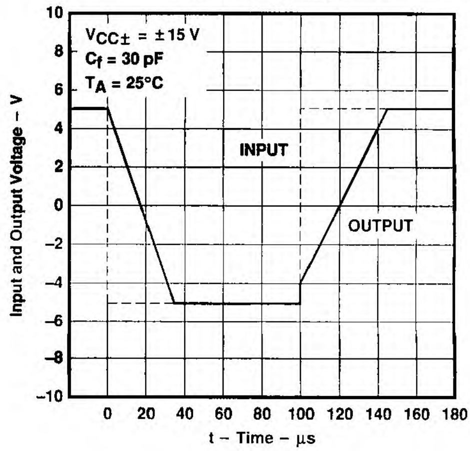
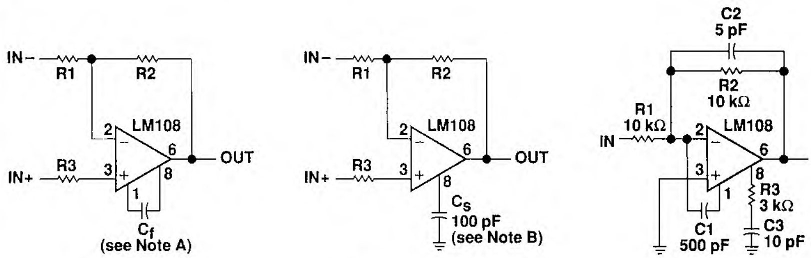


FIGURE 12

TYPICAL APPLICATION DATA

frequency compensation

Figure 13 shows the frequency compensation circuits for standard compensation, alternate compensation, and feed-forward compensation. The alternate compensation circuit improves supply voltage rejection by a factor of ten.



(a) STANDARD (b) ALTERNATE (c) FEED-FORWARD

NOTES: A. $C_f \geq R1C_O/(R1 + R2)$, C_O = 30 pF, bandwidth and slew rate are proportional to $1/C_f$.
B. Bandwidth and slew rate are proportional to $1/C_S$.

FIGURE 13. FREQUENCY COMPENSATION CIRCUITS

input guarding

Input guarding is used to reduce surface leakage (see Figure 14). Both sides of the board must be guarded. Bulk leakage reduction is less than surface leakage reduction and depends on the guard-ring width. The guard ring is connected to a low-impedance point at the same potential as the sensitive input leads. Connections for various op-amp configurations are shown in Figure 15.

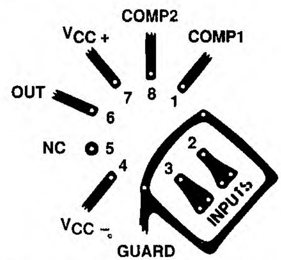
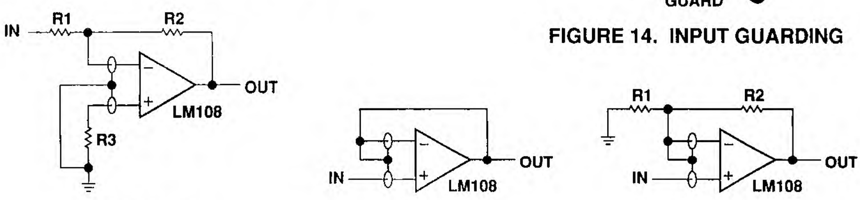


FIGURE 14. INPUT GUARDING



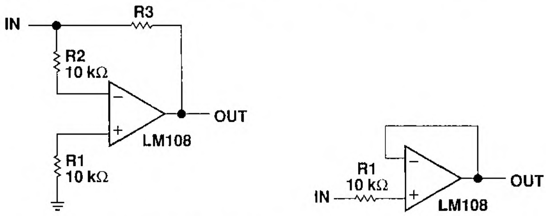
(a) INVERTING (b) FOLLOWER (c) NONINVERTING

FIGURE 15. GUARD RING CONNECTIONS FOR VARIOUS OP AMP CONFIGURATIONS

TYPICAL APPLICATION DATA

input protection

Current is limited by R2 even when the input is connected to a voltage source outside the common-mode range [see Figure 16(a)]. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation. The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted [see Figure 16(b)].

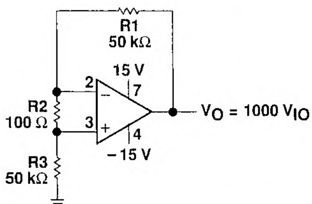


(a) CURRENT LIMITED BY R1 OR R2 (b) CURRENT LIMITED BY R1

FIGURE 16. INPUT PROTECTION

input offset voltage testing

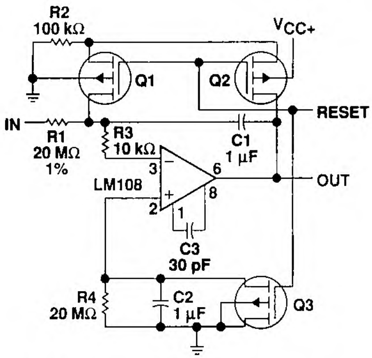
The test circuit for input offset voltage is shown in Figure 17. This circuit is also used as the burn-in configuration with supply voltages equal to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, AV = 100.



NOTE A: Resistors must have low thermoelectric potential.

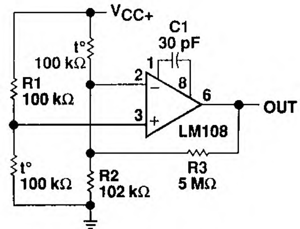
FIGURE 17. TEST CIRCUIT FOR INPUT OFFSET VOLTAGE

TYPICAL APPLICATION DATA



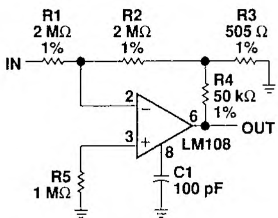
NOTE A: Q1 and Q3 should not have internal gate-protection diodes.

FIGURE 18. LOW-DRIFT INTEGRATOR WITH RESET



NOTE A: R1 = R2R3/(R2 + R3).

FIGURE 19. AMPLIFIER FOR BRIDGE TRANSDUCERS



NOTE A: R2 > R1, R2 >> R3,
A_V = R2(R3 + R4)/R1R3.

FIGURE 20. INVERTING AMPLIFIER WITH HIGH INPUT RESISTANCE

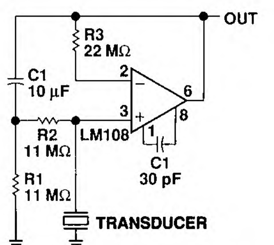
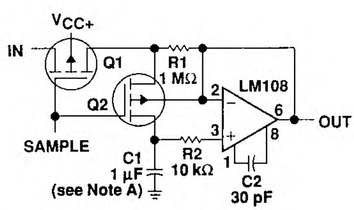
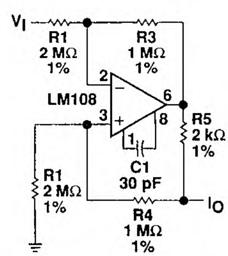


FIGURE 21. AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



NOTES: A. Teflon, polyethylene, or polycarbonate dielectric capacitor.
B. Worst case drift is less than 2.5 mV/s.

FIGURE 22. SAMPLE-AND-HOLD AMPLIFIER



NOTE A: I_O = (R3)V_I/R1R5
R3 = R4 + R5
R1 = R2

FIGURE 23. BILATERAL CURRENT SOURCE

TYPICAL APPLICATION DATA

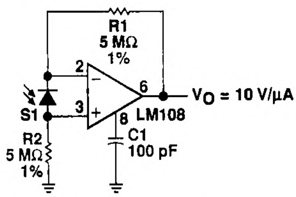
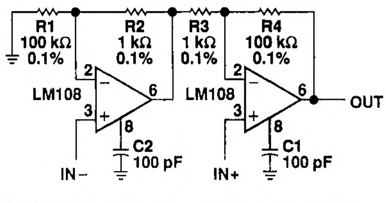
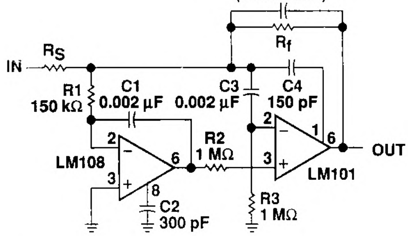


FIGURE 24. AMPLIFIER FOR PHOTODIODE SENSOR



NOTE A: R1 = R4, R2 = R3, $A_V = 1 + R1/R2$

FIGURE 25. DIFFERENTIAL-INPUT INSTRUMENTATION AMPLIFIER

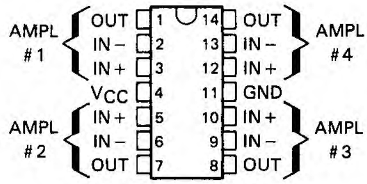


NOTES: A. $C5 = 6 \times 10^{-8}/R_f$
B. Power bandwidth = 250 kHz
C. Small-signal bandwidth = 3.5 MHz
D. Slew Rate = 10 V/µs
E. The LM101 increases speed, raises high- and low-frequency gain, increases output drive capability, and eliminates thermal feedback.

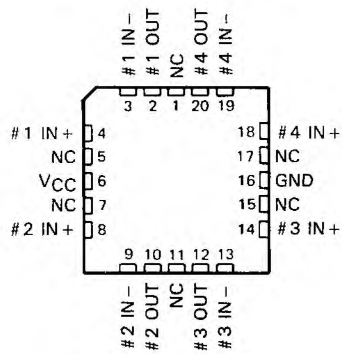
FIGURE 26. FAST SUMMING AMPLIFIER

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2902 . . . 3 V to 26 V),
  or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V (26 V for LM2902)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

LM124 . . . J OR W PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGES
(TOP VIEW)

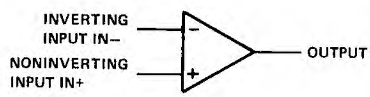


LM124
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each amplifier)



description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (for the LM2902, 3 V to 26 V), and Pin 4 is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

The LM124 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM2902 is characterized for operation from −40°C to 105°C, the LM224 and LM224A from −25°C to 85°C, and the LM324 and LM324A from 0°C to 70°C.

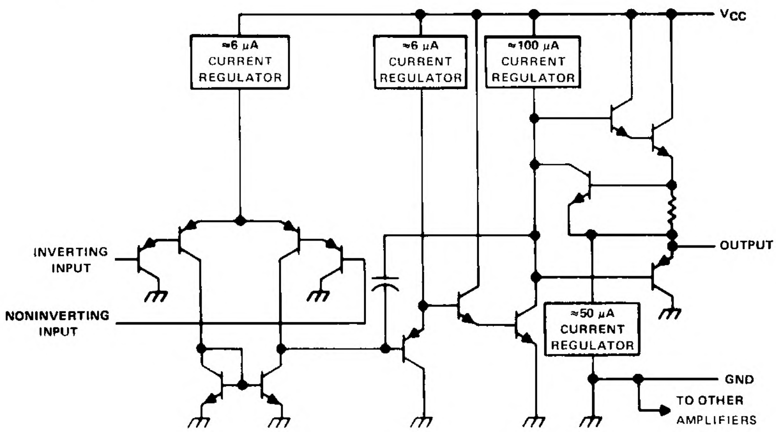
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)
0°C to 70°C	7 mV	LM324D	—	LM324J	LM324N	—
	3 mV	LM324AD		LM324AJ	LM324AN	
−25°C to 85°C	5 mV	LM224D	—	LM224J	LM224N	—
	3 mV	LM224AD		LM224AJ	LM224AN	
−40°C to 105°C	7 mV	LM2902D	—	LM2902J	LM2902N	—
−55°C to 125°C	5 mV	—	LM124FK	LM124J	—	LM124W

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM324DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM124 LM224, LM224A, LM324, LM324A	LM2902	UNIT
[illegible]ly voltage, V_{CC} (see Note 1)		32	26	V
[illegible]ential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		−0.3 to 32	−0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	LM124	−55 to 125		°C
	[illegible]A	−25 to 85		°C
	[illegible]A	0 to 70		°C
	LM2902		−40 to [illegible]	°C
Storage temperature range		−65 to 150	−65 to [illegible]	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	900 mW	7.6 mW/°C	32°C	[illegible] mW	494 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM124)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (all others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	N/A
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A
W	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124, LM224			LM324			LM2902			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500				
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		R_L = 10 kΩ	25°C							$V_{CC}-1.5$			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L = 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	R_l ≤ 10 kΩ	Full range		5	20		5	20		5	100	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120								dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1.1	3		1.1	3		1.1	3	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2902, 30 V for the others. Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, 0°C to 70°C for LM324, and −40°C to 105°C for LM2902.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

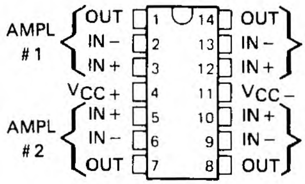
PARAMETER		TEST CONDITIONS†		LM224A			LM324A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−80		−15	−100	nA
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1$			$V_{CC}-1$			V
		V_{CC} 30 V, R_L = 2 kΩ	Full range	26			26			
		V_{CC} = 30 V, R_L = 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_l \le 10$ kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge 2$ kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5			5			
		V_{ID} = −1 V, V_O = 200 mV	Full range	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		1.5	2.4		1.5	2.4	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1.1	3		1.1	3	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25°C to 85°C for LM224A and 0°C to 70°C for LM324A.

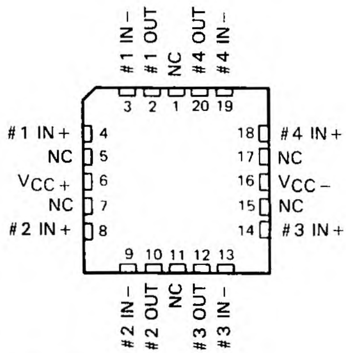
D2551, OCTOBER 1979—REVISED MAY 1988

- uA741 Operating Characteristics
- Low Supply Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to be Interchangeable with National LM148, LM248, and LM348.

LM148 . . . J PACKAGE
LM248, LM348 . . . D, J, OR N PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



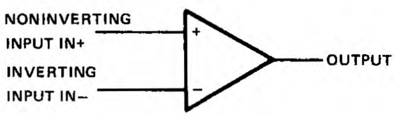
NC—No internal connection

description

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the uA741. These amplifiers exhibit low supply current drain, and input bias and offset currents that are much less than those of the uA741.

The LM148 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM248 is characterized for operation from −25°C to 85°C, and the LM348 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	6 mV	LM348D	—	LM348J	LM348N
−25°C to 85°C	6 mV	LM248D	—	LM248J	LM248N
−55°C to 125°C	5 mV	—	LM148FK	LM148J	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM348DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM148	LM248	LM348	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−[illegible]	−18	−18	V
Differential input voltage (see Note 2)		44	36	36	V
Input voltage (either input, see Notes 1 and 3)		±22	±18	±18	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to [illegible]	−65 to 150	°C
Case temperature for 60 seconds	FK package	[illegible]			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible] mW	7.6 mW/°C	32°C	608 mW	494 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM148)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM248, LM348)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	N/A
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A

electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†			LM148			LM248			LM348			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		25°C		1	5		1	6		1	6	mV
				Ful[illegible]e			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0		2[illegible]		4	25		4	50		4	50	nA
				Full range			75			125			100	
I_{IB}	Input bias current	V_O = 0		25°C		30	100		30	[illegible]		30	200	nA
				Full range			325			[illegible]			400	
V_{ICR}	Common-mode input voltage range			Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13		±12	±13		±12	±13		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			
		R_L = 2 kΩ		25°C	±10	±12		±10	±12		±10	±12		
		R_L ≥ 2 kΩ		Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ		25°C	50	160		25	160		25	160		V/mV
				Full range	25			15			15			
r_i	Input resistance			25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	A_{VD} = 1		25°C		1			1			1		MHz
ϕ_M	Phase margin	A_{VD} = 1		25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0		25°C	70	90		70	90		70	90		dB
				Full range	70			70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C	77	96		77	96		77	96		dB
				Full range	77			77			77			
I_{OS}	Short-circuit output current			25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load	V_O = 0	25°C					2.4	4.5		2.4	4.5	mA
			V_O = V_{OM}†			2.4	3.6							
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 Hz to 20 kHz,		25°C		120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for LM148, −25°C to 85°C for LM248, and 0°C to 70°C for LM348.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

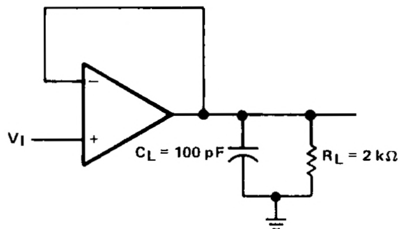
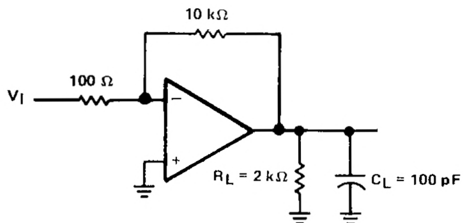


FIGURE 1. UNITY-GAIN AMPLIFIER



A_{VD} = −100

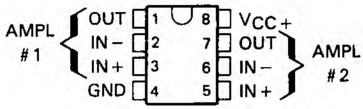
FIGURE 2. INVERTING AMPLIFIER

LM158, LM258, LM358
LM258A, LM358A, LM2904
DUAL OPERATIONAL AMPLIFIERS

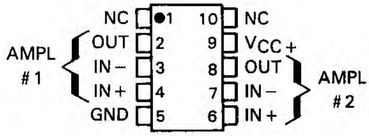
D2231, JUNE 1976—REVISED AUGUST 1988

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2904 . . . 3 V to 26 V),
  or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V (±26 V for LM2904)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

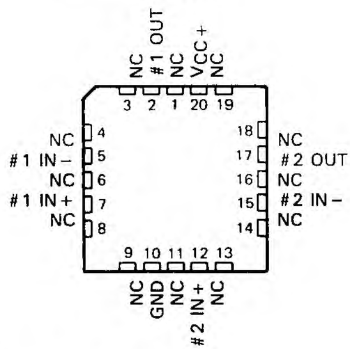
D, JG, OR P PACKAGE
(TOP VIEW)



U FLAT PACKAGE
(TOP VIEW)



LM 158
FK CHIP CARRIER PACKAGE
(TOP VIEW)



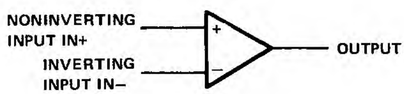
NC—No internal connection

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (3 V to 26 V for the LM2904), and the V_{CC} pin is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

schematic (each amplifier)



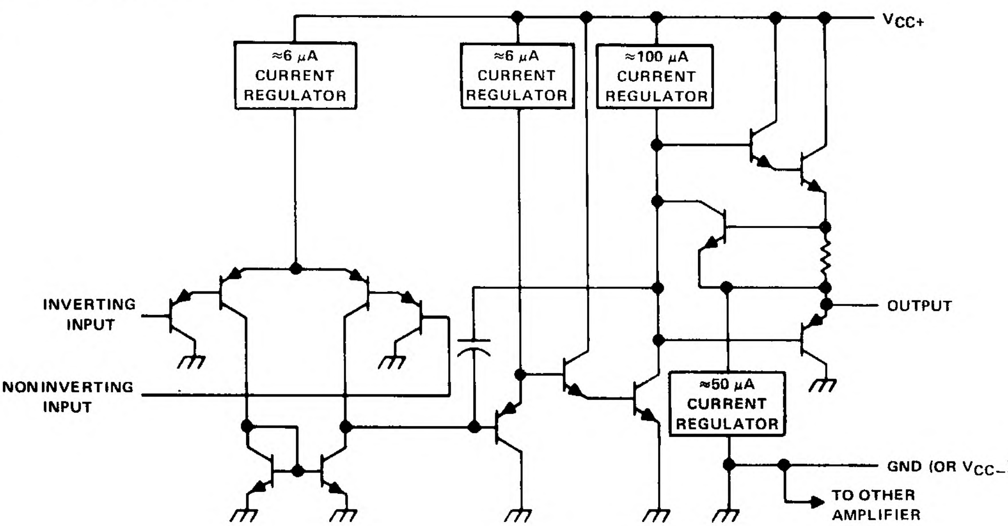
The LM158 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The LM258 and LM258A are characterized for operation from −25 °C to 85 °C, the LM358 and LM358A from 0 °C to 70 °C, and the LM2904 from −40 °C to 105 °C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)
0°C to 70°C	7 mV	LM358D	—	[illegible]	LM358P	—
	3 mV	[illegible]		[illegible]	LM358AP	
−25°C to 85°C	5 mV	[illegible]	—	[illegible]	LM258P	—
	3 mV	LM258AD		LM258AJG	LM258AP	
−40°C to 105°C	7 mV	LM2904D	—	LM2904JG	LM2904P	—
−55°C to 125°C	5 mV	—	LM158FK	LM158JG	—	LM158U

The D package is available taped and reeled. Add the suffix R to the device type. (e.g., LM358DR)

schematic (each amplifier)



2 Operational Amplifiers

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM158, LM258, LM258A LM358, LM358A	LM2904	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		0.3 to 32	0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	[illegible]	−55 to [illegible]		°C
	LM2[illegible], LM258A	−25 to 85		°C
	[illegible]	0 to 70		°C
	[illegible]		−40 to 105	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, or U package	300	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (LM158)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (all others)	825 mW	6.6 mW/°C	528 mW	429 mW	–
P	1000 mW	8.0 mW/°C	640 mW	520 mW	–
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

2
Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158, LM258			LM358			LM2904			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7			7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10			10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	[illegible]		−20	−250	nA
			Full range			−300			[illegible]			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			V
			Full range	0 to V_{CC} − 2			0 to V_{CC} − 2			0 to V_{CC} − 2			
V_{OH}	High-level output voltage	$R_L \geq 2$ kΩ	25°C	V_{CC} − 1.5			V_{CC} − 1.5						V
		$R_L \geq 10$ kΩ	25°C							V_{CC} − 1.5			
		V_{CC} = MAX, R_L = 2 kΩ,	Full range	26			26			22			
		V_{CC} = MAX, $R_L \geq 10$ kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	$R_L \leq 10$ kΩ	Full range		5	20		5	20		5	100	mV

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25 °C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min	25 °C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to MAX	25 °C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25 °C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25 °C	−20	−30		−20	−30		−20	−30		mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 5 V	25 °C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25 °C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25 °C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1	2		1	2		1	2	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2904, 30 V for the others. Full range is −55 °C to 125 °C for LM158, −25 °C to 85 °C for LM258, 0 °C to 70 °C for LM358, and −40 °C to 105 °C for LM2904.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		[illegible]3A			[illegible]			UNIT
				MIN	[illegible]	MAX	MIN	[illegible]	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 v to 30 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7	15		7	20	μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10	200		10	300	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	80		−15	−100	nA
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	$R_L \geq 2\ k\Omega$	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$			V
		V_{CC} = 30 V, $R_L = 2\ k\Omega$	Full range	26			26			
		V_{CC} = 30 V, $R_L \geq 10\ k\Omega$	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leq 10\ k\Omega$	Full range		5	20		5	20	mV

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio		25°C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		dB
V_{o1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	20	30	60	20	30	60	mA
			Full range	10			10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1	2			2	

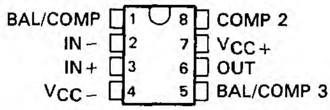
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25°C to 85°C for LM258A and 0°C to 70°C to LM358A.

2 Operational Amplifiers

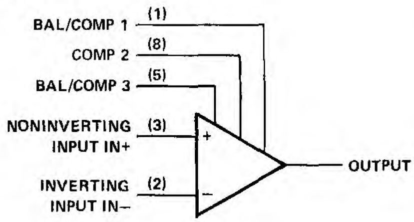
D2219, JUNE 1976 – REVISED OCTOBER

- **Small-Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/ μs Min**
- **Bias Current . . . 250 nA Max (LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



description

The LM218 and LM318 are precision, high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 150 V/μs and almost double the bandwidth. Over compensation may be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for 0.1% error band to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample and hold circuits, and general purpose amplifiers.

The LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

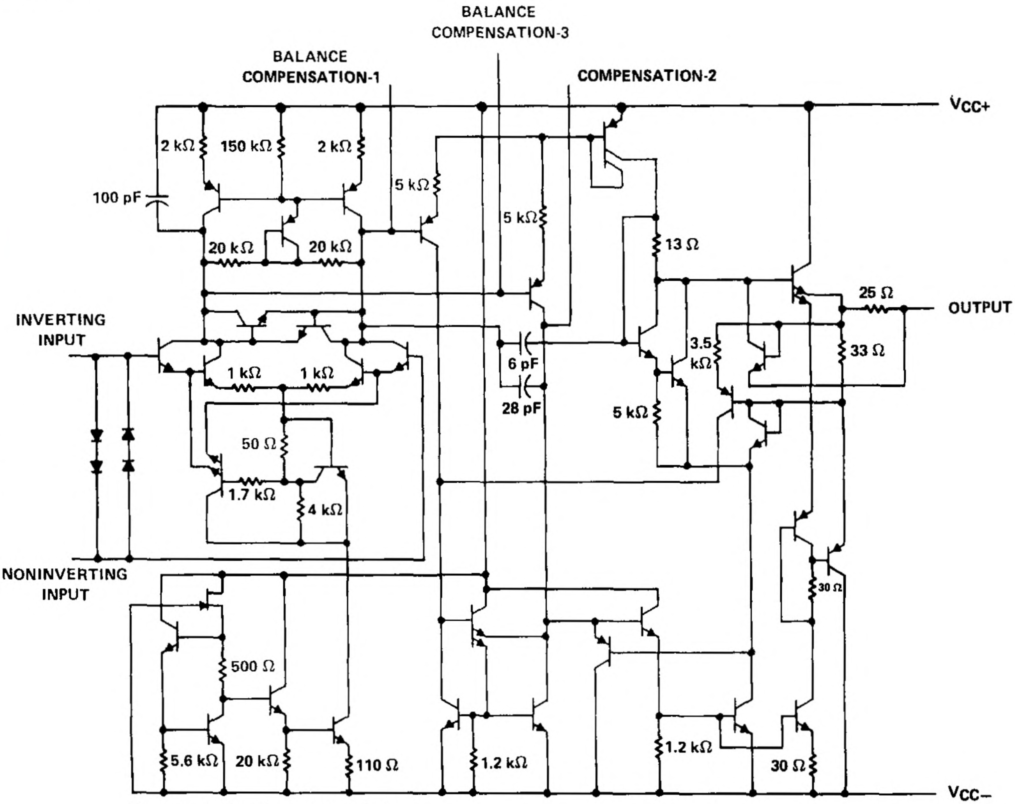
T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LM318D	LM318JG	LM318P
−25°C to 85°C	4 mV	LM218D	LM218JG	LM218P

The D packages are available taped and reeled. Add the suffix R to the device type (e.g., LM318DR).

2

Operational Amplifiers

schematic



Component values shown are nominal.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)		20	20	V
Supply voltage, V_{CC-} (see Note 1)		−20	−20	V
Input voltage (either input, see Notes 1 and 2)		±15	±15	V
Differential input current (see Note 3)		±10	±10	mA
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. For the LM218 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW
JG	500 mW	6.6 mW/°C	74°C	500 mW	429 mW
P	500 mW	N/A	N/A	500 mW	500 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	$V_O = 0$	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		120	250		150	500	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm15$ V	Full range	±11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm15$ V, $R_L = 2$ kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm} = \pm15$ V	25°C		15			15		MHz
r_i	Input resistance		25°C	1	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	Full range	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	No load, $V_O = 0$	25°C		5	8		5	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM218 is −25°C to 85°C and for LM318 is 0°C to 70°C.

Note 5: Unless otherwise noted, $V_{CC} = \pm5$ V to ±20 V. All typical values are at $V_{CC\pm} = \pm15$ V, $T_A = 25$°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC} = 15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_I = 10$ V,	$C_L = 10$ pF,	See Figure 1	50	70		V/µs

PARAMETER MEASUREMENT INFORMATION

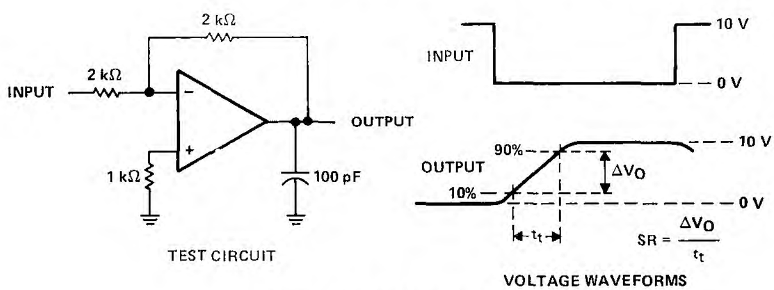
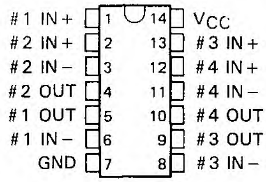


FIGURE 1. SLEW RATE

D2531, JULY 1979—REVISED AUGUST 1988

- **Wide Range of Supply Voltages, Single or Dual Supplies**
- **Wide Bandwidth**
- **Large Output Voltage Swing**
- **Output Short-Circuit Protection**
- **Internal Frequency Compensation**
- **Low Input Bias Current**
- **Designed to be Interchangeable with National Semiconductor LM2900 and LM3900, Respectively**

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



description

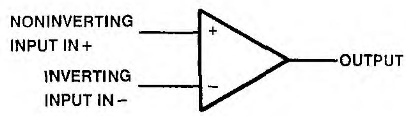
These devices consist of four independent, high-gain frequency-compensated Norton operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible. The low supply current drain is essentially independent of the magnitude of the supply voltage. These devices provide wide bandwidth and large output voltage swing.

The LM2900 is characterized for operation from −40°C to 85°C, and the LM3900 is characterized for operation from 0°C to 70°C.

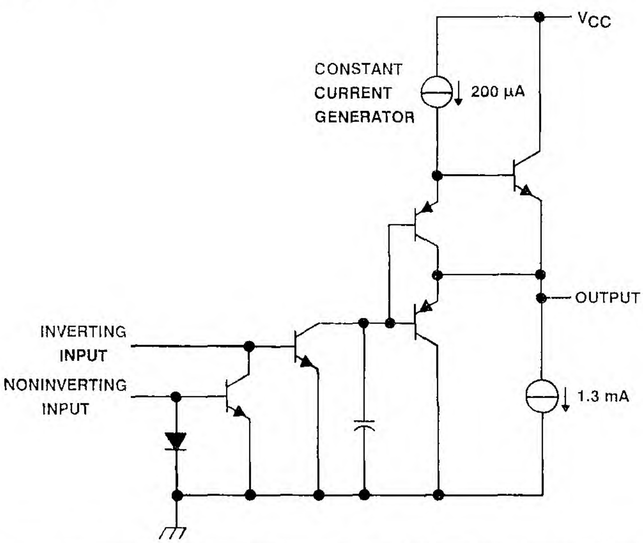
AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC DIP (N)	CERAMIC DIP (J)
0°C to 70°C	LM3900N	LM3900J
−40°C to 85°C	LM2900N	LM2900J

symbol (each amplifier)



schematic (each amplifier)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM2900	LM3900	UNIT
Supply voltage, V_{CC} (see Note 1)		36	36	V
Input current		20	20	mA
Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature (see Note 2)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J Package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	LM2900		LM3900		UNIT
	MIN	MAX	MIN	MAX	
Input current (see Note 3)		−1		−1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

NOTE 3: Clamp transistors are included that prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately −1 mA. Negative input currents in excess of −4 mA will cause the output voltage to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode current biasing can be used to prevent negative input voltages.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM2900			LM3900			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IB}	Input bias current (inverting input)	$I_{I+} = 0$	T_A = 25°C		30	200		30	200	nA
			T_A = Full range		300			300		
$\frac{I_{I-}}{I_{I+}}$	Mirror gain	I_{I+} = 20 μA to 200 μA, T_A = Full range, See Note 4		0.9		1.1	0.9		1.1	μA/μA
	Change in mirror gain				2	5		2	15	%
	Mirror current	$V_{I+} = V_{I-}$, T_A = Full range, See Note 4			10	500		10	500	μA
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ, f = 100 Hz		1.2	2.8		1.2	2.8		V/mV
r_i	Input resistance (inverting input)				1			1		MΩ
r_o	Output resistance				8			8		kΩ
B_1	Unity-gain bandwidth (inverting input)				2.5			2.5		MHz
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)				70			70		dB
V_{OH}	High-level output voltage	$I_{I+} = 0$, $I_{I-} = 0$	R_L = 2 kΩ	13.5			13.5			V
			V_{CC} = 30 V, No load		29.5			29.5		
V_{OL}	Low-level output voltage	$I_{I+} = 0$, I_{I-} = 10 μA, R_L = 2 kΩ			0.09	0.2		0.09	0.2	V
I_{OHS}	Short-circuit output current (output internally high)	$I_{I+} = 0$, $I_{I-} = 0$, $V_O = 0$		−6	−18		−6	−10		mA
	Pull-down current			0.5	1.3		0.5	1.3		mA
I_{OL}	Low-level output current‡	I_{I-} = 5 μA, V_{OL} = 1 V			5			5		mA
I_{CC}	Supply current (four amplifiers)	No load			6.2	10		6.2	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for LM2900, and 0°C to 70°C for LM3900.
‡ The output current-sink capability can be increased for large-signal conditions by overdriving the inverting input.
NOTE 4: These parameters are measured with the output balanced midway between V_{CC} and ground.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	Low-to-high output	V_O = 10 V, C_L = 100 pF, R_L = 2 kΩ		0.5		V/μs
		High-to-low output			20		

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT (INVERTING INPUT)
vs
FREE-AIR TEMPERATURE

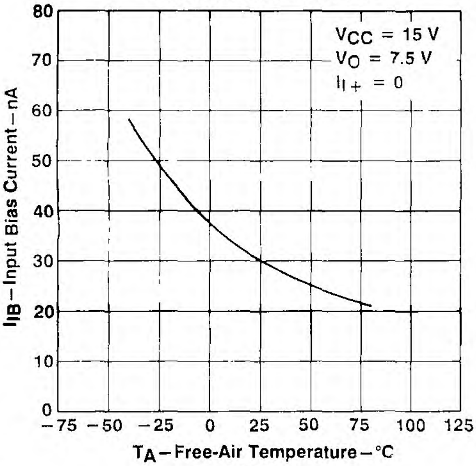

FIGURE 1

MIRROR GAIN
vs
FREE-AIR TEMPERATURE

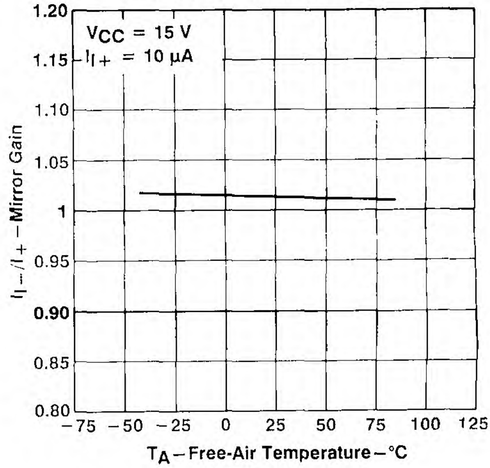

FIGURE 2

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

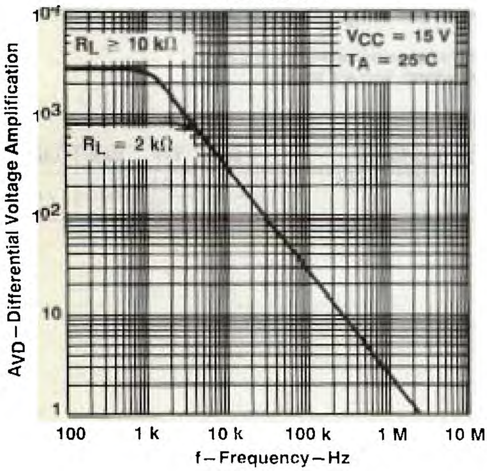

FIGURE 3

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

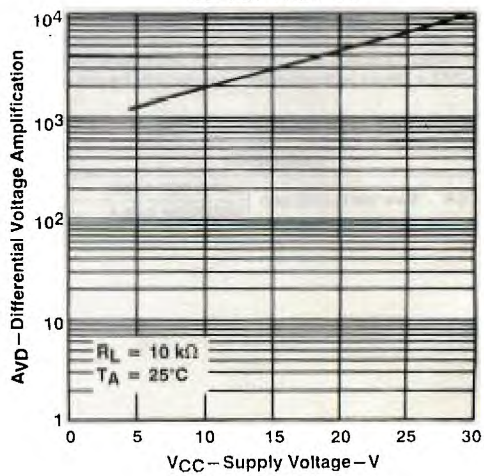

FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

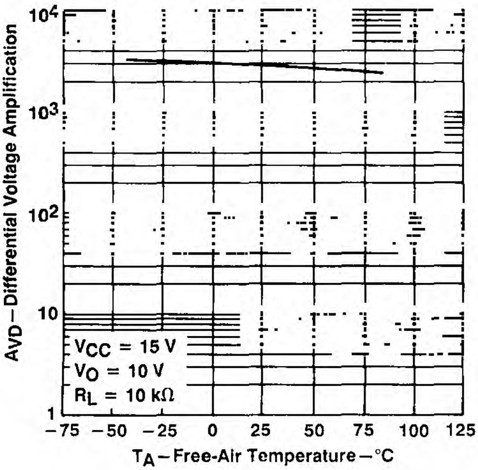

FIGURE 5

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

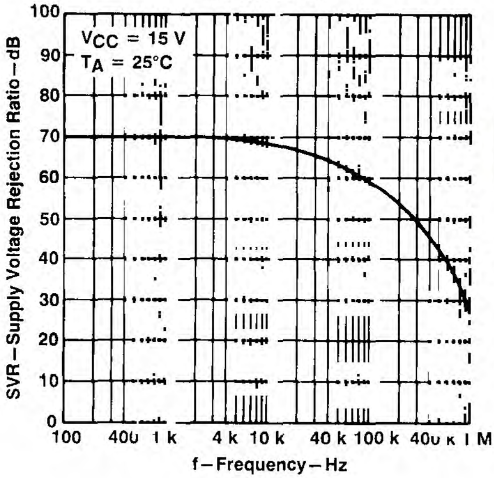

FIGURE 6

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

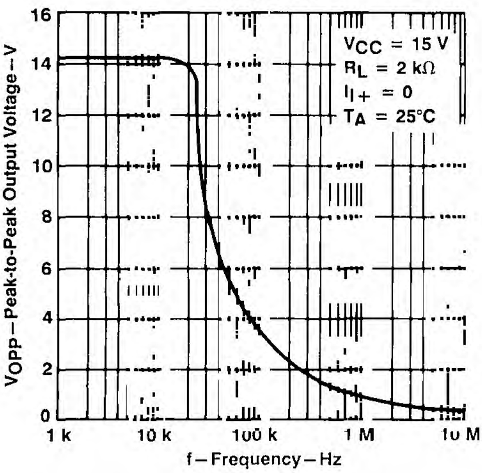

FIGURE 7

LM2900
SHORT-CIRCUIT OUTPUT CURRENT
(OUTPUT INTERNALLY HIGH)
vs
SUPPLY VOLTAGE

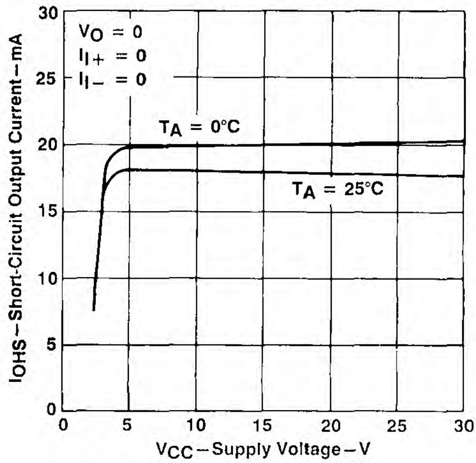

FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

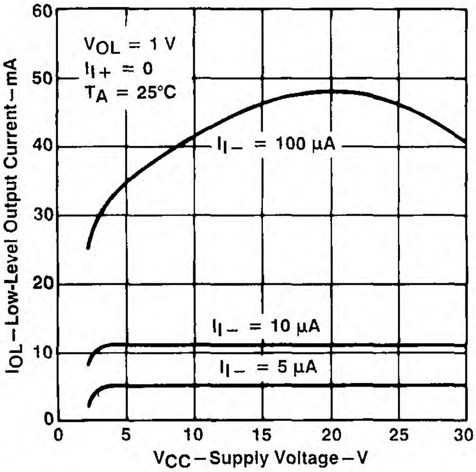

FIGURE 9

PULL-DOWN CURRENT
vs
SUPPLY VOLTAGE

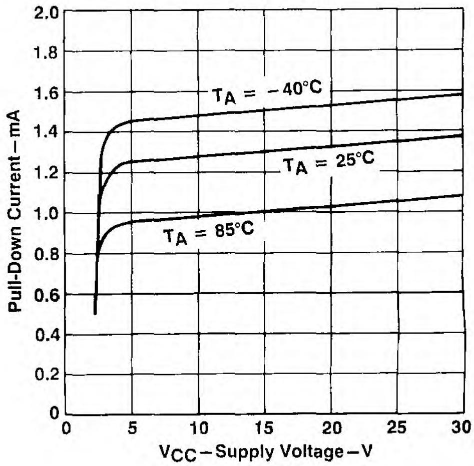

FIGURE 10

PULL-DOWN CURRENT
vs
FREE-AIR TEMPERATURE

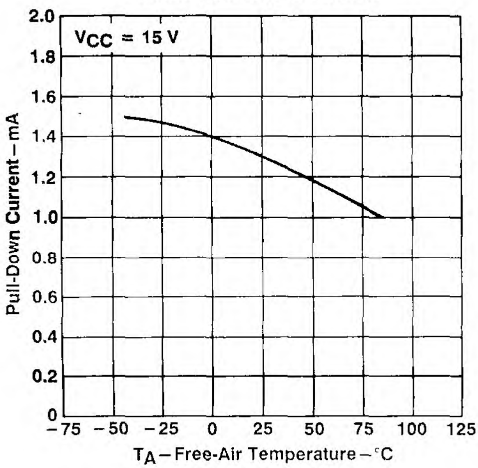

FIGURE 11

TOTAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE

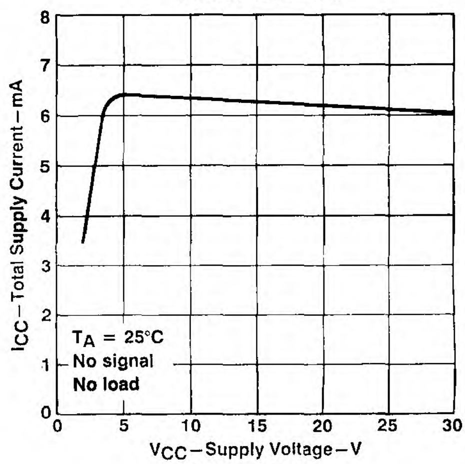

FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL APPLICATION DATA

Norton (or current-differencing) amplifiers can be used in most standard general-purpose op-amp applications. Performance as a dc amplifier in a single-power-supply mode is not as precise as a standard integrated-circuit operational amplifier operating from dual supplies. Operation of the amplifier can be best be understood by noting that input currents are differenced at the inverting input terminal and this current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near (or even below) ground.

Internal transistors clamp negative input voltages at approximately −0.3 V but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately −100 μA.

Noise immunity of a Norton amplifier is less than that of standard bipolar amplifiers. Circuit layout is more critical since coupling from the output to the noninverting input can cause oscillations. Care must also be exercised when driving either input from a low-impedance source. A limiting resistor should be placed in series with the input lead to limit the peak input current. Current up to 20 mA will not damage the device but the current mirror on the noninverting input will saturate and cause a loss of mirror gain at higher current levels, especially at high operating temperatures.

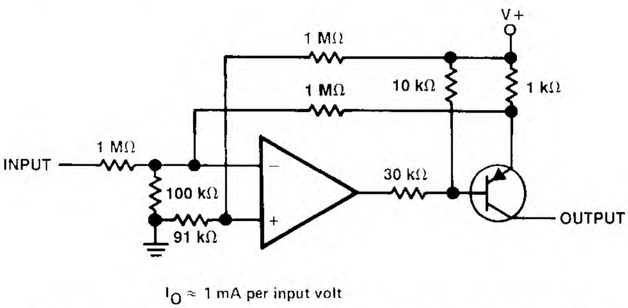


FIGURE 13. VOLTAGE-CONTROLLED CURRENT SOURCE

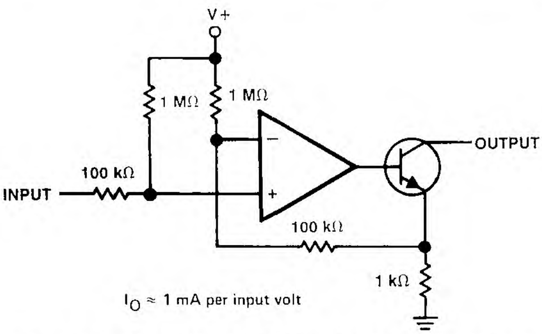
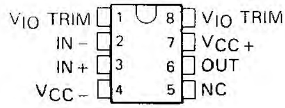


FIGURE 14. VOLTAGE-CONTROLLED CURRENT SINK

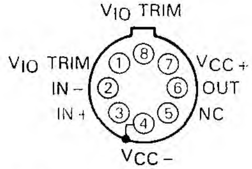
LT1001 PRECISION OPERATIONAL AMPLIFIER

- **Low Input Offset Voltage:**
  LT1001AM . . . 15 µV Max
  LT1001AC . . . 25 µV Max
  LT1001M, LT1001C . . . 60 µV Max
- **Low Offset Voltage Temperature Coefficient:**
  LT1001AM, LT1001AC . . . 0.6 µV/°C Max
  LT1001M, LT1001C . . . 1 µV/°C Max
- **Low Input Bias Current:**
  LT1001AM, LT1001AC . . . ±2 nA Max
  LT1001M, LT1001C . . . ±4 nA Max
- **Low Common-Mode Rejection Ratio:**
  LT1001AM, LT1001AC . . . 114 dB Min
  LT1001M, LT1001C . . . 110 dB Min
- **Low Supply Voltage Rejection Ratio:**
  LT1001AM, LT1001AC . . . 110 dB Min
  LT1001M, LT1001C . . . 106 dB Min
- **Low Power Dissipation:**
  LT1001AM, LT1001AC . . . 75 mW Max
  LT1001M, LT1001C . . . 80 mW Max
- **Low Peak-to-Peak Equivalent Input Noise Voltage . . . 0.3 µV Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L package) is in electrical contact with the case.

description

The LT1001 is a precision operational amplifier suited for applications such as thermocouple amplifiers, strain gauge amplifiers, low-level signal processing, and high-accuracy data acquisition. In the design, processing, and testing of the device, particular attention has been paid to optimizing the entire distribution of several key parameters. The input offset voltage of all units is less than 60 µV, and the LT1001AM is specified at 15 µV maximum. Power dissipation is nearly halved compared to the most popular precision operational amplifiers without adversely affecting noise or speed performance. The output drive capability of the LT1001 is enhanced with voltage gain at a load current of 10 mA.

The specifications of the low-cost commercial-temperature device, the LT1001C, have been significantly improved when compared to equivalent grades of similar precision amplifiers. The input bias current, input offset current, and common-mode and supply voltage rejection ratios of the LT1001C offer performance previously attainable only with high-cost, selected grades of other devices.

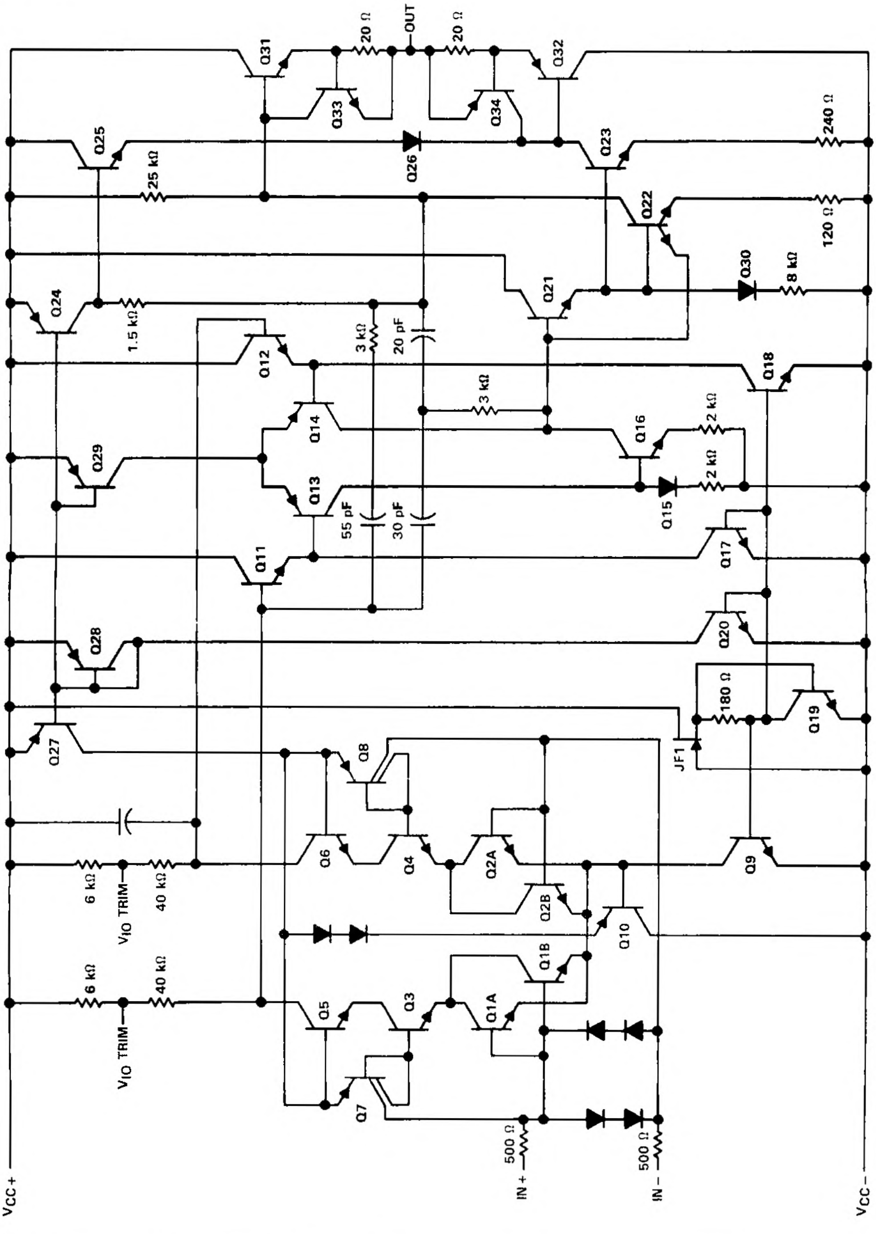
The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C	60 µV	LT1001CD	LT1001CJG	LT1001CL	LT1001CP
to 70°C	25 µV		LT1001ACJG	LT1001ACL	LT1001ACP
−55°C	60 µV		LT1001MJG	LT1001ML	
to 125°C	15 µV		LT1001AMJG	LT1001AML	

The D package is available in tape and reel. Add the suffix R to the device type (e.g., LT1001CDR).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) .... 22 V
Supply voltage, V_{CC-} .... −22 V
Differential input voltage (see Note 2) .... ±30 V
Input voltage range, V_I .... ±22 V
Duration of short-circuit current at (or below) 25°C .... unlimited
Continuous power dissipation .... See Dissipation Rating Table
Operating free-air temperature range: M-suffix .... −55°C to 125°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		M-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm15$ V			±13			±13	V
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1001M MIN	LT1001M TYP	LT1001M MAX	LT1001AM MIN	LT1001AM TYP	LT1001AM MAX	UNIT
V_{IO}	Input offset voltage	See Note 3	25°C		18	60		7	15	μV
			−55°C to 125°C			160			60	
α_{VIO}	Average temperature coefficient of input offset voltage		−55°C to 125°C		0.3	1		0.2	0.6	μV/°C
	Long-term drift of input offset voltage	See Note 4			0.3	1.5		0.2	1	μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		0.4	3.8		0.3	2	nA
			−55°C to 125°C			7.6			4	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±0.7	±4		±0.5	±2	nA
			−55°C to 125°C			±8			±4	
V_{OH}	Maxiumum peak output voltage swing	R_L ≥ 2 kΩ	25°C	±13	±14		±13	±14		V
		R_L ≥ 1 kΩ	25°C	±12	±13.5		±12	±13.5		
		R_L ≥ 2 kΩ	−55°C to 125°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	400	800		450	800		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V	25°C	250	500		300	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	200			300			
r_{id}	Differential input resistance		25°C	15	80		30	100		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V	25°C	110	126		114	126		dB
			−55°C to 125°C	106			110			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±3 V to ±18 V	25°C	106	123		110	123		dB
			−55°C to 125°C	100			104			
P_D	Total power dissipation	No load	25°C		48	80		46	75	mW
		No load, $V_{CC\pm}$ = ± 3 V	25°C		4	8		4	6	
		No load	−55°C to 125°C			100			90	

NOTES: 3. The input offset voltage for all devices is measured with high-speed test equipment approximately 1 second after power is applied. The LT1001AM receives a 168-hour burn-in at 125°C or equivalent.

4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{IO} during the first 30 days is typically 2.5 μV.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1001M MIN	LT1001M TYP	LT1001M MAX	LT1001AM MIN	LT1001AM TYP	LT1001AM MAX	UNIT
SR	Slew rate at unity gain	R_L ≥ 2 kΩ		0.1	0.25		0.1	0.25		V/μs
ϕ_m	Phase margin at unity gain	A_V = 40 dB,	T_A = 25°C		60°			63°		
		R_S = 100 Ω,	T_A = MIN		63°			63°		
		C_L = 10 pF	T_A = MAX		57°			57°		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			0.3	0.6		0.3	0.6	μV
V_n	Equivalent input noise voltage	f = 10 Hz			10.5	18		10.3	18	nV/√Hz
		f = 1 MHz			9.8	11		9.6	11	
GBW	.. bandwidth product			0.4	0.8		0.4	0.8		MHz

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1001C MIN	LT1001C TYP	LT1001C MAX	LT1001AC MIN	LT1001AC TYP	LT1001AC MAX	UNIT
V_{IO}	Input offset voltage	See Note 5	25°C		18	60		10	25	µV
			0°C to 70°C			110			60	
α_{VIO}	Average temperature coefficient of input offset voltage		0°C to 70°C		0.3	1		0.2	0.6	µV/°C
	Long-term drift of input offset voltage	See Note 4			0.3	1.5		0.2	1	µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		0.4	3.8		0.3	2	nA
			0°C to 70°C			5.3			3.5	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±0.7	±4		±0.5	±2	nA
			0°C to 70°C			±5.5			±3.5	
V_{OH}	Maximum peak output voltage swing	$R_L \geq 2\ k\Omega$	25°C	±13	±14		±13	±14		V
		$R_L \geq 1\ k\Omega$	25°C	±12	±13.5		±12	±13.5		
		$R_L \geq 2\ k\Omega$	0°C to 70°C	±12.5			±12.5			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, V_O = ±12 V	25°C	400	800		450			V/mV
		$R_L \geq 1\ k\Omega$, V_O = ±10 V	25°C	250	500		300			
		$R_L \geq 2\ k\Omega$, V_O = ±10 V	0°C to 70°C	250			350			
r_{id}	Differential input resistance		25°C	15	80		30	100		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V	25°C	110	126		114	126		dB
			0°C to 70°C	106			110			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±3 V to ±18 V	25°C	106	123		110	123		dB
			0°C to 70°C	103			106			
P_D	Total power dissipation	No load	25°C		48	80		46	75	mW
		No load, $V_{CC\pm}$ = ± 3 V	25°C		4	8		4	6	
		No load	0°C to 70°C			90			85	

Notes: 4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{IO} during the first 30 days is typically 2.5 µV.

5. The input offset voltage for all devices is measured with high-speed test equipment approximately 1 second after power is applied.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1001C MIN	LT1001C TYP	LT1001C MAX	LT1001AC MIN	LT1001AC TYP	LT1001AC MAX	UNIT
SR	Slew rate at unity gain	$R_L \geq 2\ k\Omega$		0.1	0.25		0.1	0.25		V/µs
ϕ_m	Phase margin at unity gain	A_V = 40 dB,	T_A = 25°C		60°			63°		
		R_S = 100 Ω,	T_A = MIN		63°			63°		
		C_L = 10 pF	T_A = MAX		57°			57°		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			0.3	0.6		0.3	0.6	µV
V_n	Equivalent input noise voltage	f = 10 Hz			10.5	18		10.3	18	nV/√Hz
		f = 1 MHz			9.8	11		9.6	11	
GBW	[illegible] bandwidth product			0.4	0.8		0.4	0.8		MHz

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

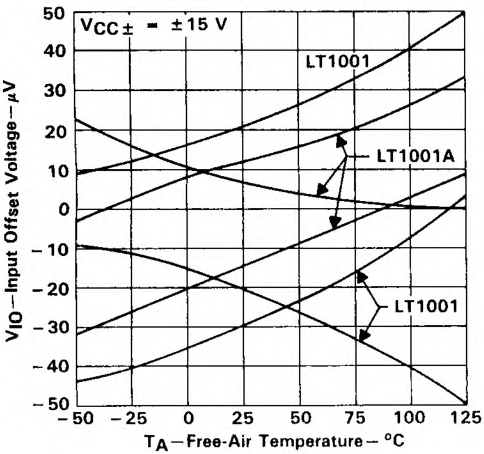


FIGURE 1

WARM-UP CHANGE
IN INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

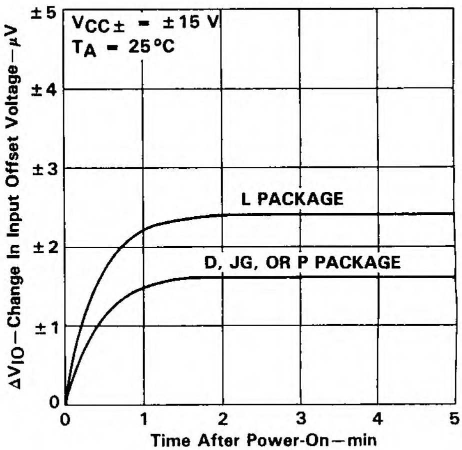


FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

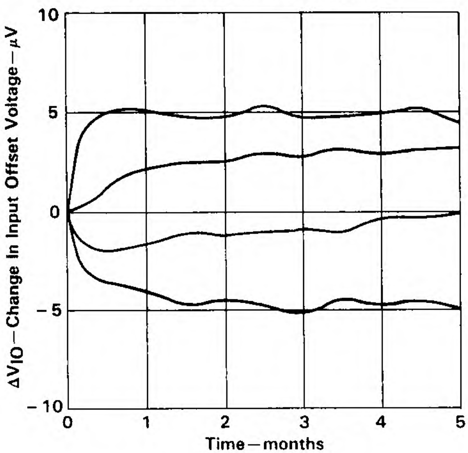


FIGURE 3

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
and INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

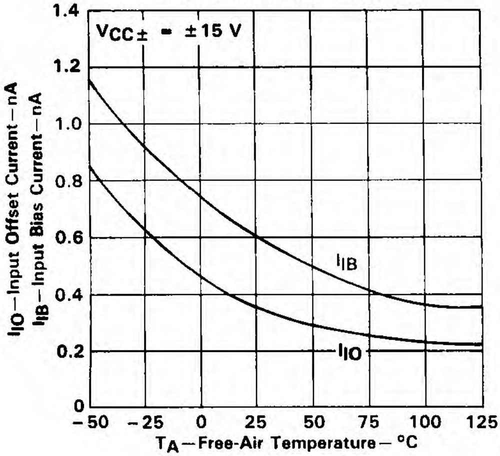


FIGURE 4

INPUT BIAS CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

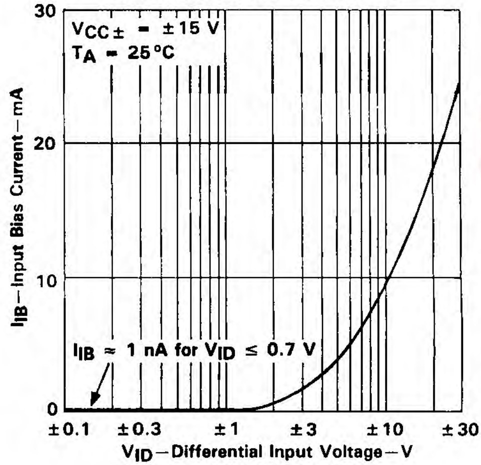


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

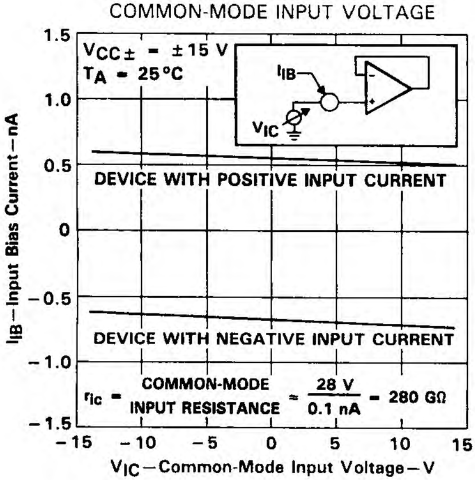


FIGURE 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

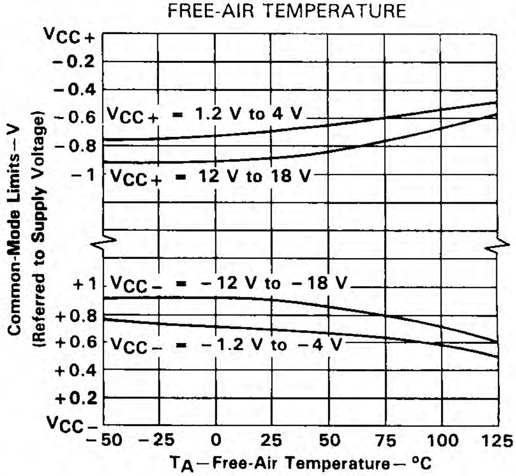


FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

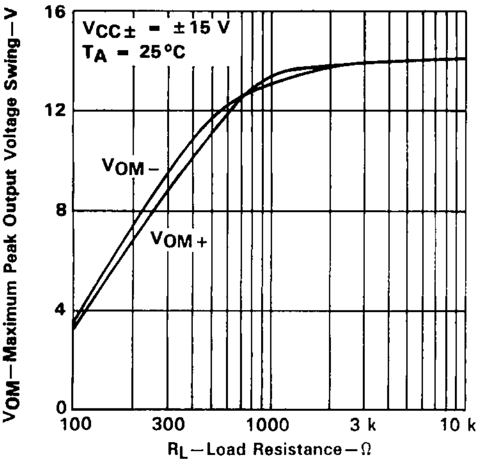


FIGURE 8

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
FREQUENCY

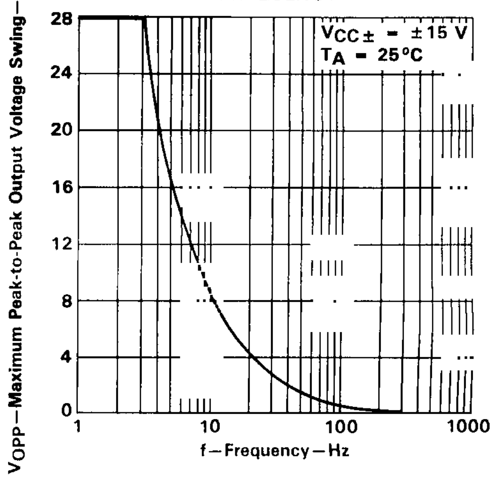


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

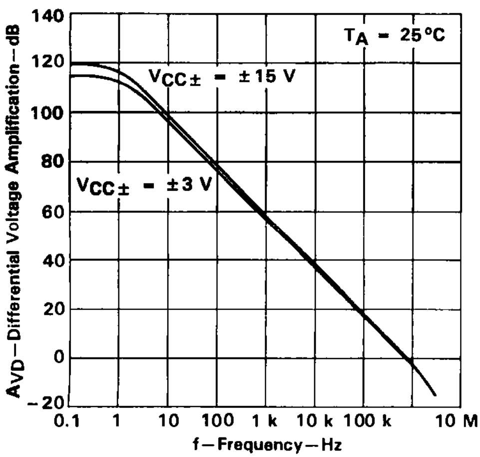


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

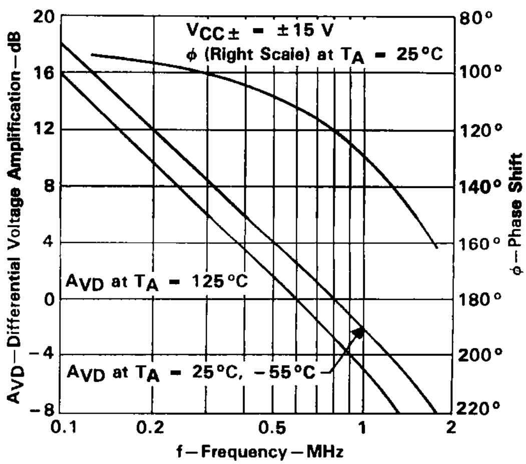


FIGURE 11

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

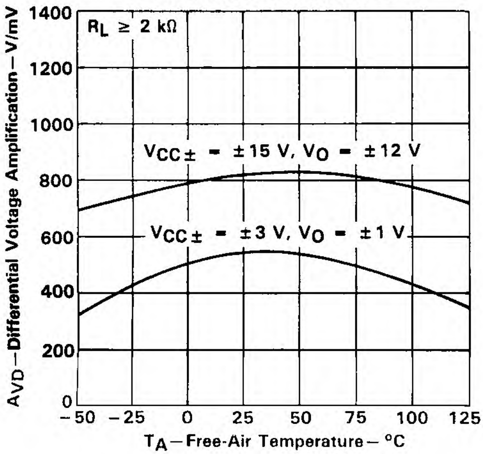


FIGURE 12

OUTPUT IMPEDANCE
vs
FREQUENCY

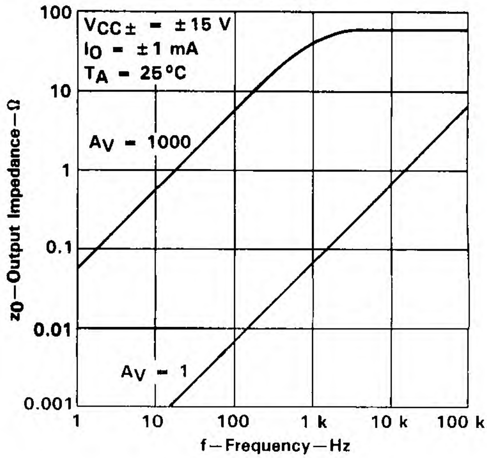


FIGURE 13

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

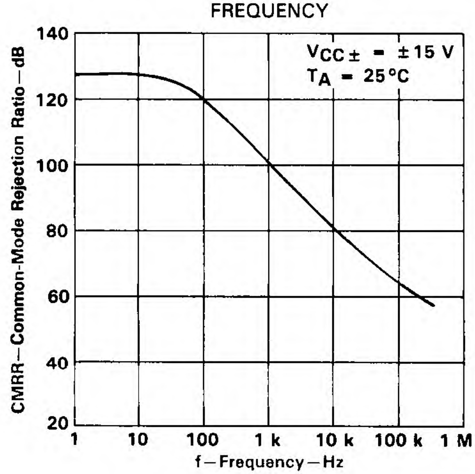


FIGURE 14

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

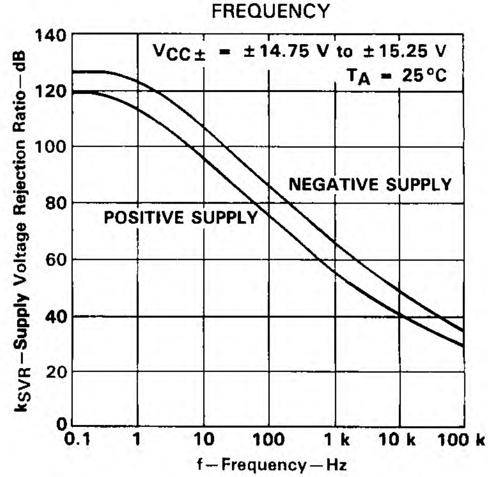


FIGURE 15

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

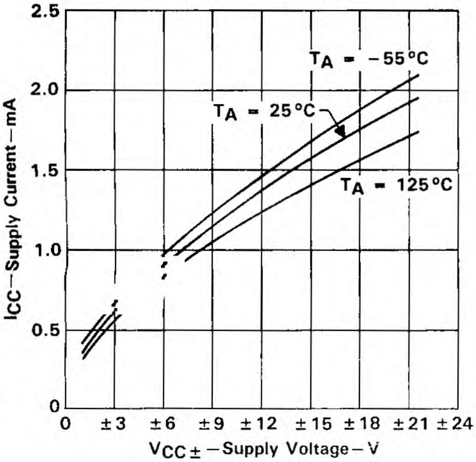


FIGURE 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

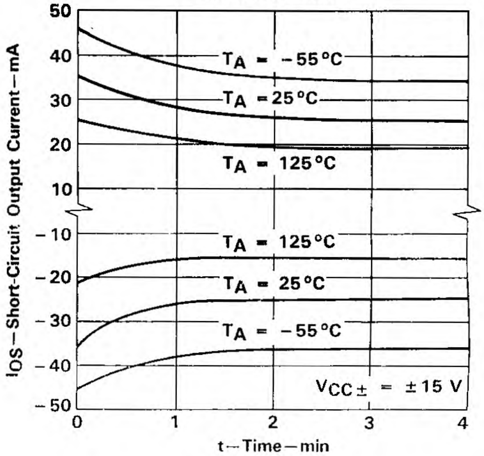


FIGURE 17

EQUIVALENT INPUT NOISE VOLTAGE
and EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

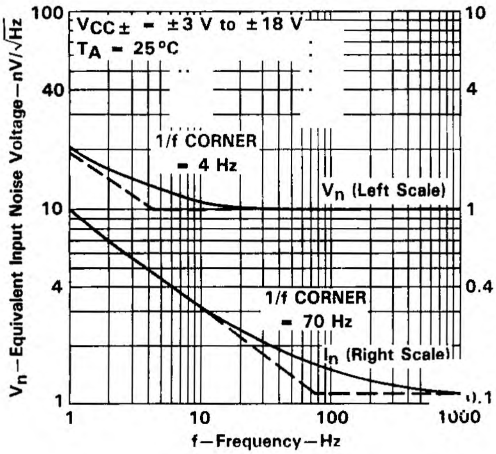


FIGURE 18

OUTPUT NOISE VOLTAGE
OVER A
10-SECOND PERIOD

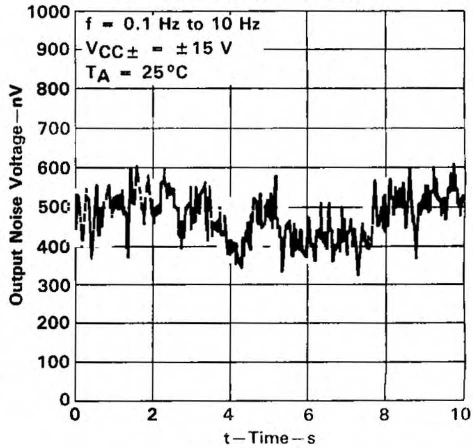


FIGURE 19

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

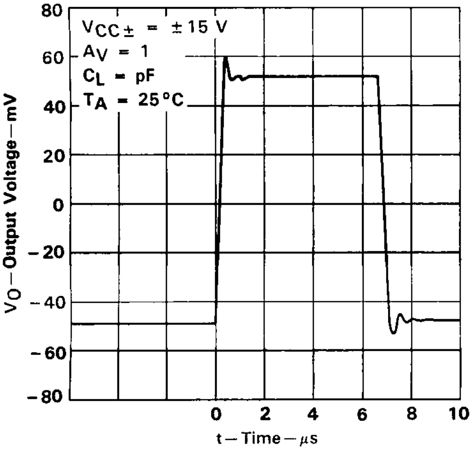


FIGURE 20

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

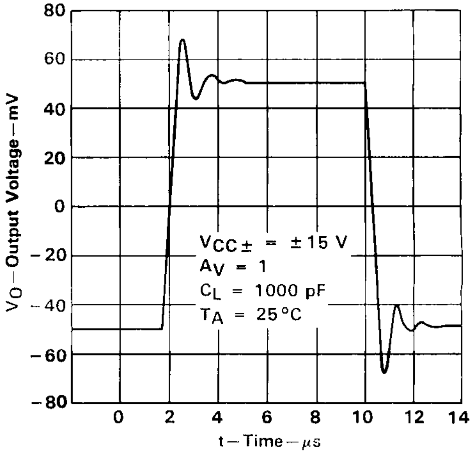


FIGURE 21

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE-RESPONSE

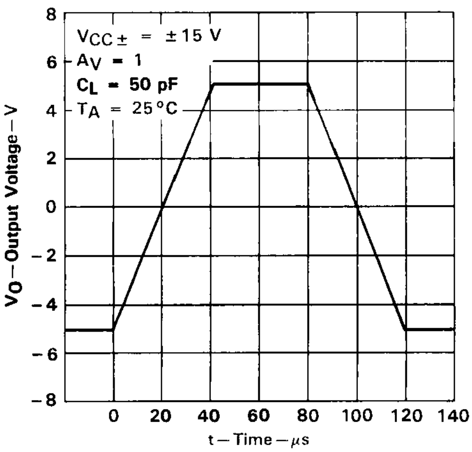


FIGURE 22

VOLTAGE-FOLLOWER OVERSHOOT
vs
LOAD CAPACITANCE

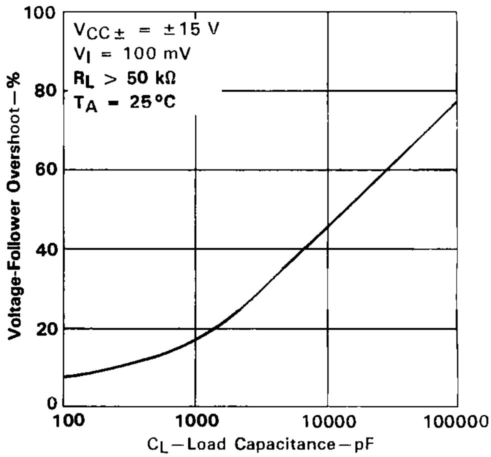
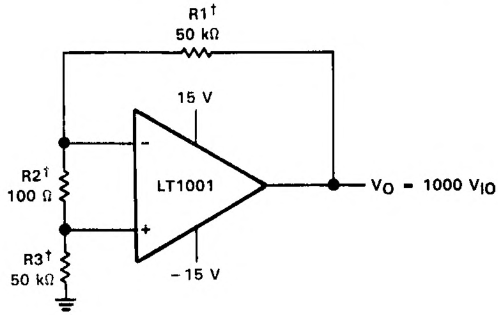


FIGURE 23

2

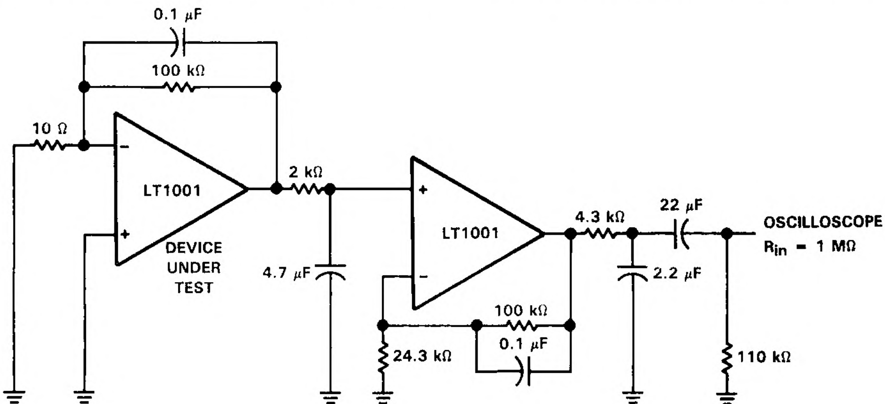
Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION



†Resistors must have low thermoelectric potential.
NOTE: This circuit is also used as the burn-in configuration for the LT1001 with supply voltages increased to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, and A_V = 100.

FIGURE 24. TEST CIRCUIT FOR INPUT OFFSET VOLTAGE AND ITS TEMPERATURE COEFFICIENT



NOTES: A. A_V = 50,000.
B. The device under test should be warmed up for three minutes and shielded from air currents.

FIGURE 25. TEST CIRCUIT FOR 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE (MEASURED OVER A 10-SECOND INTERVAL)

TYPICAL APPLICATION DATA

application notes

The LT1001 series units may be inserted directly into OP-07 or LM108A sockets with or without removing external frequency compensation or nulling components.

The LT1001 is specified over a wide range of supply voltages from ±3 V to ±18 V. Operation with lower supply voltages (e.g., two Ni-Cad batteries) is possible down to ±1.2 V. However, with ±1.2-V supplies, the device is stable only in closed-loop gains of 2 or higher (or inverting gains of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent temperature coefficient of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

input offset voltage adjustment

The input offset voltage and temperature coefficient of the LT1001 are permanently trimmed to a low level at wafer test. However, if further adjustment of V_{IO} is necessary, nulling with a 10-kΩ or 20-kΩ potentiometer will not degrade the temperature coefficient. Trimming to a value other than zero creates a temperature coefficient change of (V_{IO}/300) µV/°C. For example, if V_{IO} is adjusted to 300 µV, the change in the temperature coefficient will be 1 µV/°C. The adjustment range with a 10-kΩ or 20-kΩ potentiometer is approximately ±2.5 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 26 has an approximate null range of ±100 µV.

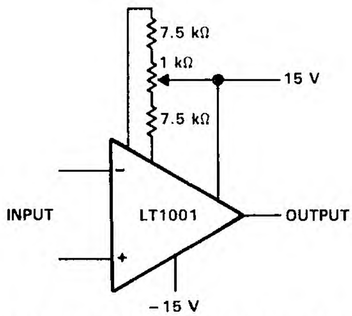
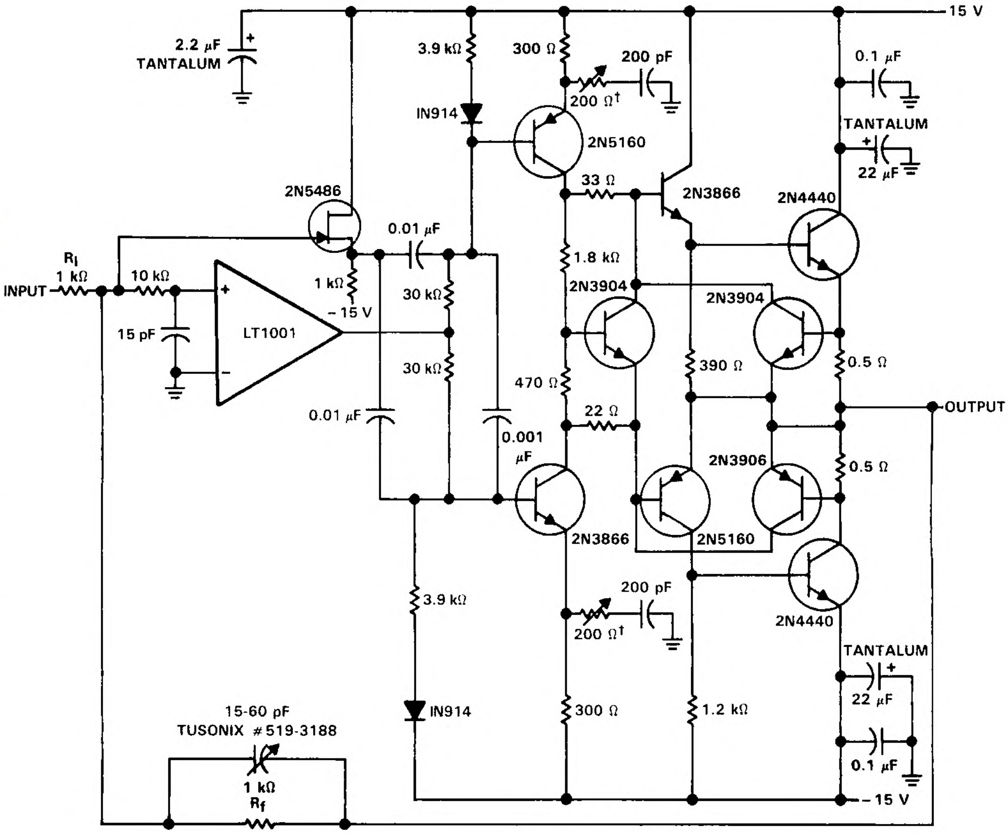


FIGURE 26. IMPROVED SENSITIVITY ADJUSTMENT

TYPICAL APPLICATION DATA



†Adjust for best square wave at output.
NOTE: Full-power bandwidth is 8 MHz.

FIGURE 27. DC-STABILIZED 1000-V/μs OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA

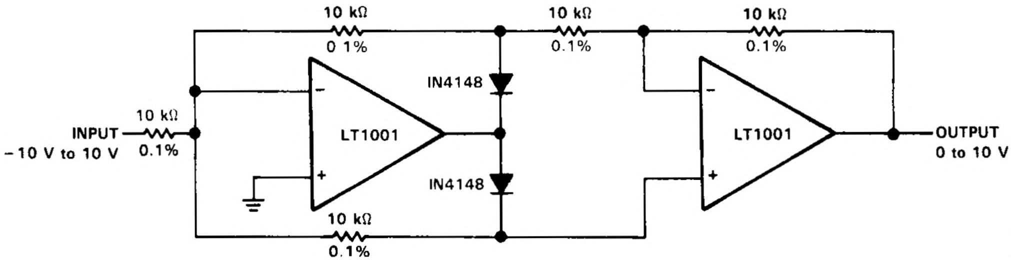


FIGURE 28. PRECISION ABSOLUTE VALUE CIRCUIT

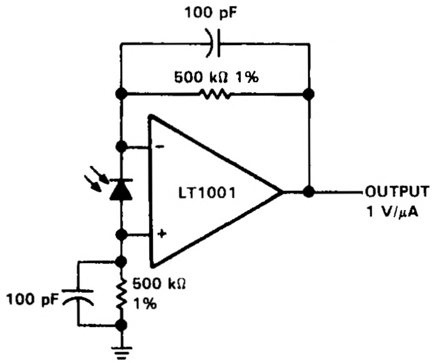


FIGURE 29. PHOTODIODE AMPLIFIER

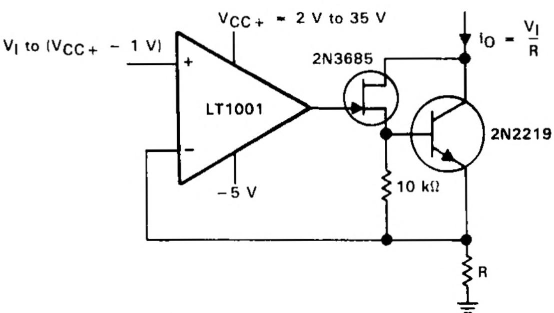
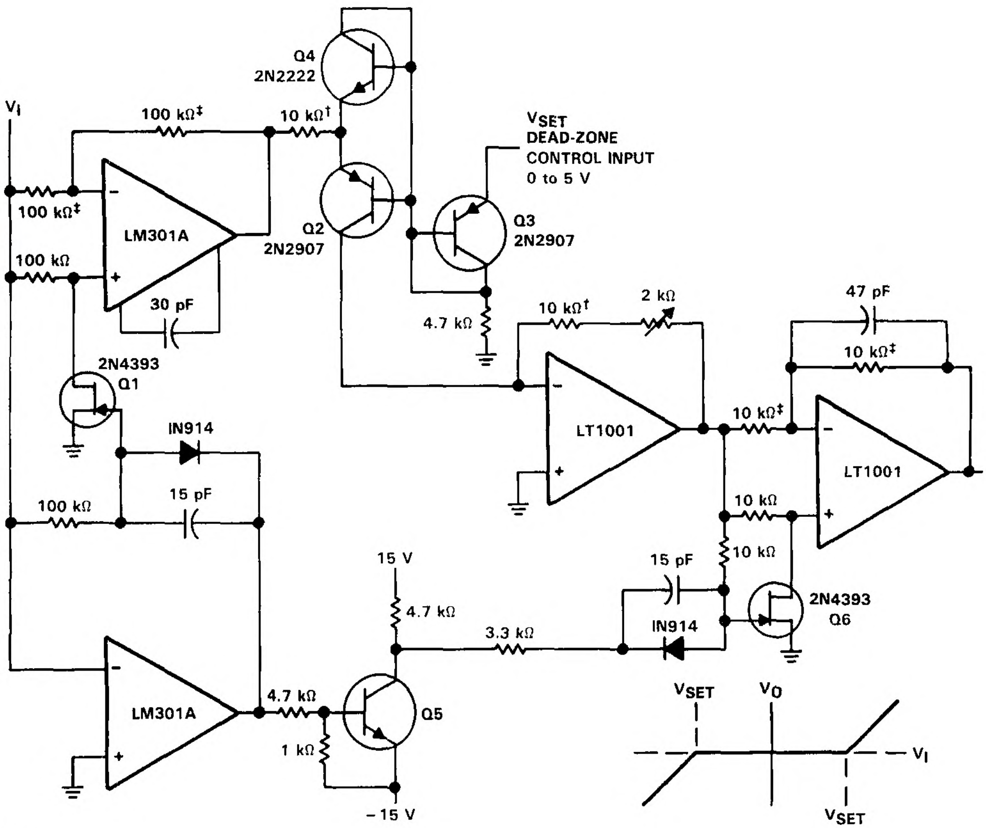


FIGURE 30. PRECISION CURRENT SINK

TYPICAL APPLICATION DATA



† 1% film
‡ Ratio match 0.05%

NOTES: A. The bipolar symmetry for this application is excellent because one device, Q2, sets both limits.
B. Q2-Q5 are a CA 3096 transistor array.

FIGURE 31. DEAD-ZONE GENERATOR

TYPICAL APPLICATION DATA

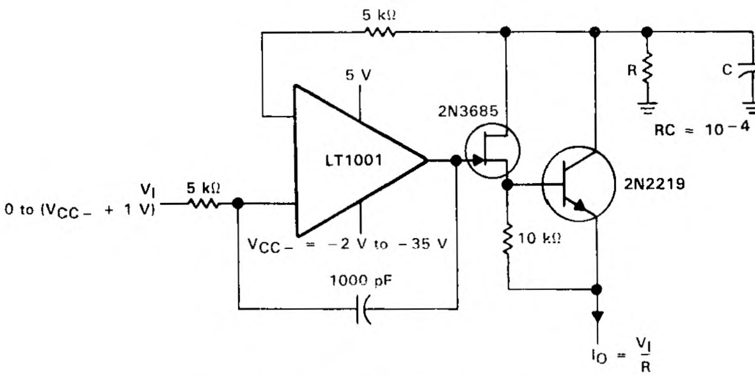
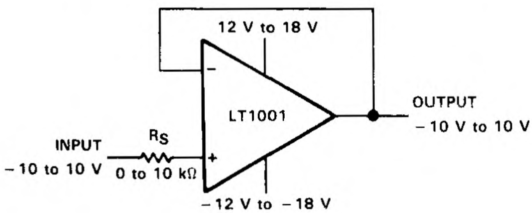


FIGURE 32. PRECISION CURRENT SOURCE



OUTPUT ACCURACY

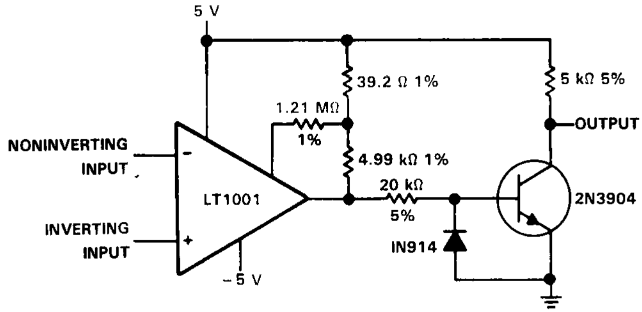
ERROR	LT1001AM T_A = 25°C MAX	LT1001C T_A = 25°C MAX	LT1001AM T_A = −55°C to 125°C MAX	LT1001C T_A = 0°C to 70°C MAX
Input Offset Voltage	15 μV	60 μV	60 μV	110 μV
Input Bias Current	20 μV	40 μV	40 μV	55 μV
Common-Mode Rejection Ratio	20 μV	30 μV	30 μV	50 μV
Supply Voltage Rejection Ratio	18 μV	30 μV	36 μV	42 μV
Differential Voltage Amplification	22 μV	25 μV	33 μV	40 μV
Worst-case Sum	95 μV	185 μV	199 μV	297 μV
Percent of Full Scale (= 20 V)	0.0005%	0.0009%	0.0010%	0.0015%

NOTE: The contributing error terms are due to input offset voltage, input bias current, voltage gain, common-mode rejection ratio, and supply voltage rejection ratio The worst-case specifications are given in the above table.

FIGURE 33. LARGE-SIGNAL VOLTAGE FOLLOWER WITH 0.001% WORST-CASE ACCURACY

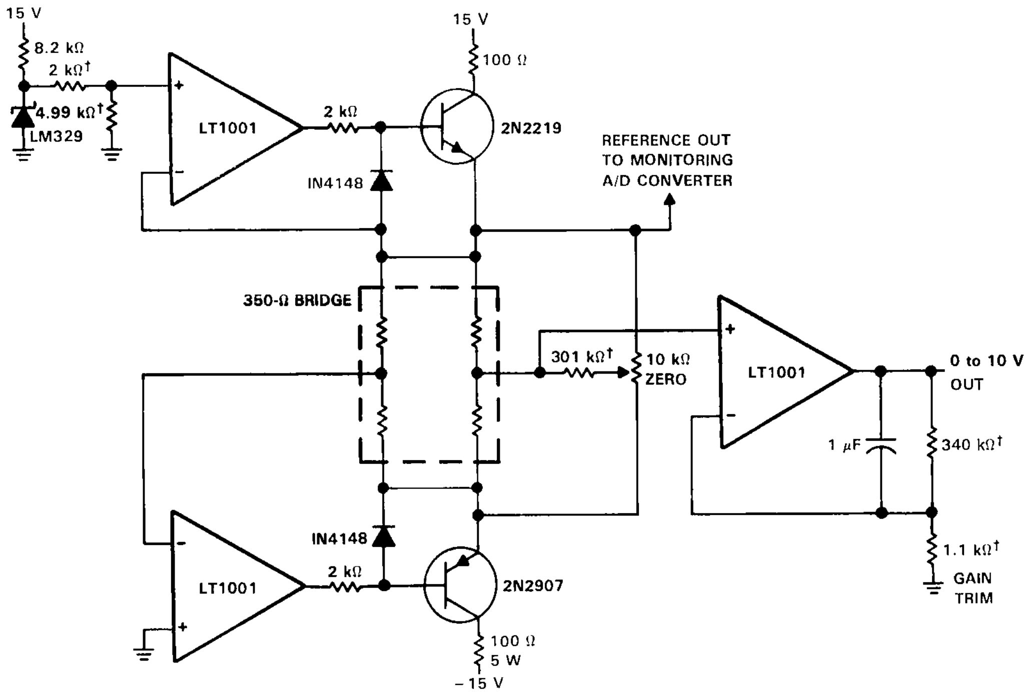
2 Operational Amplifiers

TYPICAL APPLICATION DATA



NOTE: Positive feedback to one of the nulling terminals creates 5 μV to 20 μV of hysteresis. The input offset voltage is typically changed by less than 5 μV due to the feedback.

FIGURE 34. MICROVOLT COMPARATOR WITH TTL OUTPUT



†RN60C film resistors

FIGURE 35. STRAIN-GAUGE SIGNAL CONDITIONER WITH BRIDGE EXCITATION

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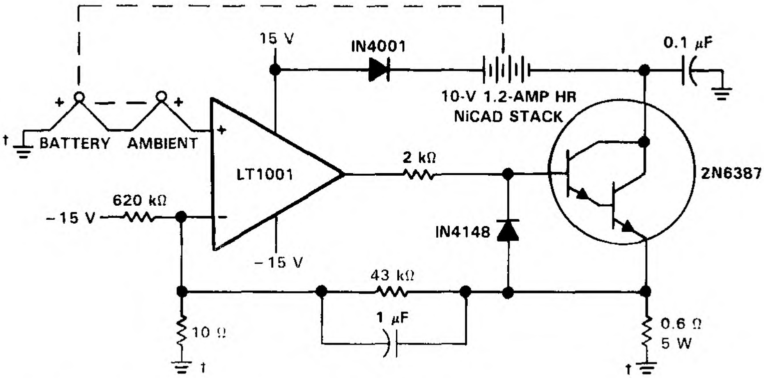
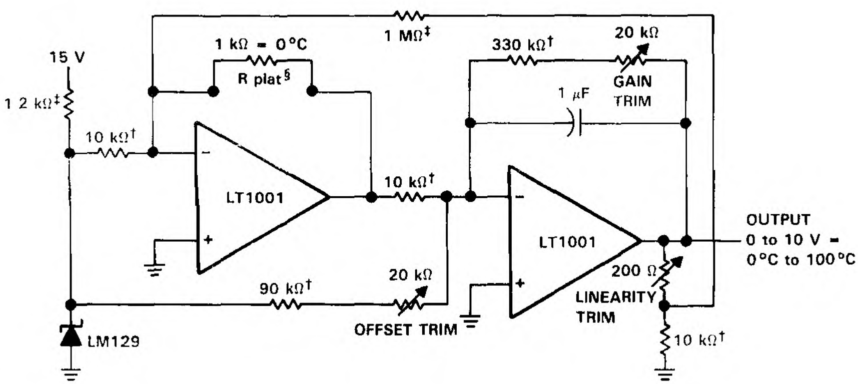
TYPICAL APPLICATION DATA



†Single point ground thermocouples are 40 µV/°C chromel-alumel (type K).
NOTE: This circuit uses the temperature difference between the battery pack mounted thermocouple and the ambient thermocouple to set the battery charge current. The peak charging current is 1 A.

FIGURE 36. THERMALLY CONTROLLED NICAD CHARGER



†ULTRONIX 105A wirewound
‡1% film
§Platinum RTD 118MF (Rosemount, Inc.)
NOTE: Trim sequence: trim offset (0°C = 1000 Ω), trim linearity (35°C = 1138.7 Ω), trim gain (100°C = 1392.6 Ω). Repeat until all three points are fixed with ±0.025°C.

FIGURE 37. LINEARIZED PLATINUM RESISTANCE THERMOMETER WITH ±0.025°C ACCURACY FOR T_A = 0°C TO 100°C

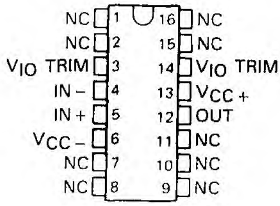
D3195, FEBRUARY 1989

- **Maximum Equivalent Input Noise Voltage:**
  3.8 nV/√Hz at 1 kHz
  4.5 nV/√Hz at 10 Hz
- **Low Peak-to-Peak Equivalent Input Noise Voltage: 60 nV Typ from 0.1 Hz to 10 Hz**
- **Slew Rate (LT1037 and LT1037A): 11 V/μs Min**

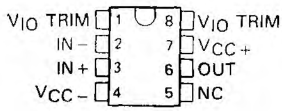
LT1007A and LT1037A Specifications:

- **High Voltage Amplification:**
  7 V/μV Min, R_L = 2 kΩ
  3 V/μV Min, R_L = 600 Ω
- **Low Input Offset Voltage 25 μV Max**
- **Low Input Offset Voltage Temperature Coefficient: 0.6 μV/°C Max**
- **Common-Mode Rejection Ratio: 117 dB Min**

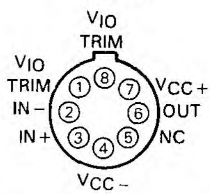
DW SMALL-OUTLINE PACKAGE
(TOP VIEW)



JG AND P
DUAL-IN-LINE PACKAGES
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

description

These monolithic operational amplifiers feature extremely low noise performance and outstanding precision and speed specifications. The typical differential voltage amplification (at T_A = 25°C) of these devices is an extremely high 20 V/μV driving a 2-kΩ load to ±12 V and 12 V/μV driving a 600-Ω load to ±10 V.

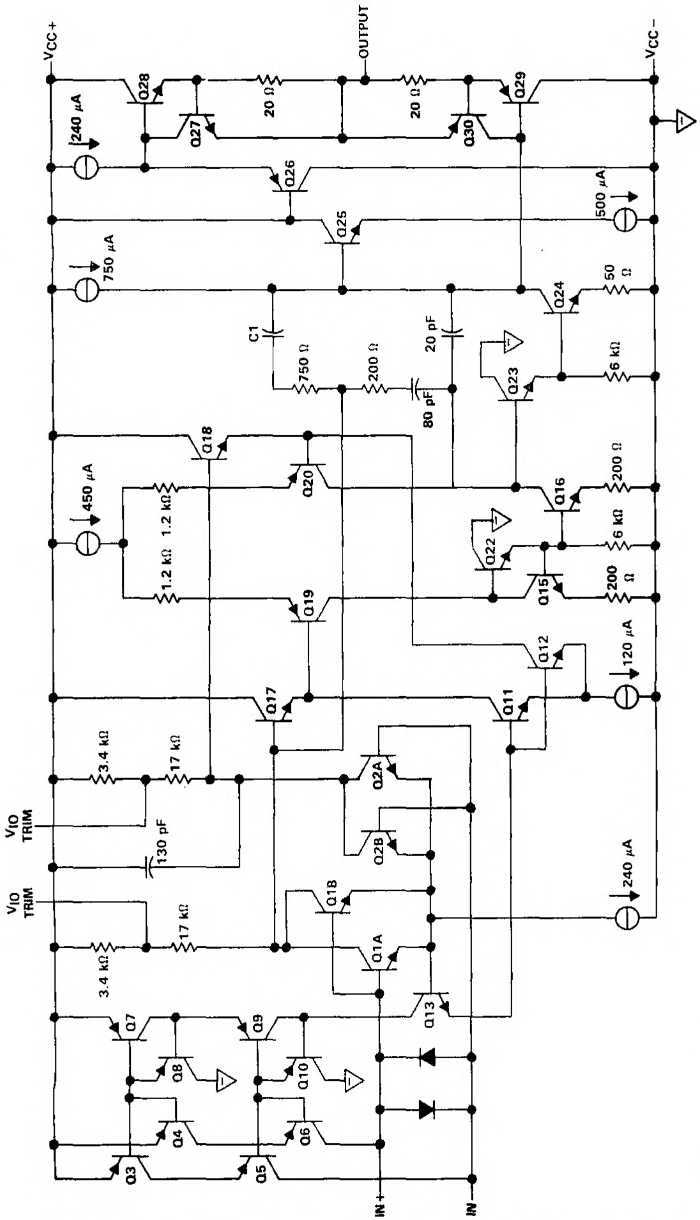
In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest-cost grades (the LT1007C and the LT1037C) have been greatly improved compared to equivalent grades of competing amplifiers.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE [illegible]	CERAMIC DIP [illegible]	METAL CAN [illegible]	PLASTIC DIP (P)
0°C to 70°C	60 μV	[illegible]	[illegible]	[illegible]	[illegible]
	25 μV	—	[illegible]	[illegible]	[illegible]
	60 μV	LT1037CDW	[illegible]	[illegible]	[illegible]
	25 μV	—	[illegible]	[illegible]	LT1037ACP
−55°C to 125°C	60 μV	—	[illegible]	[illegible]	[illegible]
	25 μV	—	[illegible]	[illegible]	[illegible]
	60 μV	—	LT1037MJG	LT1037ML	LT1037MP
	25 μV	—	LT1037AMJG	LT1037AML	LT1037AMP

The DW packages are available taped and reeled. Add the suffix "R" to the device type. (e.g., LT1007CDWR).

schematic



C1 = 110 pF for LT1007
C1 = 12 pF for LT1037
All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 22 V
Supply voltage, V_{CC-} . . . . −22 V
Input voltage . . . . $V_{CC\pm}$
Duration of output short-circuit . . . . Unlimited
Differential input current (see Note 2) . . . . ±25 mA
Power dissipation . . . . see Dissipation Rating Table
Operating free-air temperature range:
  LT1007M, LT1007AM, LT1037M, LT1037AM . . . . −55°C to 125°C
  LT1007C, LT1007AC, LT1037C, LT1037AC . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW and P packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG and L packages . . . . . . 300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs, unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	[illegible] mW	8.2 mW/°C	[illegible] mW	N/A	N/A
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	338 mW	N/A
P	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		LT1007M, LT1037M			LT1007C, LT1037C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	[illegible]	4	15	[illegible]	V
Supply voltage, V_{CC-}		−4	−15	[illegible]	−4	−15	−22	V
Input voltage, V_I	$T_A = 25°C$	±11			±11			V
	T_A = full range	±10.3			±10.5			V
Operating free-air temperatue, T_A		−55		125	0		70	°C

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

	PARAMETER	TEST CONDITIONS	T_A	LT1007, LT1037			LT1007A, LT1037A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	60		10	25	μV
			−55°C to 125°C			160			60	
αV_{IO}	Average temperature coefficient of input offset voltage		−55°C to 125°C			1			0.6	μV/°C
I_{IO}	Input offset current		25°C		12	50		7	30	nA
			−55°C to 125°C			85			50	
I_{IB}	Input bias current		25°C		±15	±55		±10	±35	nA
			−55°C to 125°C			±95			±60	
V_{OM}	Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
		R_L = [illegible] Ω	25°C	±10.5	±12.5		±11	±12.5		
		R_L = 2 kΩ	−55°C to 125°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/μV
		R_L ≥ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
		R_L ≥ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
		R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	2			3			
		R_L ≥ 1 kΩ, V_O = ±10 V	−55°C to 125°C	1.5			2			
$r_{i(CM)}$	Common-mode input resistance		25°C		5			7		GΩ
r_o	Open-loop output resistance		25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	[illegible]		117	[illegible]		dB
		V_{IC} = ±10.3 V	−55°C to 125°C	104			112			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	106	126		110	130		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	−55°C to 125°C	100			104			
P_D	Power dissipation	LT1007M, LT1007AM	25°C		80	140		80	120	mW
		LT1037M, LT1037AM	25°C		85	140		80	[illegible]	
			−55°C to 125°C			170			150	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

TEXAS INSTRUMENTS
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electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS	T_A	LT1007, LT1037 MIN	LT1007, LT1037 TYP	LT1007, LT1037 MAX	LT1007A, LT1037A MIN	LT1007A, LT1037A TYP	LT1007A, LT1037A MAX	UNIT
V_{IO}	Input offset voltage	See Note 3	25°C		20	60		10	25	μV
			0°C to 70°C			110			50	
αV_{IO}	Average temperature coefficient of input offset voltage		0°C to 70°C			1			0.6	μV/°C
I_{IO}	Input offset current		25°C		12	50		7	30	nA
			0°C to 70°C			70			40	
I_{IB}	Input bias current		25°C		±15	±55		±10	±35	[illegible]
			0°C to 70°C			±75			±45	
V_{OM}	Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
		R_L = 600 Ω	25°C	±10.5	±12.5		±11	±12.5		
		R_L = 2 kΩ	0°C to 70°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/μV
		R_L ≥ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
		R_L ≥ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
		R_L ≥ 2 kΩ, V_O = ±10 V	0°C to 70°C	2.5			4			
		R_L ≥ 1 kΩ, V_O = ±10 V	0°C to 70°C	2			2.5			
$r_{i(CM)}$	Common-mode input resistance		25°C		5			7		GΩ
r_o	Open-loop output resistance		25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		117	130		dB
		V_{IC} = ±10.5 V	0°C to 70°C	106			114			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	[illegible]	126		110	130		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	0°C to 70°C	102			106			
P_D	Power dissipation	LT[illegible], LT[illegible]AM	25°C		80	140		80	[illegible]	mW
		LT[illegible], LT[illegible]AM	25°C		85	140		80	[illegible]	
			0°C to 70°C			160			144	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

operating characteristics $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LT1007/LT1007A			LT1037/LT1037A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$R_L \geq 2$ kΩ, $A_{VD} \geq 1$ (LT1007, LT1007A)	1.7	2.5					V/μs
		$R_L \geq 2$ kΩ, $A_{VD} \geq 5$ (LT1037, LT1037A)				11	15		
V_{NPP}	Peak-to-peak equivalent input noise voltage	0.1 Hz to 10 Hz, See Note 4		0.06	0.13		0.06	0.13	μV
V_n	Equivalent input noise noise voltage	10 Hz		2.8	4.5		2.8	4.5	nV/√Hz
		1 kHz		2.5	3.8		2.5	3.8	
I_n	Equivalent input noise current	10 Hz, See Note 5		1.5	4		1.5	4	pA/√Hz
		1 kHz, See Note 5		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	100 kHz	5	8					MHz
		10 kHz, $A_V \geq 15$				45	60		

NOTES: 4. See the test circuit and frequency response curve for 0.1 Hz to 10 Hz noise (Figure 39) in the Applications Information section.
5. See the test circuit for current noise measurement (Figure 40) in the Applications Information section.

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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power on	2
		vs Time (long-term stability)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
		over common-mode range	6
	Common-mode limit voltage	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage swing	vs Load resistance	8
		vs Frequency	9
A_{VD}	Differential voltage amplification	vs Frequency	10
		vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
		vs Temperature	13
		vs Load resistance	14
		vs Supply voltage	15
		at 2 kΩ and 600 Ω	16
V_{ID}	Differential input voltage	vs Output voltage	16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply voltage rejection ratio	vs Frequency	18
SR	Slew rate	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
ϕ	Phase shift	vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
ϕ_m	Phase margin	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
V_n	Equivalent input noise voltage	vs Free-air temperature	21
		vs Time (0.01-Hz to 1-Hz noise)	22
		vs Frequency	23
		vs Bandwidth	24
		vs Supply voltage	25
I_n	Equivalent input noise current	vs Frequency	26
	Total noise	vs Source resistance	27
GBW	Gain bandwidth product	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
I_{OS}	Short-circuit output current	vs Time (from short to [illegible]	28
I_{CC}	Supply current	vs Supply voltage	29
z_o	Closed-loop output impedance	vs Frequency	30
	Pulse response (LT1007)	Small-signal (C_{load} = 15 pF)	31
		Large-signal	32
	Pulse response (LT1037)	Small-signal (C_{load} = 15 pF)	33
		Large-signal	34

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

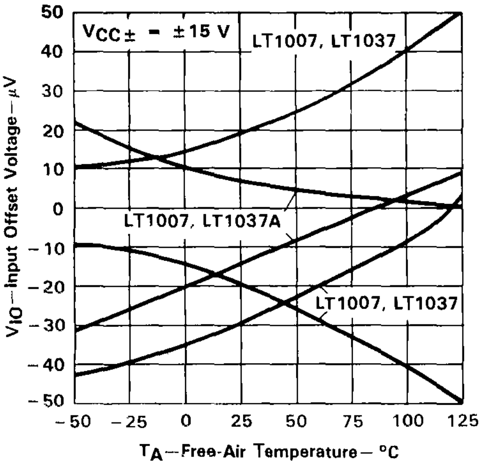


FIGURE 1

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

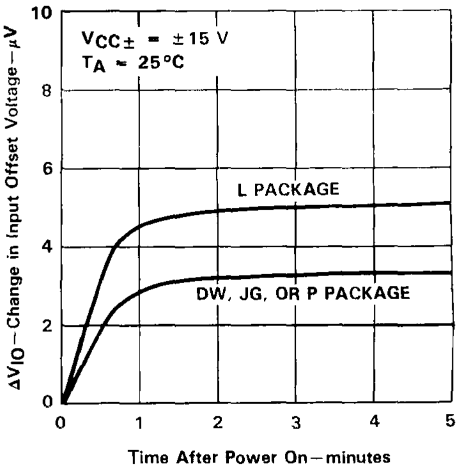


FIGURE 2

LONG TERM STABILITY OF
INPUT OFFSET VOLTAGE
FOR FOUR REPRESENTATIVE UNITS

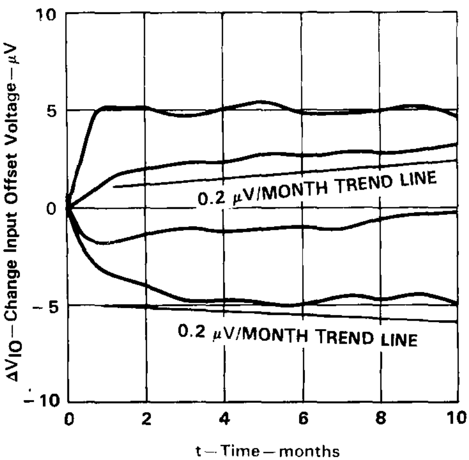


FIGURE 3

INPUT OFFSET CURRENT
vs
TEMPERATURE

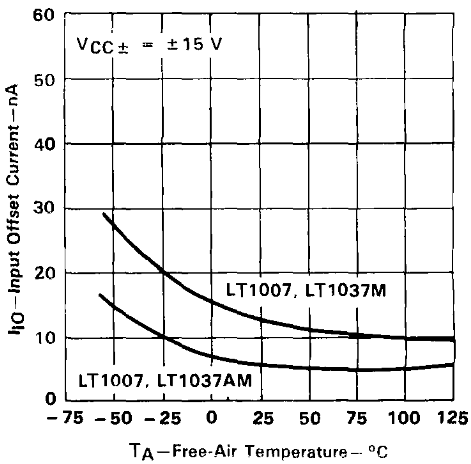


FIGURE 4

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

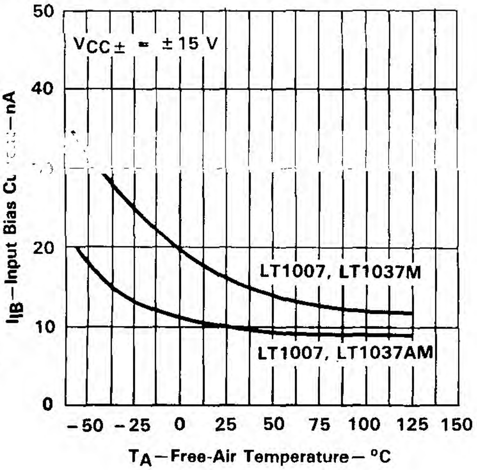


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

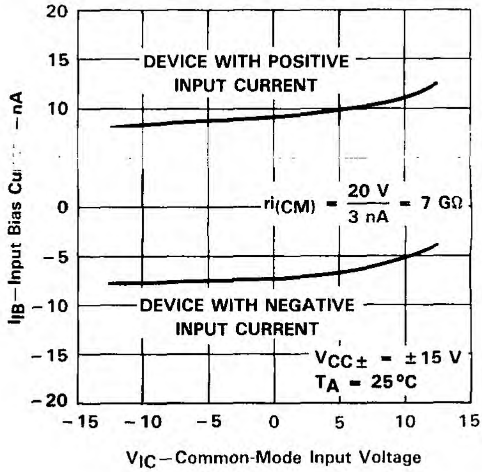


FIGURE 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

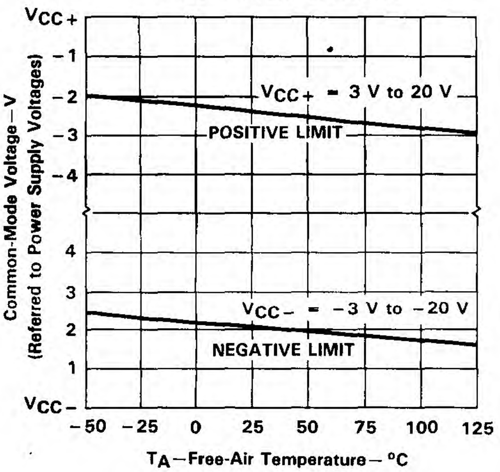


FIGURE 7

PEAK OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

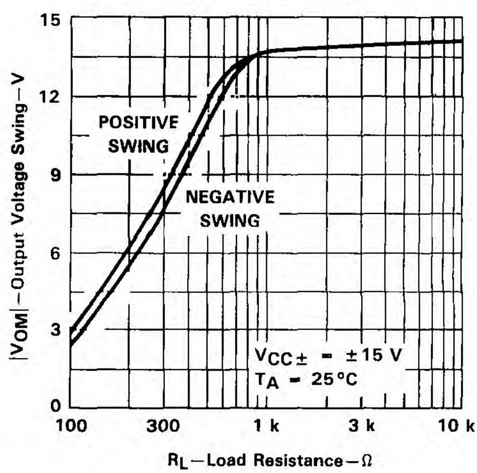


FIGURE 8

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

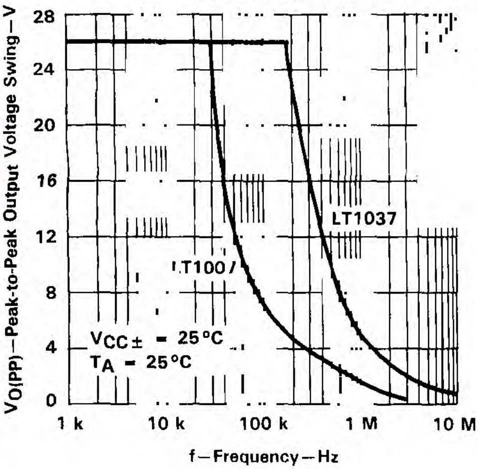


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

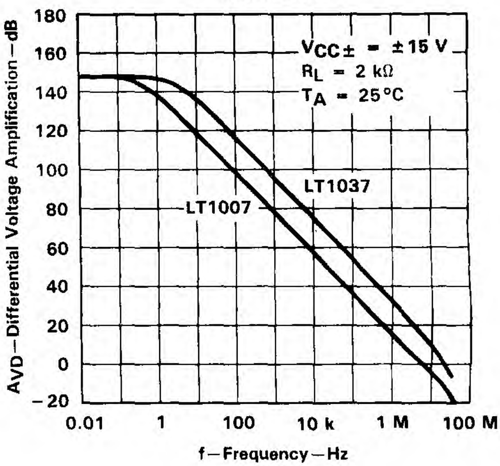


FIGURE 10

LT1007
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

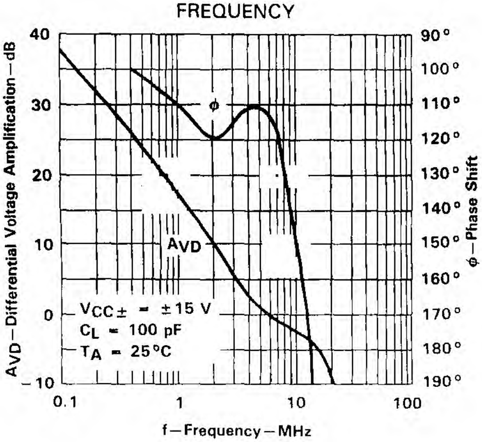


FIGURE 11

LT1037
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

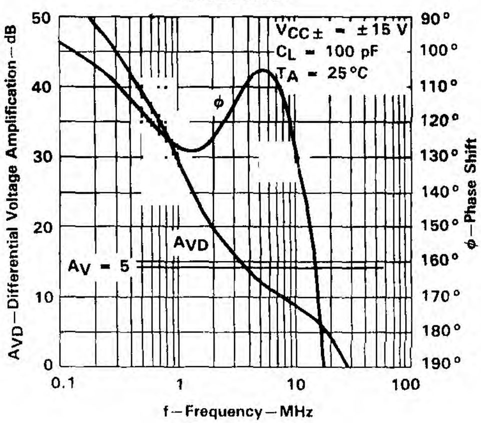


FIGURE 12

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

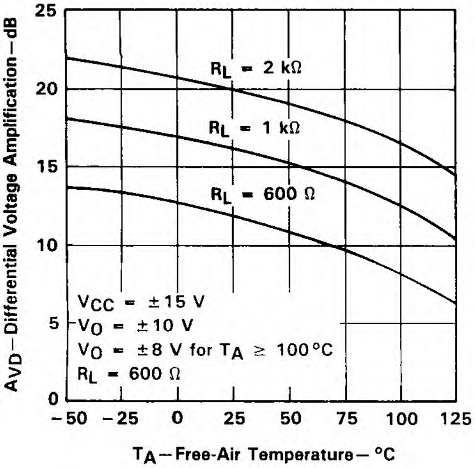


FIGURE 13

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

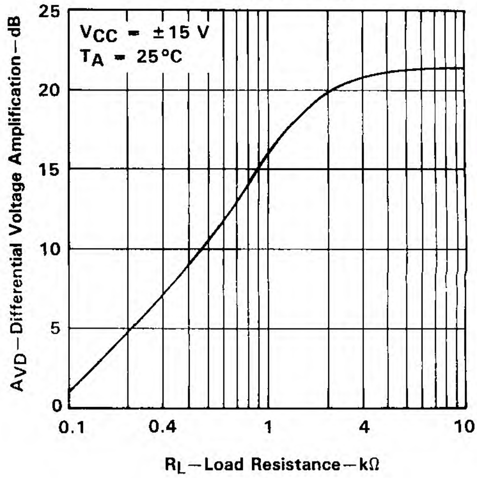


FIGURE 14

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

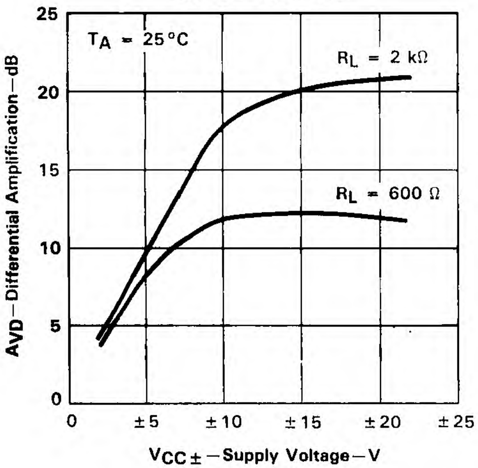


FIGURE 15

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

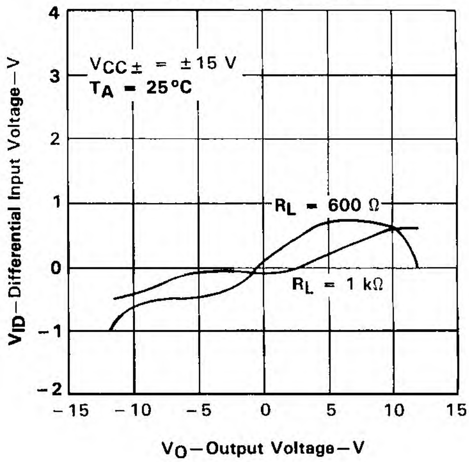


FIGURE 16

2

Operational Amplifiers

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

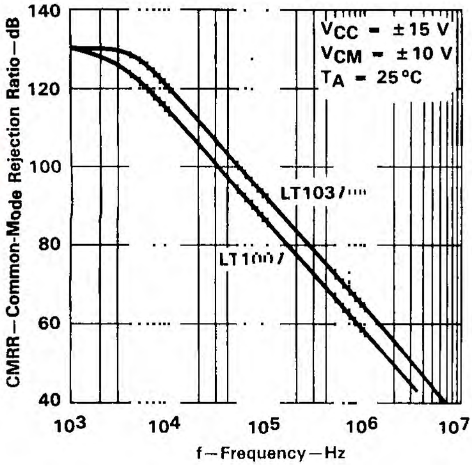


FIGURE 17

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

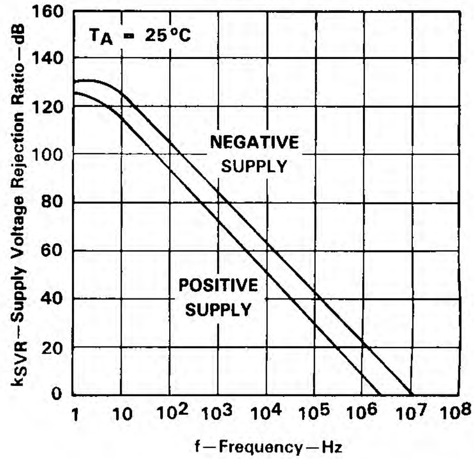


FIGURE 18

LT1007
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

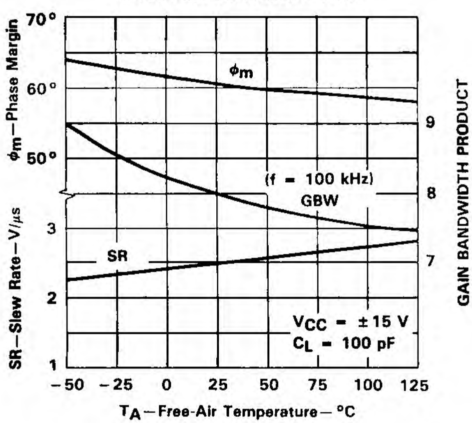


FIGURE 19

LT1037
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

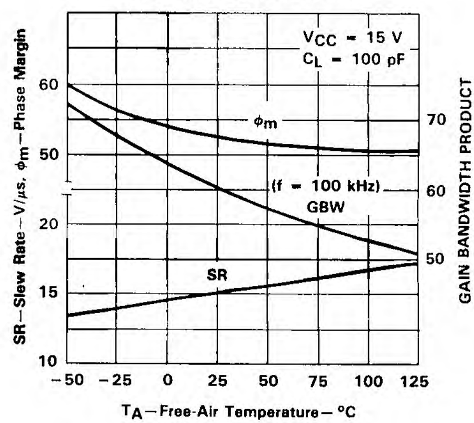


FIGURE 20

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREE-AIR TEMPERATURE

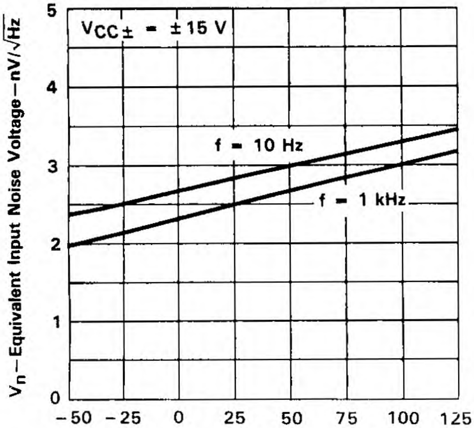


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 100-SECOND TIME PERIOD

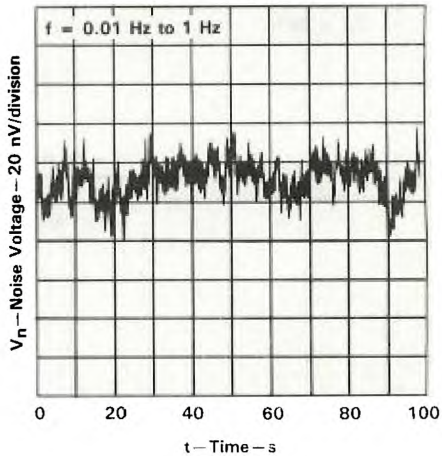


FIGURE 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

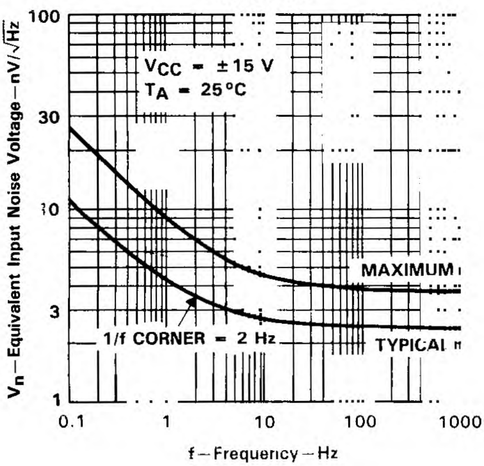


FIGURE 23

BROADBAND NOISE VOLTAGE
0.1 Hz TO INDICATED FREQUENCY

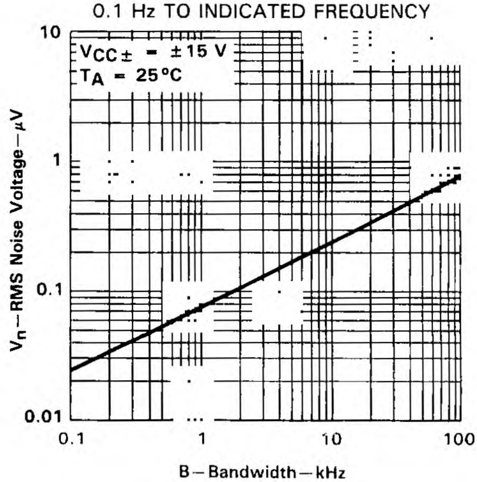


FIGURE 24

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SUPPLY VOLTAGE

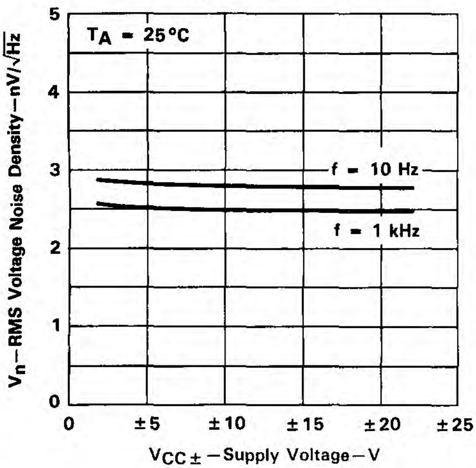


FIGURE 25

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

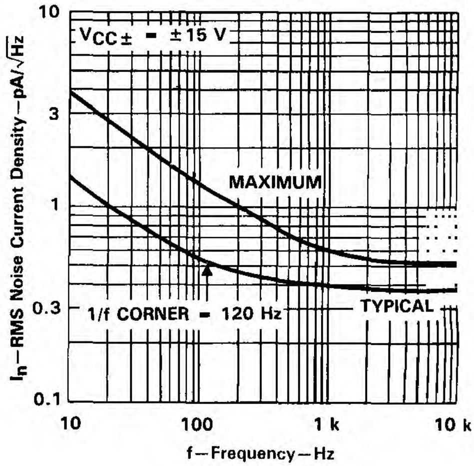


FIGURE 26

TOTAL NOISE VOLTAGE
vs
SOURCE RESISTANCE

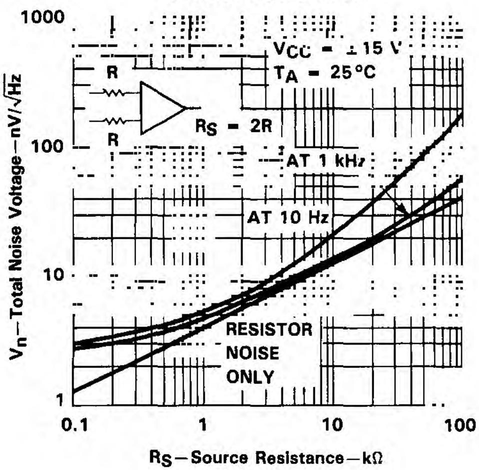


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

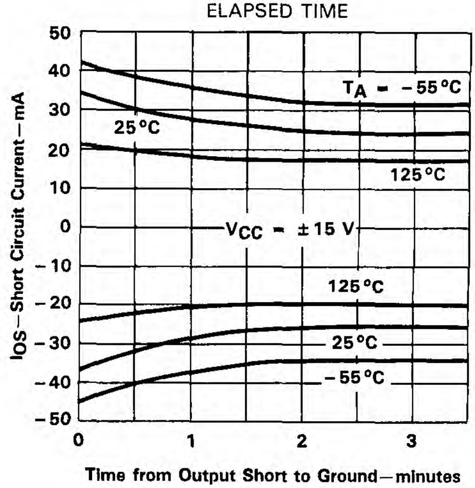


FIGURE 28

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

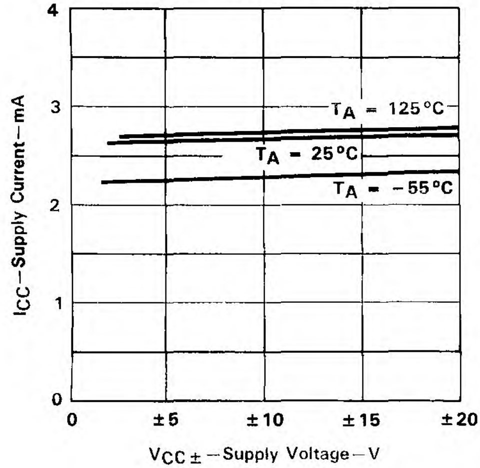


FIGURE 29

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

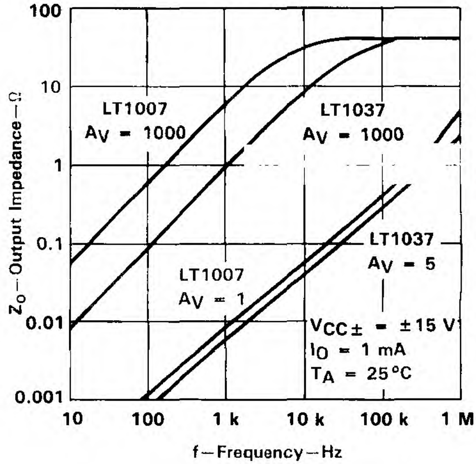


FIGURE 30

LT1037
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

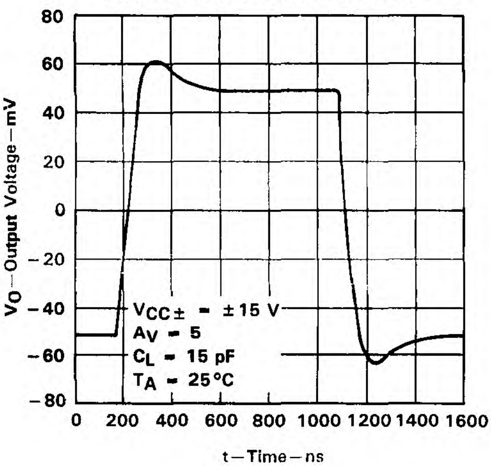


FIGURE 31

LT1037
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

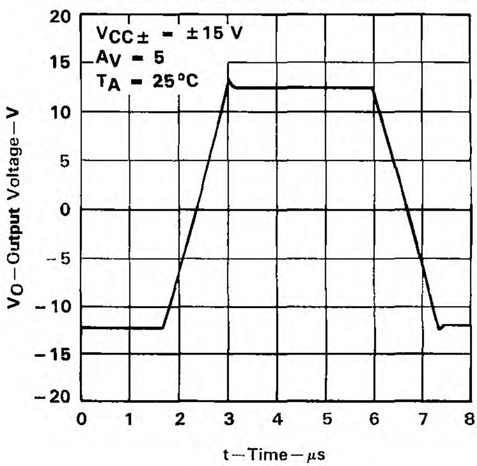


FIGURE 32

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

2

Operational Amplifiers

TYPICAL CHARACTERISTICS

LT1007
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

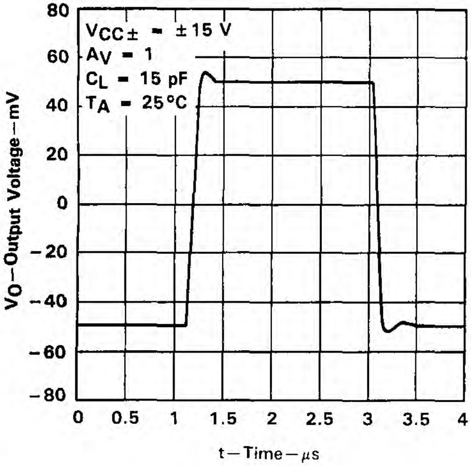


FIGURE 33

LT1007
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

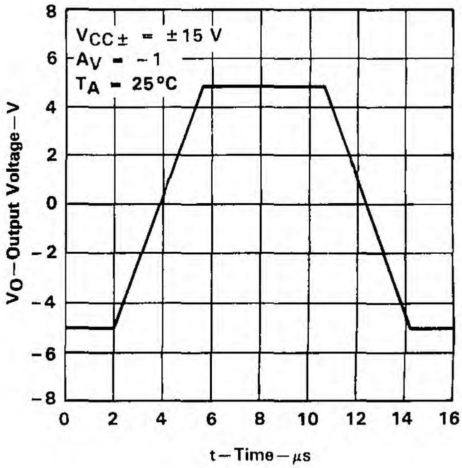


FIGURE 34

TYPICAL APPLICATION DATA

general

The LT1007- and LT1037-series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external-compensation or nulling components. In addition, the LT1007 and LT1037 may be fitted to μA741 sockets by removing or modifying external nulling components.

offset voltage adjustment

The input offset voltage and its change with temperature of the LT1007 and LT1037 are permanently trimmed to a low level at wafer testing . However, if further adjustment of V_{IO} is necessary, the use of a 10-kΩ nulling potentiometer, as shown in Figure 35, will not degrade drift with temperature. Trimming to a value other than zero creates a drift of V_{IO}/300 μV/°C (e.g., if V_{IO} is adjusted to 300 μV, the change in temperature coefficient will be 1 μV/°C).

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 36 has an approximate null range of ±200 μV.

offset voltage and drift

Unless proper care is exercised, thermocouple effects at the contacts to the input terminals, caused by temperature gradients across dissimilar metals, can exceed the inherent temperature coefficient of the amplifier. Air currents should be minimized, package leads should be short, input leads should be close together, and input leads should be at the same temperature.

TYPICAL APPLICATION DATA

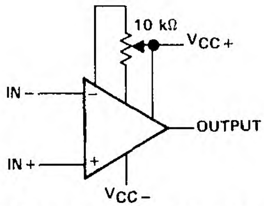


FIGURE 35. STANDARD ADJUSTMENT

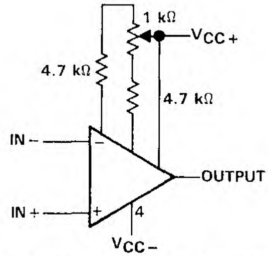


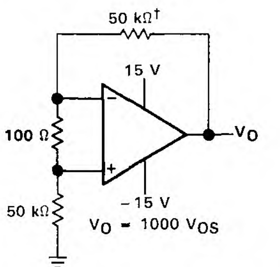
FIGURE 36. IMPROVED SENSITIVITY ADJUSTMENT

The circuit shown in Figure 37 can be used to measure offset voltage. In addition, with the supply voltages increased to ±20 V, it can be used as the burn-in configuration for the LT1007 and LT1037.

When $R_F \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (>1 V), the output waveform will be as shown in Figure 38.

During the fast-feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When R_F is $\geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs.

When R_F is >2 kΩ, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_F will eliminate this problem.



†Resistors must have low thermoelectric potential

FIGURE 37. TEST CIRCUIT FOR OFFSET VOLTAGE AND OFFSET VOLTAGE DRIFT WITH TEMPERATURE

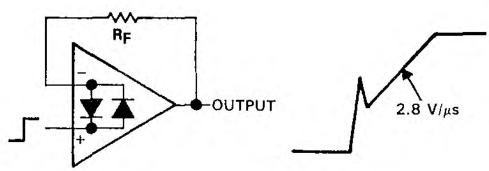


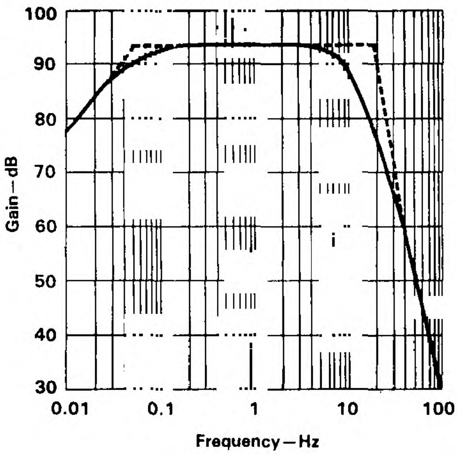
FIGURE 38. PULSE OPERATION

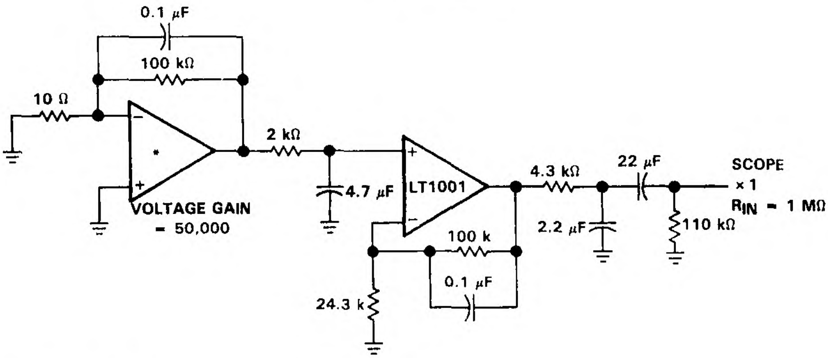
TYPICAL APPLICATION DATA

noise testing

Figure 39 shows a test circuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the LT1007 and LT1037. The frequency response of this noise tester indicates that the 0.1 Hz corner is defined by only one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.

0.1 Hz to 10 Hz p-p NOISE TESTER
FREQUENCY RESPONSE





*Device under test
NOTE: All capacitor values are for non-polarized capacitors only.

FIGURE 39. 0.1-Hz TO 10-Hz NOISE TEST CIRCUIT

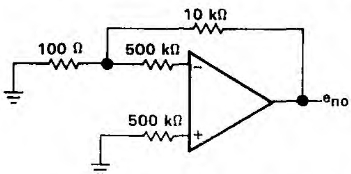
TYPICAL APPLICATION DATA

Special test precautions are required to measure the typical 60-nV peak-to-peak noise performance of the LT1007 and LT1037:

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 3 μV, due to the chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10-second measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. The device must be well shielded from air currents to eliminate thermoelectric effects. In excess of a few nanovolts, thermoelectric effects would invalidate the measurements.
3. Sudden motion in the vicinity of the device can produce a feedthrough effect that increases observed noise.

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement will correlate well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 40 shows a circuit that measures noise current and presents the formula for calculating noise current.



$$i_n = \frac{[v_n^2 - (130\ \text{nV})^2]^{1/2}}{1\ \text{M}\Omega \times 100}$$

FIGURE 40. NOISE TEST CIRCUIT

The LT1007 and LT1037 achieve low noise, in part, by operating the input stage at 120 μA versus the typical 10 μA for most other operational amplifiers. Voltage noise is directly proportional to the square root of the stage current; therefore, the LT1007 and LT1037 noise current is relatively high. At low frequencies, the low 1/f current-noise corner frequency (≈ 120 Hz) minimizes noise current to some extent.

In most practical applications, however, noise current will not limit system performance; this is illustrated in Figure 27, where:

$$\text{total noise} = [(\text{noise voltage})^2\ (\text{noise current} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$$

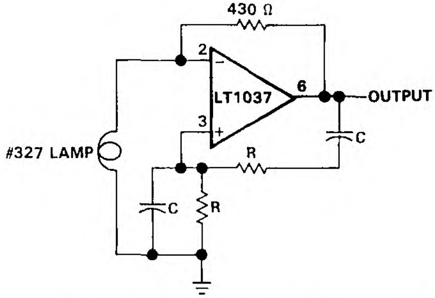
Three regions can be identified as a function of source resistance:

(i)	$R_S \leq 400\ \Omega$	Voltage noise dominates in region (i)
(ii)	$R_S = 400\ \Omega$ to 50 kΩ at 1 kHz	Resistor noise dominates in region (ii)
	$R_S = 400\ \Omega$ to 8 kΩ at 10 Hz	
(iii)	$R_S > 50$ kΩ at 1 kHz	Current noise dominates in region (iii)
	$R_S > 8$ kΩ at 10 Hz	

The LT1007 and LT1037 should not be used in region (iii) where total system noise is at least six times higher than the noise voltage of the operational amplifier (i.e., the low-voltage noise specification is completely wasted).

TYPICAL APPLICATIONS

The sine wave generator application shown below, utilizes the low-noise and low-distortion characteristics of the LT1037.



$f = \frac{1}{2\pi RC}$
R = 1591.5Ω ±0.1%
C = 0.1 μF ±0.1%

TOTAL HARMONIC DISTORTION ≤ 0.0025%
NOISE ≤ 0.001%
AMPLITUDE = ±8 V
OUTPUT FREQUENCY = 1.000 kHz FOR VALUES GIVEN ± 0.4%

FIGURE 41. ULTRA-PURE 1-kHz SINE-WAVE GENERATOR

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

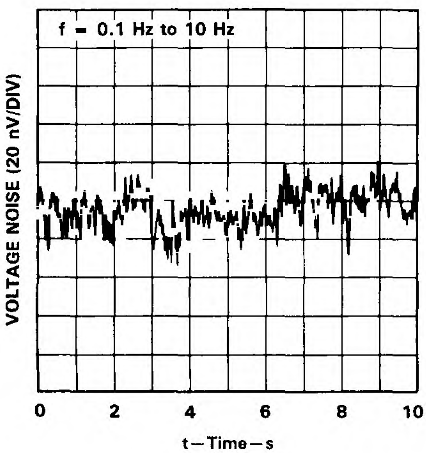
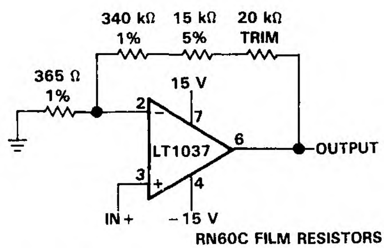


FIGURE 42



The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low-frequency high-closed-loop-gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500 kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3 Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision—bandwidth product" is 200 times higher, as shown.

FIGURE 43. GAIN 1000 AMPLIFIER WITH 0.01% ACCURACY, DC to 5 Hz

TYPICAL APPLICATIONS

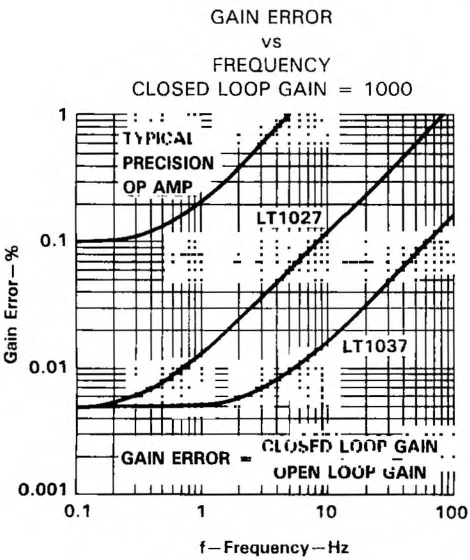
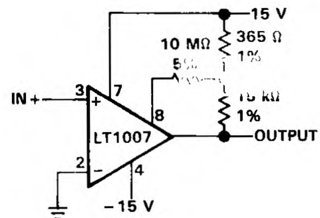


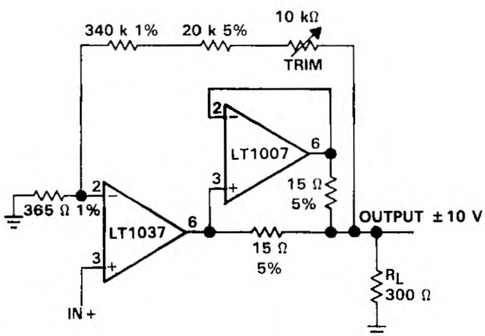
FIGURE 44



Positive feedback to one of the nulling terminals creates approximately 5 μV of hysteresis. Output can sink 16 mA.

Input offset voltage is typically changed less than 5 μV due to the feedback.

FIGURE 45. MICROVOLT COMPARATOR WITH HYSTERESIS



The addition of the LT1007 doubles the amplifier's output drive to ±33 mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

FIGURE 46. PRECISION AMPLIFIER DRIVES 300-Ω LOAD TO ±10 V

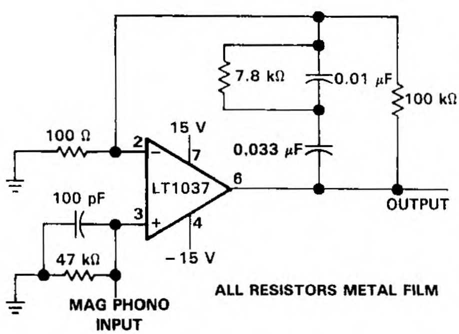


FIGURE 47. PHONO PREAMPLIFIER

TYPICAL APPLICATIONS

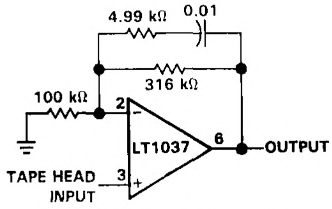


FIGURE 48. TAPE HEAD AMPLIFIER

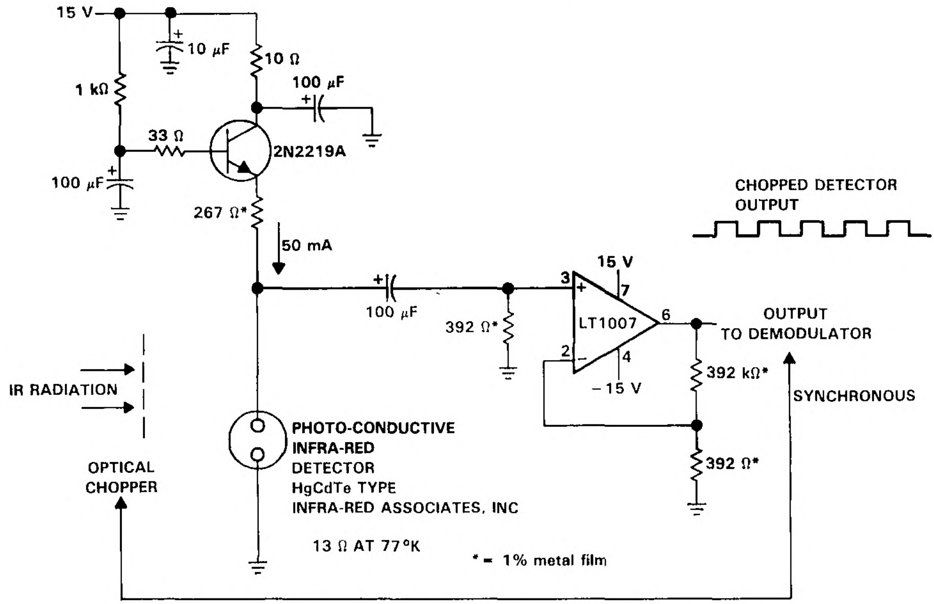
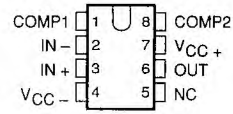


FIGURE 49. INFRA-RED DETECTOR PREAMPLIFIER

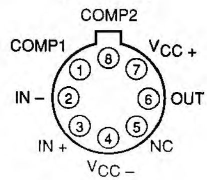
D3233, MAY 1988 – REVISED FEBRUARY 1989

- **Input Bias Current . . . ± 30 pA Typ, ± 100 pA Max at 25°C**
- **Input Offset Voltage . . . 30 µV Typ, 120 µV Max at 25°C**
- **Offset Voltage Temperature Coefficient . . . 1.5 µV/°C Max**
- **Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 0.5 µV**
- **Low Supply Current . . . 380 µA Typ, 600 µA Max at 25°C**
- **Supply Voltage Rejection Ratio . . . 114 dB Min at 25°C**
- **Common-Mode Rejection Ratio . . . 114 dB Min at 25°C**
- **High Voltage Amplification with 5-mA Load Current**
- **Applications:**
  - **Precision Instrumentation**
  - **Charge Integrators**
  - **Wide-Dynamic-Range Logarithmic Amplifiers**
  - **Light Meters**
  - **Low-Frequency Active Filters**
  - **Standard Cell Buffers**
  - **Thermocouple Amplifiers**

JG OR P PACKAGE
(TOP VIEW)

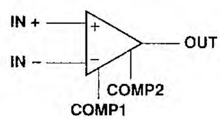


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L Package) is in electrical contact with the case.

symbol



description

The LT1008 is a precision operational amplifier that can be used in practically all precision applications. The LT1008 offers picoampere bias currents (maintained over the full temperature range), microvolt offset voltage, low offset voltage temperature coefficient and long-term drift, low voltage and current noise, and low power dissipation. Additionally, the LT1008's precision specifications include high common-mode and supply voltage rejection ratios. The LT1008 can deliver a 5-mA load current with high voltage amplification.

The LT1008 is externally compensated with a single capacitor to add flexibility in shaping the frequency response of the amplifier. The LT1008 is a pin-for-pin replacement for the LM108 series.

The LT1008M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1008C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	LT1008CJG	LT1008CL	LT1008CP
−55°C to 125°C	LT1008MJG	LT1008ML	LT1008MP

TEXAS INSTRUMENTS
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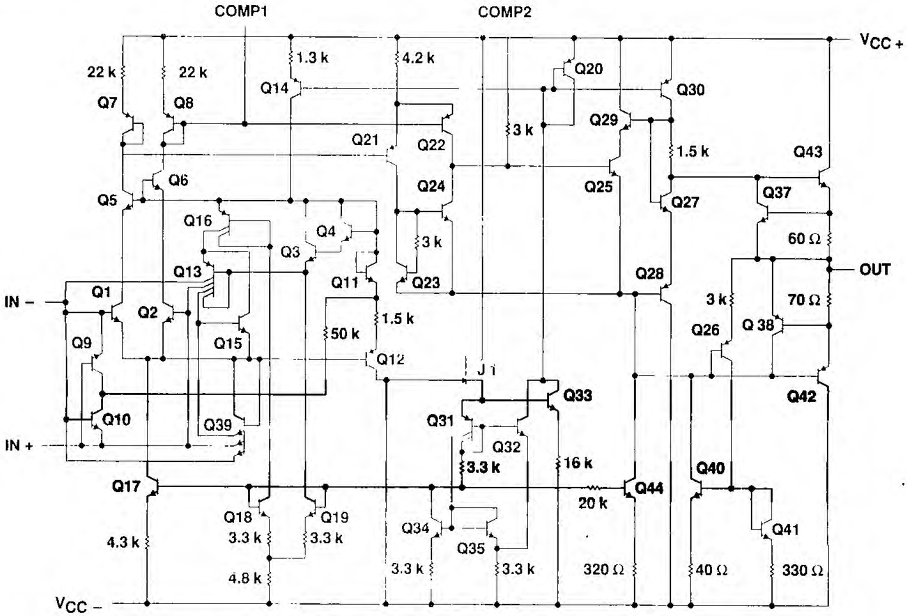
schematic



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) .... 20 V
Supply voltage, V_{CC-} .... − 20 V
Input voltage range, V_I .... ± 20 V
Differential input current (see Note 2) .... ± 10 mA
Duration of output short-circuit at (or below) 25°C (see Note 3) .... unlimited
Operating free-air temperature, T_A: LT1008M .... − 55°C to 125°C
LT1008C .... 0°C to 70°C
Storage temperature range .... − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package .... 260°C

NOTES: 1. All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages greater than 1 V will cause excessive current to flow through the input protection diodes unless current-limiting resistors are used.
3 The output may be shorted to either supply

recommended operating conditions

		LT1008M			LT1008C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}				± 20			± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 15 V			± 13.5	− 15		± 13.5	V
Operating free-air temperature, T_A		− 55		125	0		70	°C

electrical characteristics, $V_{CC\pm}$ = ± 15V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1008M MIN	LT1008M TYP	LT1008M MAX	LT1008C MIN	LT1008C TYP	LT1008C MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ± 15 V, V_{IC} = 0	25°C		30	120		30	120	µV
			Full range			250			180	
		$V_{CC\pm}$ = ± 15 V, V_{IC} = ±13.5 V	25°C		40	180		40	180	
			Full range			[illegible]			[illegible]	
		$V_{CC\pm}$ = ± 2 V to ± 20 V	25°C		40	180		40	[illegible]	
		$V_{CC\pm}$ = ± 2.5 V to ± 20 V	Full range			320			250	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		0.2	1.5		0.2	1.5	µV/°C
	Long-term drift of input offset voltage		25°C		0.3			0.3		µV/mo
I_{IO}	Input offset current	$V_{CC\pm}$ = ± 15 V, V_{IC} = 0	25°C		30	100		30	100	pA
			Full range			250			180	
		$V_{CC\pm}$ = ± 15 V, V_{IC} = ±13.5 V	[illegible]		40	150		40	150	
			Full range						250	
		$V_{CC\pm}$ = ± 2 V to ± 20 V	25°C		40	150		40	150	
		$V_{CC\pm}$ = ± 2.5 V to ± 20 V	Full range			350			250	
α_{IIO}	Average temperature coefficient of input offset current		Full range		0.4	2.5		0.4	2.5	pA/°C
I_{IB}	Input bias current	$V_{CC\pm}$ = ± 15 V, V_{IC} = 0	25°C		± 30	± 100		± 30	± 100	pA
			Full range			± 600			± 180	
		$V_{CC\pm}$ = ± 15 V, V_{IC} = ±13.5 V	25°C		± 40	± 150		± 40	± 150	
			Full range			± 800			± 250	
		$V_{CC\pm}$ = ± 2 V to ± 20 V	25°C		± 40	± 150		± 40	± [illegible]	
		$V_{CC\pm}$ = ± 2.5 V to ± 20 V	Full range			± 800			± 250	
α_{IIB}	Average temperature coefficient of input bias current		Full range		0.6	6		0.4	2.5	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	± 13.5	± 14		± 13.5	± 14		V
			Full range	± 13.5			± 13.5			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	± 13	± 14		± 13	± 14		V
			Full range	± 13			± 13			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 12 V, R_L ≥ 10 kΩ	25°C	200	2000		200	2000		V/mV
			Full range	100			150			
		V_O = ± 10 V, R_L ≥ 2 kΩ	25°C	120	600		120	[illegible]		
CMRR	Common-mode rejection ratio	V_{IC} = ±13.5 V	25°C	114	132		114	132		dB
			Full range	108			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2 V to ± 20 V	25°C	114	132		114	132		dB
		$V_{CC\pm}$ = ± 2.5 V to ± 20 V	Full range	[illegible]			110			
I_{CC}	Supply current	$V_{CC\pm}$ = ± 15 V, V_{IC} = ±13.5 V	25°C		380	600		380	600	µA
		$V_{CC\pm}$ = ± 2 V to ± 20 V	25°C		380	600		380	600	
		$V_{CC\pm}$ = ± 15 V, V_{IC} = 0	Full range			800			800	

†Full range is –55°C to 125°C for the LT1008M and 0°C to 70°C for the LT1008C.

2 Operational Amplifiers

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	C_f = 30 pF, See Figure 29(a)	0.1	0.2		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.5		μV
V_n	Equivalent input noise voltage	f = 10 Hz		17	30	nV/√Hz
		f = 1 kHz		14	22	
I_n	Equivalent input noise current	f = 10 Hz		20		fA/√Hz

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
		vs Source resistance	5
ΔV_{IO}	Change in input offset voltage	vs Time – minutes	2
		vs Time – months	3
α_{VIO}	Temperature coefficient of input offset voltage	vs Source resistance	6
I_{IB}	Input bias current	vs Common-mode input voltage	7
		vs Temperature	8
A_{VD}	Differential voltage amplification	vs Load resistance	9
		vs Frequency	10, 11, 12
CMRR	Common-mode rejection ratio	vs Frequency	13
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	14
I_{OS}	Short-circuit output current	vs Time	15
I_{CC}	Supply current	vs Supply voltage	4
SR	Slew rate	vs Compensation capacitance	16
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Time	17
V_n, I_n	Equivalent input noise voltage and equivalent input noise current	vs Frequency	18
	Total equivalent input noise voltage	vs Source resistance	19
	Phase shift	vs Frequency	11, 12
	Pulse response	Small-signal	20, 21, 22
		Large-signal	23, 24

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

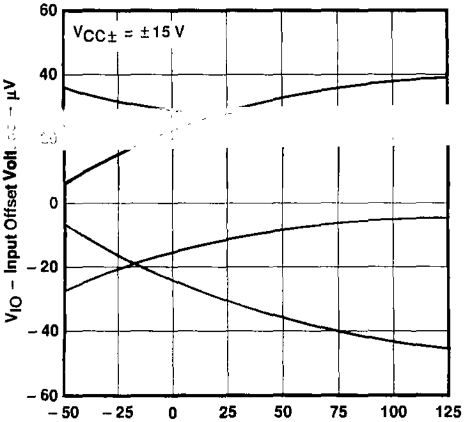


FIGURE 1

WARM-UP CHANGE IN
INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

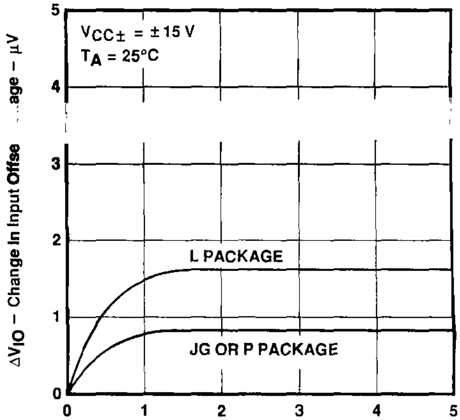


FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

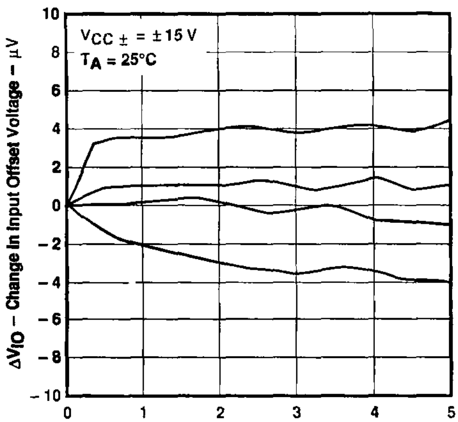


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

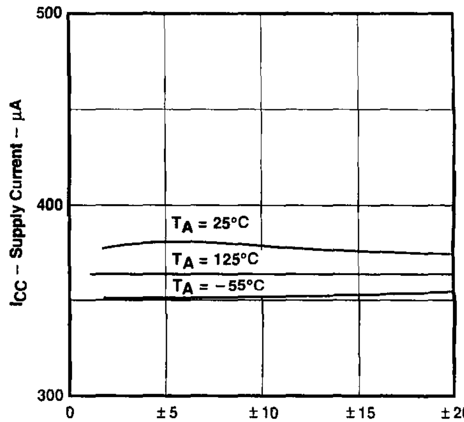


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

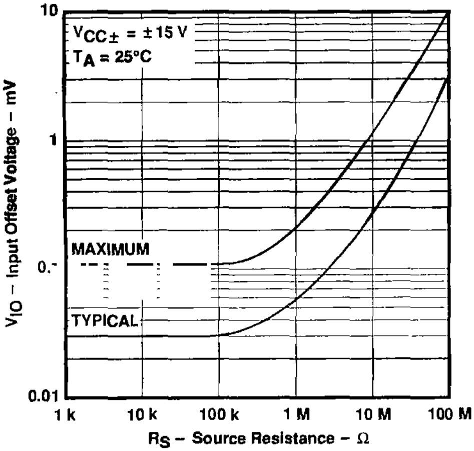


FIGURE 5

AVERAGE TEMPERATURE COEFFICIENT
OF INPUT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

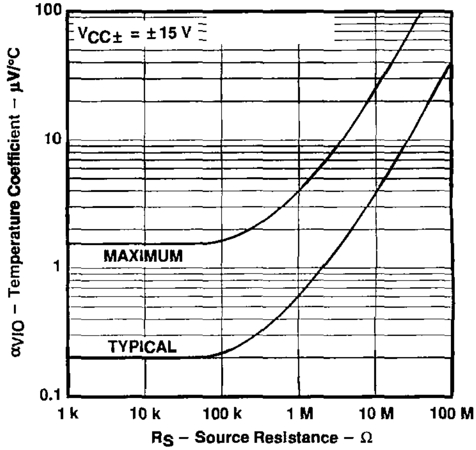


FIGURE 6

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

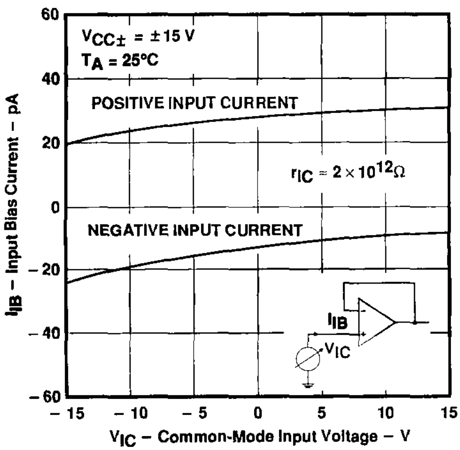


FIGURE 7

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

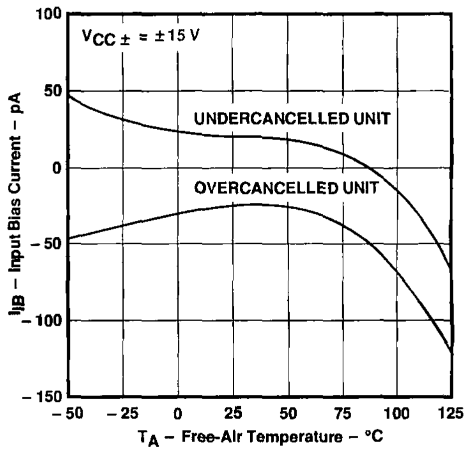


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

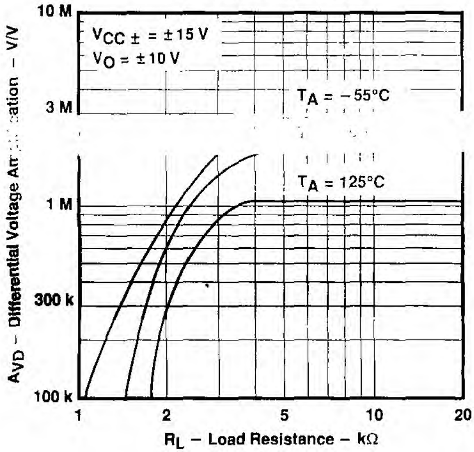


FIGURE 9

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

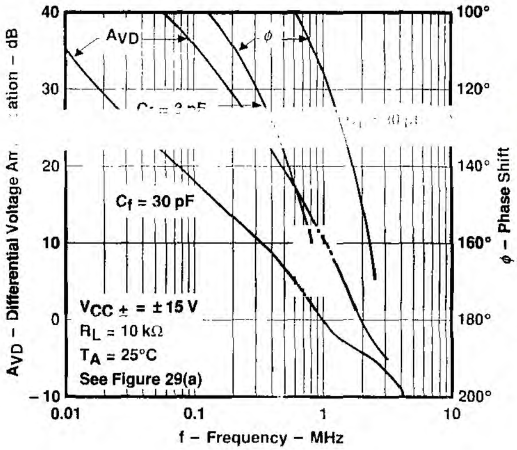


FIGURE 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

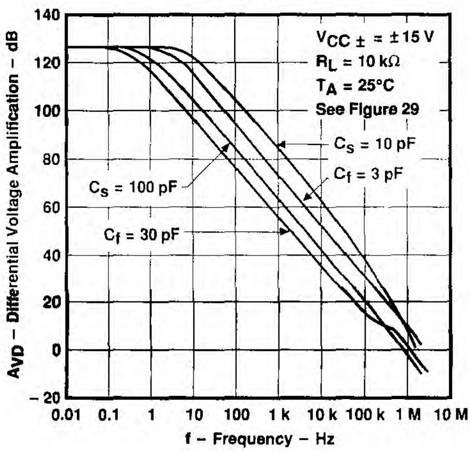


FIGURE 11

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

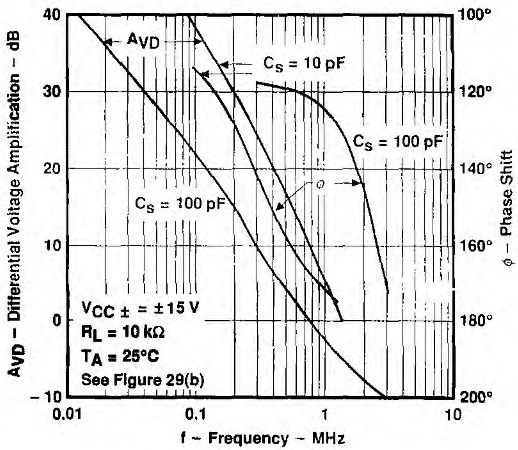


FIGURE 12

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

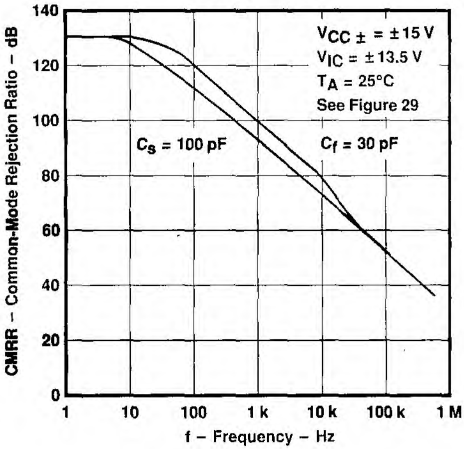


FIGURE 13

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

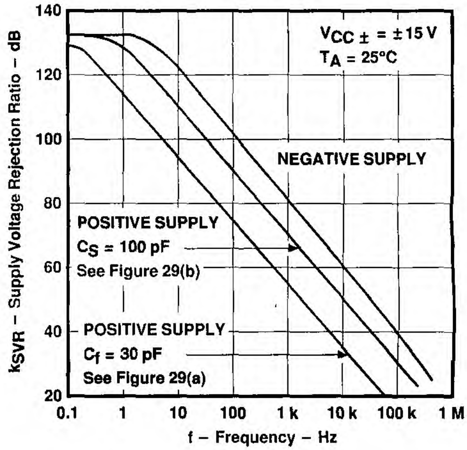


FIGURE 14

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

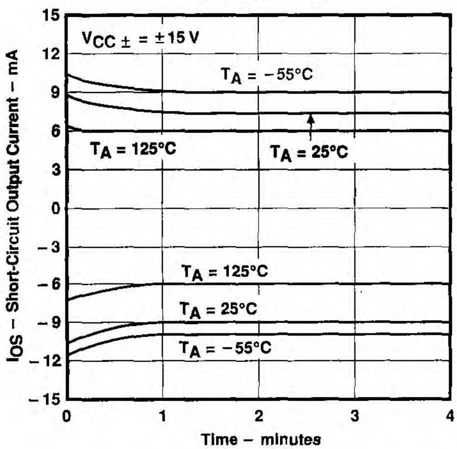


FIGURE 15

SLEW RATE
vs
COMPENSATION CAPACITANCE

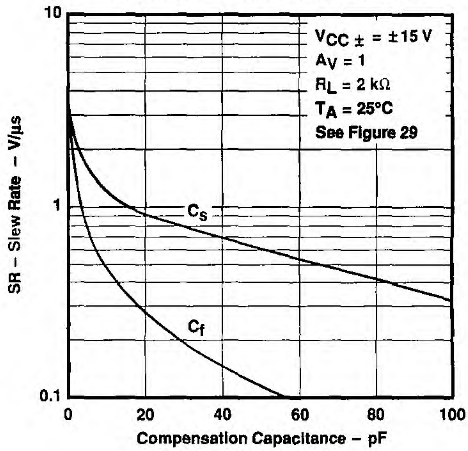


FIGURE 16

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

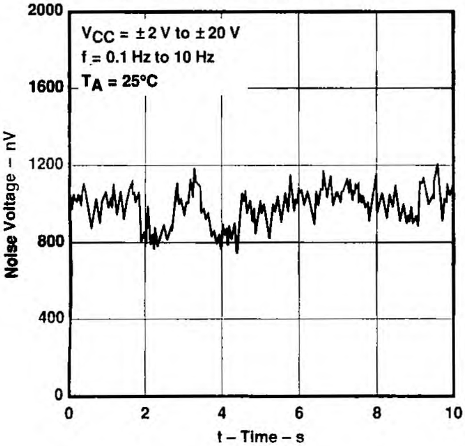


FIGURE 17

EQUIVALENT INPUT NOISE VOLTAGE
and EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

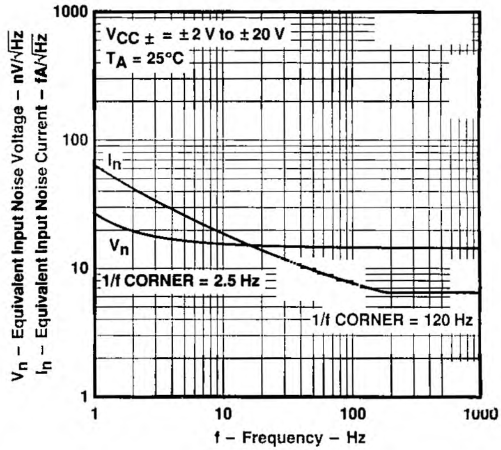


FIGURE 18

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

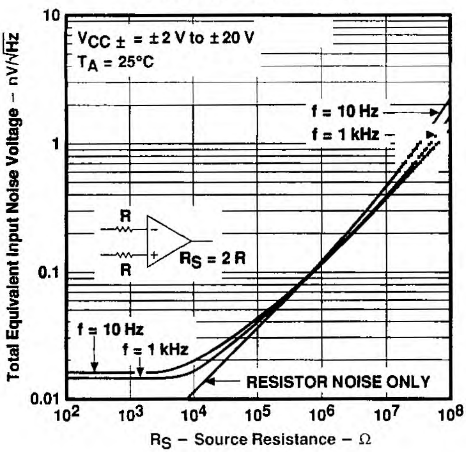


FIGURE 19

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

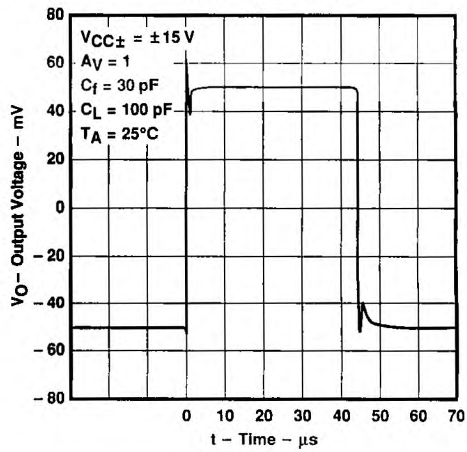


FIGURE 20

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

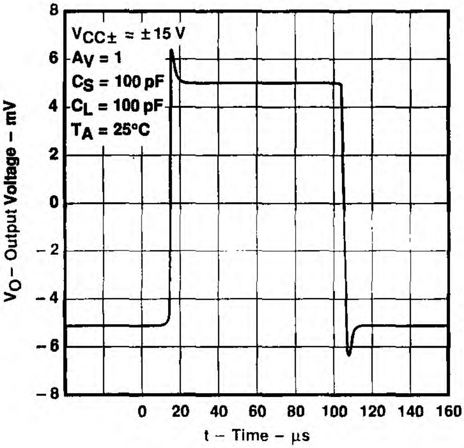


FIGURE 21

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

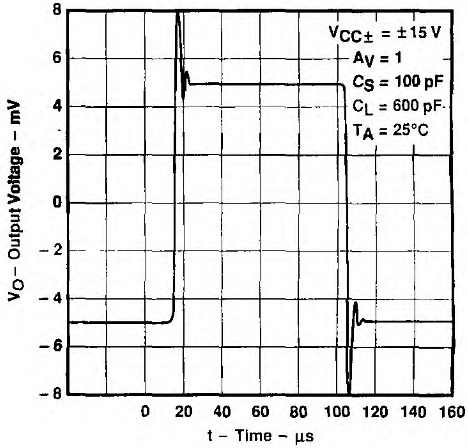


FIGURE 22

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

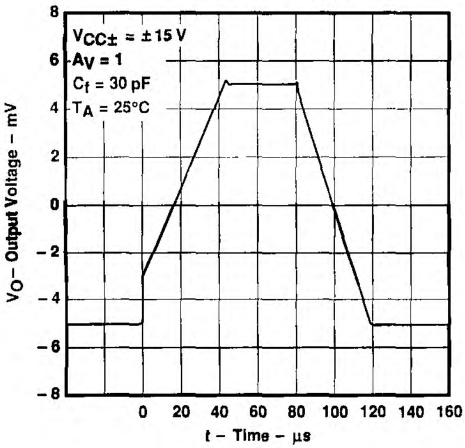


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

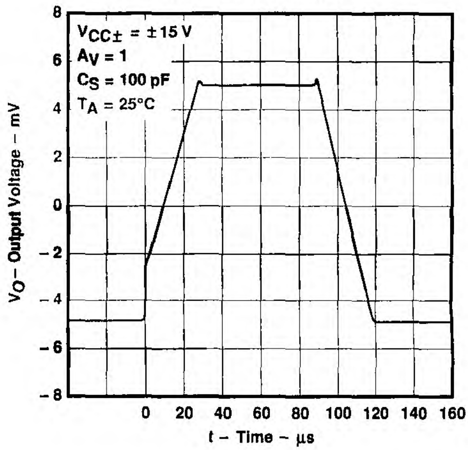


FIGURE 24

TYPICAL APPLICATION DATA

achieving picoampere, microvolt performance

Proper care should be exercised to realize the picoampere, microvolt accuracy of the LT1008. Because leakage currents in external circuitry can significantly degrade performance, high-quality insulation should be used (e. g.,Teflon, Kel-F). All insulating surfaces should be cleaned to remove fluxes and other residues. Surface coating may be necessary to provide a moisture barrier in high-humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs (see Figure 25). In inverting configurations, the guard ring should be tied to ground; in noninverting configurations, the guard ring should be tied to the inverting input (pin 2). Both sides of the printed circuit board should be guarded. Bulk leakage reduction depends on the guard ring width. Nanoampere-level leakage into the compensation terminals can affect input offset voltage and its temperature coefficient (see Figure 26).

Microvolt-level error voltages can also be generated in the external circuitry. Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent temperature coefficient of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature. The LT1008 is specified over a wide range of supply voltages from ±2 V to ±18 V. Operation with lower supplies (down to ±1 V) is possible with two Ni-Cad batteries.

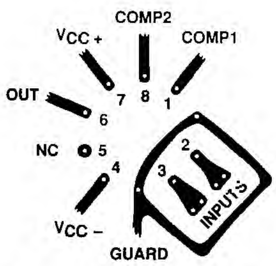
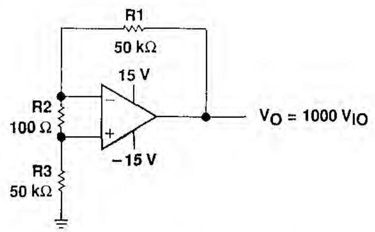


FIGURE 25. GUARD RING



NOTES: A. Resistors must have low thermoelectric potential.
B. This circuit is also used as the burn-in configuration for the LT1008, with supply voltages increased to ± 20 V, R1 = R3 = 20 kΩ, R2 = 200 Ω, and A_V = 100.

FIGURE 26. TEST CIRCUIT FOR V_{IO} AND α_{VIO}

noise testing

The peak-to-peak equivalent input noise voltage of the LT1008 is measured in the test circuit shown in Figure 27. The frequency response of this noise tester indicates that the 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

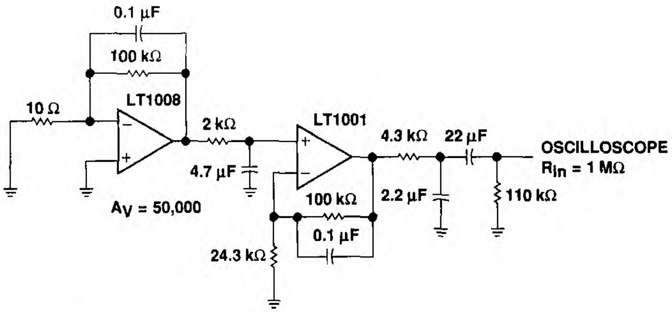
An input noise voltage test is recommended when measuring noise in a large number of units. A 10-Hz input noise voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured by the current shown in Figure 28 and calculated by the following formula in which the noise of the source resistors is subtracted:

$$I_n = \frac{[V_{no}^2 - (820\ nV)^2]^{1/2}}{40\ M\Omega \times 100}$$

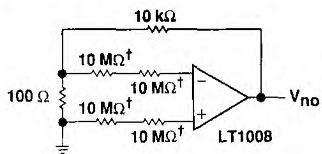
TYPICAL APPLICATION DATA

noise testing (continued)



NOTE A : All capacitor values are for nonpolarized capacitors only.

FIGURE 27. 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE TEST CIRCUIT

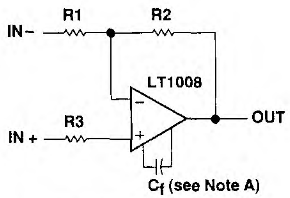


† Metal film.

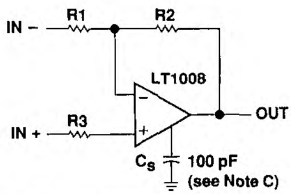
FIGURE 28. NOISE CURRENT TEST CIRCUIT

frequency compensation

The LT1008 is externally frequency compensated with a single capacitor. The two compensation circuits shown in Figure 29 are identical to the frequency compensation circuits for the LM108A series. Therefore, the LT1008 operational amplifiers can be inserted directly into LM108A or LM308A sockets, with similar ac and upgraded dc performance.



(a) STANDARD COMPENSATION



(b) ALTERNATE COMPENSATION (see Note B)

NOTES: A. $C_f \geq (R1 \times C_o) / (R1 + R2)$, C_o = 30 pF. Bandwidth and slew rate are proportional to $1/C_f$.
B. This circuit improves the supply voltage rejection ratio by a factor of 5.
C. Bandwidth and slew rate are proportional to $1/C_S$.
D. For (R2/R1) > 200, no external frequency compensation is necessary.

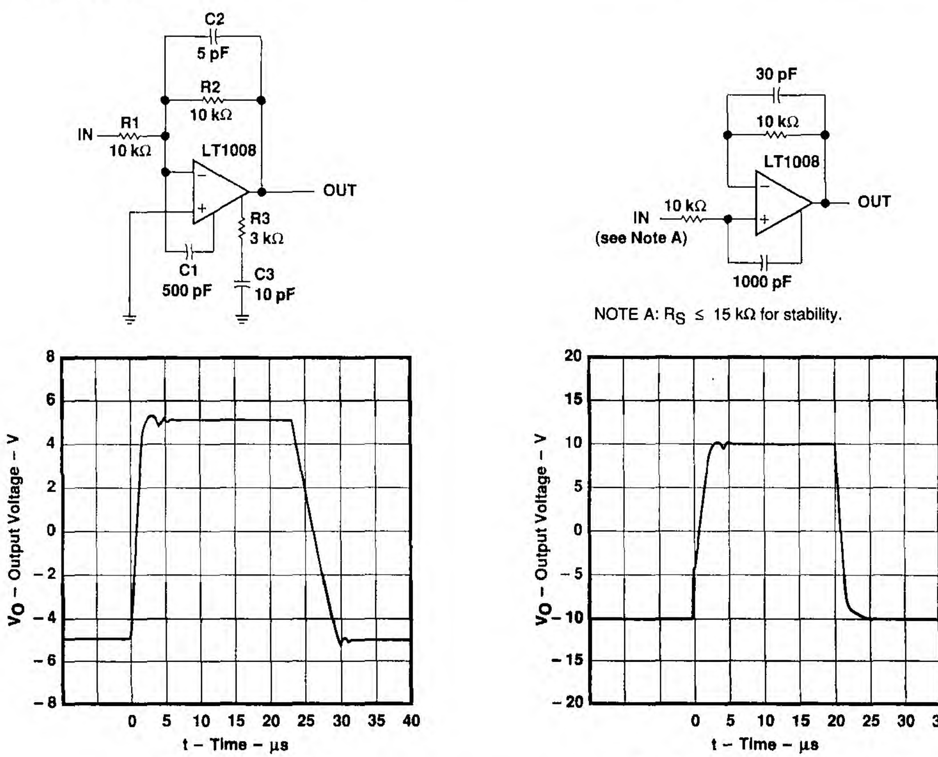
FIGURE 29. FREQUENCY COMPENSATION CIRCUITS (see Note D)

TYPICAL APPLICATION DATA

frequency compensation (continued)

External frequency compensation provides additional flexibility in shaping the frequency response of the amplifier. For example, for a voltage gain of 10 and C_f = 3 pF, a gain-bandwidth product of 5 MHz and slew rate of 1.2 V/µs can be realized. For closed-loop gains greater than 200, no external compensation is necessary, and the slew rate increases to 4 V/µs. The LT1008 can also be overcompensated (e.g., $C_f > 30$ pF or $C_S > 100$ pF) to improve capacitive-load-handling capability or to narrow noise bandwidth. In applications in which the feedback loop around the amplifier has gain, overcompensation can stabilize the circuit with a single capacitor.

The availability of the compensation terminals permits the use of feed-forward frequency compensation to enhance slew rate in low closed-loop-gain configurations (see Figure 30). The inverter slew rate is increased to 1.4 V/µs. The voltage-follower feed-forward scheme bypasses the amplifier's gain stages and slews at nearly 10 V/µs.



(a) INVERTER FEED-FORWARD

(b) VOLTAGE-FOLLOWER FEED-FORWARD

FIGURE 30. FREQUENCY COMPENSATION CIRCUITS and VOLTAGE-FOLLOWER PULSE RESPONSES

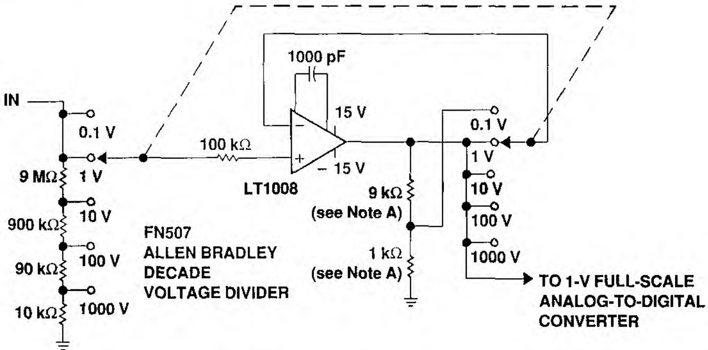
TYPICAL APPLICATION DATA

other considerations

The inputs of the LT1008 are protected by back-to-back diodes. Current-limiting resistors are not used because the leakage of these resistors would prevent the realization of picoampere-level bias currents at elevated temperatures. In the voltage-follower configuration, when the input is driven by a fast, large-signal pulse (> 1 V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection, flows through the diodes.

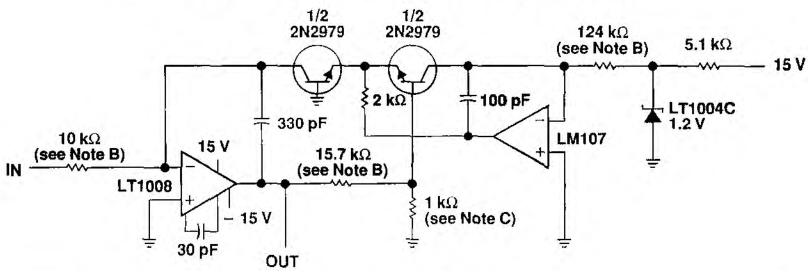
The use of a feedback resistor, as shown in the voltage-follower feed-forward diagram, is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

typical applications



NOTES: A. Ratio match ± 0.01 %.
B. This application requires low bias current, low offset voltage and offset voltage temperature coefficient, low noise, and low long-term offset voltage drift.

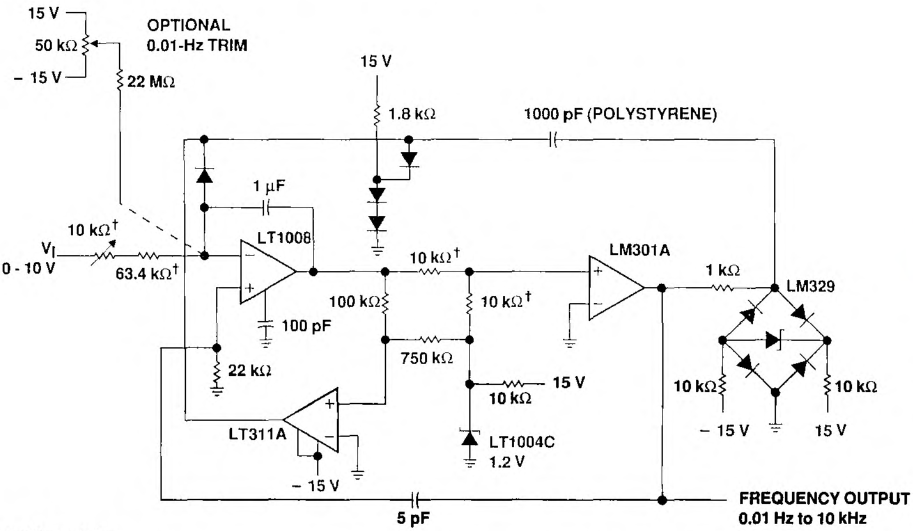
FIGURE 31. INPUT AMPLIFIER FOR 4 1/2-DIGIT VOLTMETER



NOTES: A. The low bias current and offset voltage of the LT1008 allow 4 1/2 decades of voltage input logging.
B. 1% film resistor.
C. Tel. Labs, Type Q81.

FIGURE 32. LOGARITHMIC AMPLIFIER

TYPICAL APPLICATION DATA



†1% metal film resistor

NOTES: A. The LT1008 integrator extends the low frequency range. The total dynamic range is 0.01 Hz to 10 kHz (or 120 dB) with 0.01% linearity.
B. All diodes 1N4148.

FIGURE 33. EXTENDED RANGE CHARGE PUMP VOLTAGE-TO-FREQUENCY CONVERTER

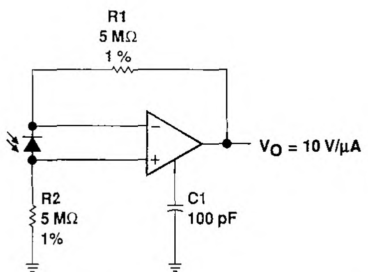
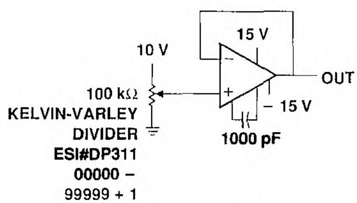


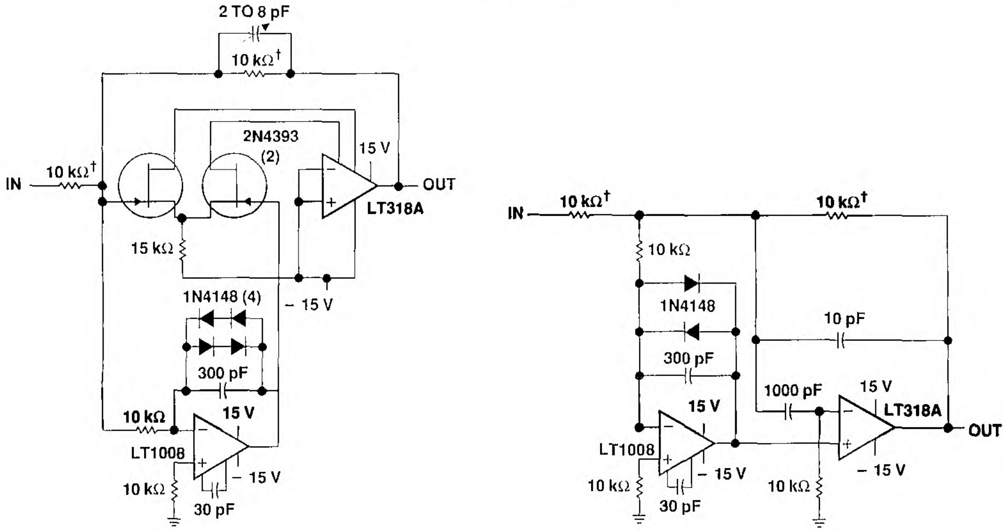
FIGURE 34. AMPLIFIER FOR PHOTODIODE SENSOR



NOTE A: Approximate error due to noise, bias current, common-mode rejection, and voltage gain of the amplifier is 1/5 of a least significant bit.

FIGURE 35. FIVE-DECADE KELVIN-VARLEY DIVIDER BUFFERED BY THE LT1008

TYPICAL APPLICATION DATA

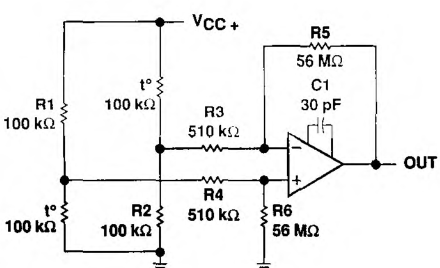


(a) SR = 100 V/µs
I_{IB} = 30 pA
V_{IO} = 30 µV
Settling = 5 µs to 0.01%/10-V step

(b) SR = 50 V/µs
I_{IB} = 30 pA
V_{IO} = 30 µV
α_{VIO} = 0.3 µV/°C
BW = 2 MHz
Settling = 12 µs to 0.01%/10-V step

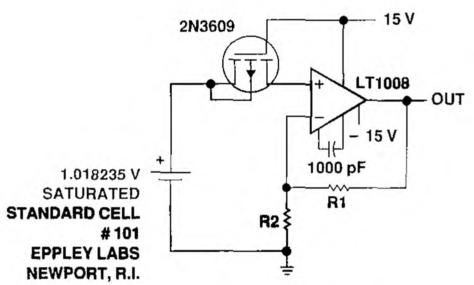
†1% metal film resistor.

FIGURE 36. FAST PRECISION INVERTERS



NOTE A : A_{VD} = 100.

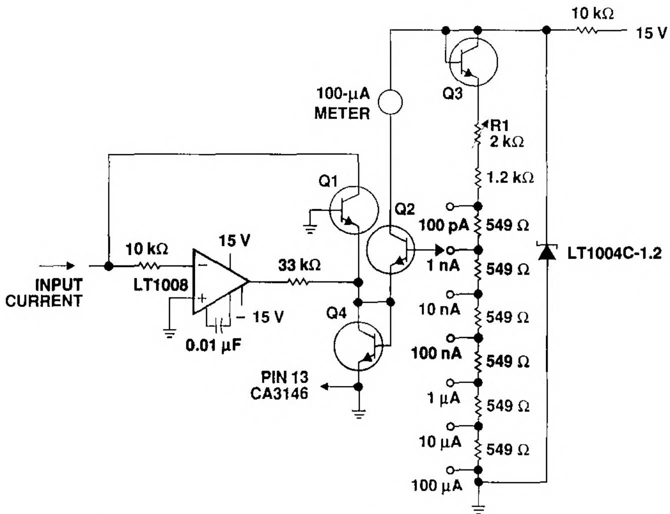
FIGURE 37. AMPLIFIER FOR BRIDGE TRANSDUCERS



NOTE A : The typical 30-pA input bias current of the LT1008 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

FIGURE 38. SATURATED STANDARD-CELL AMPLIFIER

TYPICAL APPLICATION DATA



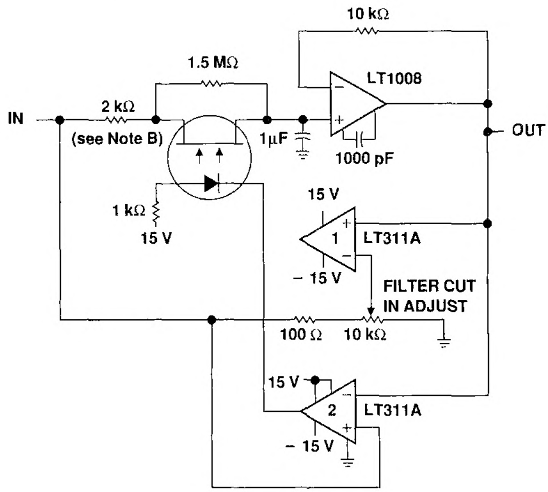
NOTES: A. This ammeter measures currents from 100 pA to 100 μA without the use of expensive high-value resistors. Accuracy at 100 μA is limited by the offset voltage between Q1 and Q2 and, at 100 pA, by the inverting bias current of the LT1008.

B. Q1-Q4 RCA CA3146 transistor array.

C. Adjust R1 for full-scale deflection with 1-μA input current.

FIGURE 39. AMMETER WITH 6-DECADE RANGE

TYPICAL APPLICATION DATA



NOTES: A. This circuit is useful where fast signal acquisition and high precision are required, as in electronic scales. The filter's time constant is set by the 2-kΩ resistor and the 1-µF capacitor until COMP1 switches. The time constant is then set by the 1.5-MΩ resistor and the 1-µF capacitor. COMP2 provides a quick reset. The circuit settles to a final value three times as fast as a simple 1.5-MΩ, 1-µF filter with almost no dc error.

B. OPTO-MOS switch, Type OFMIA, Theta-J Corp.

FIGURE 40. PRECISION, FAST-SETTLING, LOW-PASS FILTER.

TEXAS INSTRUMENTS
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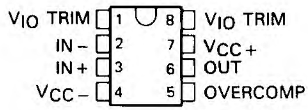
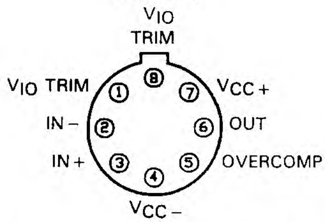
D3186, MARCH 1989

- Internally Compensated
- Input Offset Voltage:
  LT1012M . . . 35 μV Max
  LT1012C . . . 50 μV Max
- Input Bias Current (LT1012M):
  100 pA Max at 25°C
  600 pA Max from −55°C to 125°C
- αV_{IO} . . . 1.5 μV/°C Max
- Typical Peak-To-Peak Noise Voltage . . . 0.5 μV at f = 0.1 Hz to 10 Hz
- Low Supply Current . . . 600 μA Max
- CMRR . . . 114 dB Min (LT1012M)
- k_{SVR} . . . 114 dB Min (LT1012M)
- 5-mA Load Current with Voltage Gain of 200,000 Min (LT1012M)

P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



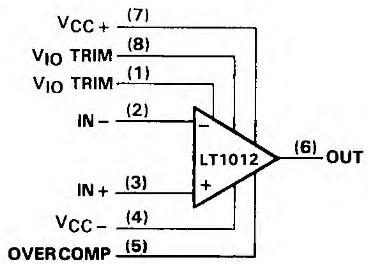
Pin 4 (L package) is in electrical contact with the case.

description

The LT1012 is an internally compensated operational amplifier that can be used in practically all precision applications. The LT1012 combines picoampere bias currents (maintained over the full temperature range), microvolt offset voltage, low offset voltage temperature coefficient and long-term drift, low voltage and current noise, and low power dissipation. High common-mode and supply voltage rejection ratios, low warm-up drift, and the capability to deliver 5-mA load current with a voltage gain of 200,000 complete the LT1012's precision specifications.

The LT1012M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1012C is characterized for operation from 0°C to 70°C.

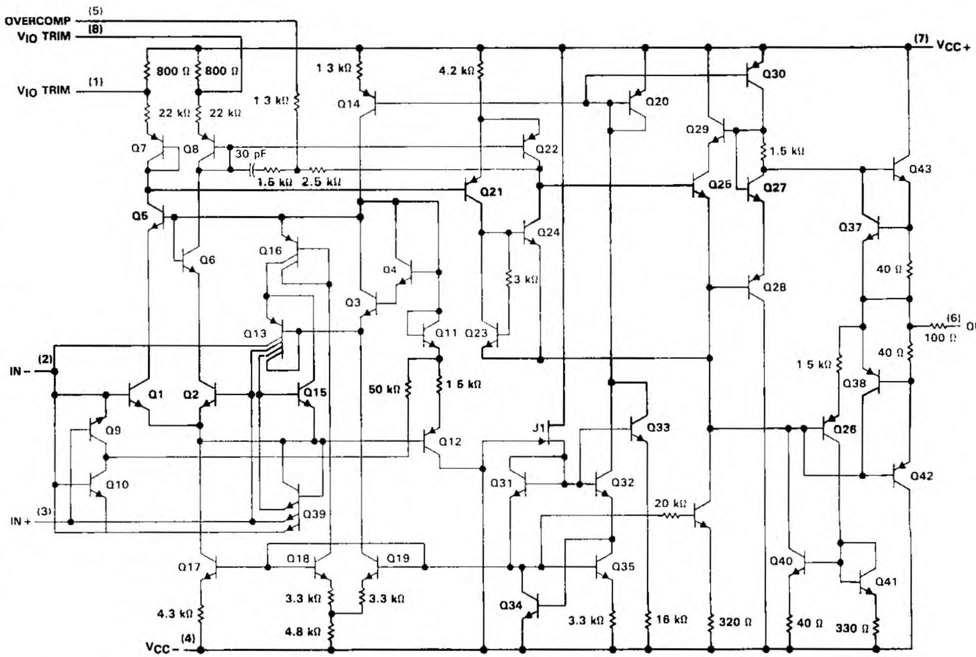
symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE	
		METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	50 μV	LT1012CL	LT1012CP
−55°C to 125°C	35 μV	LT1012ML	−

schematic



All resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	+20 V
Supply voltage, V_{CC-} (see Note 1)	−20 V
Input voltage	$V_{CC\pm}$
Differential input current (see Note 2)	±10 mA
Duration of output short-circuit at or below 25°C	unlimited
Operating free-air temperature range: LT1012M	−55°C to 125°C
LT1012C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: L package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages greater than 1 V cause excessive current to flow through the input protection diodes unless limiting resistance is used.

TEXAS INSTRUMENTS
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electrical characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A†	LT1012M MIN	LT1012M TYP	LT1012M MAX	LT1012C MIN	LT1012C TYP	LT1012C MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		8	35		10	50	µV
			Full range			180			120	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		20	90		25	120	
			Full range			250			200	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		20	90		25	120	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			250			200	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		[illegible]	[illegible]		0.2	[illegible]	[illegible]
	Long-term drift of input offset voltage		25°C		0.3			0.3		µV/mo
I_{IO}	Input offset current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		15	100		20	150	pA
			Full range			250			230	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		25	150		30	200	
			Full range			350			300	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		25	150		30	200	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			350			300	
α_{IIO}	Average temperature coefficient of input offset current		Full range		0.3	2.5		0.3	2.5	pA/°C
I_{IB}	Input bias current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		±25	±100		±30	±150	pA
			Full range			±600			±230	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		±35	±150		±40	±200	
			Full range			±800			±300	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		±35	±150		±40	±200	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			±800			±300	
α_{IIB}	Average temperature coefficient of input bias current		Full range		0.6	6		0.3	2.5	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13.5	±14		±13.5	±14		V
			Full range	±13.5			±13.5			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±13	±14		±13	±14		V
			Full range	±13			±13			
A_{VD}	Large-signal differential voltage amplification	V_O = ±12 V, R_L ≥ 10 kΩ	25°C	300	2000		200	2000		V/mV
			Full range	100			100			
		V_O = ±10 V, R_L ≥ 2 kΩ	25°C	200	1000		120	1000		
			Full range	100			100			
CMRR	Common-mode rejection ratio	V_{IC} = ±13.5 V	25°C	114	132		110	132		dB
			Full range	108			108			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±20 V	25°C	114	132		110	132		dB
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range	108			108			
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		380	600		380	600	µA
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C			600		380	600	
			Ful [illegible]			800			800	

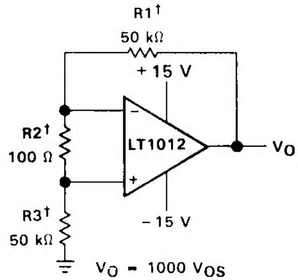
† Full range is −55°C to 125°C for the LT1012M and 0°C to 70°C for the LT1012C.

operating characteristics at T_A = 25°C, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	LT1012M			LT1012C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain		0.1	0.2		0.1	0.2		V/μs
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f= 0.1 Hz to 10 Hz		0.5			0.5	0.65	μV
V_n	Equivalent input noise voltage	f= 10 Hz, See Note 3		17	30		17	30	nV/√Hz
		f= 1 kHz		14	22		14	22	
I_n	Equivalent input noise current	f= 10 Hz		20			20		fA/√Hz

NOTE 3: This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



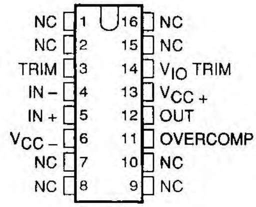
† Resistors must have low thermoelectric potential.
This circuit is also used as the burn-in configuration for the LT1012, with supply voltages increased to ± 20 V, R1 = R3 = 20 kΩ, R2 = 200 Ω, A_V = 100.

FIGURE 1. TEST CIRCUIT FOR OFFSET VOLTAGE AND ITS TEMPERATURE COEFFICIENT

D3239, MAY 1988 – REVISED MARCH 1989

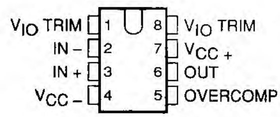
- Very Low Input Noise Voltage: 1.1 nV/√Hz Max , 0.85 nV/√Hz Typ at 1 kHz for LT1028AM, LT1028AC
- Low Peak-To-Peak Input Noise Voltage . . . 35 nV Typ at f = 0.1 Hz to 10 Hz
- Noise Voltage and Current 100% Tested
- Gain-Bandwidth Product . . . 50 MHz Min
- Slew Rate . . . 11 V/µs Min
- Input Offset Voltage . . . 40 µV Max at 25°C for LT1028AM, LT1028AC
- Offset Voltage Temperature Coefficient . . . 0.8 µV/°C Max for LT1028AM, LT1028AC
- Applications:
  - Low-Noise Frequency Synthesizers
  - High-Quality Audio
  - Infrared Detectors
  - Accelerometer and Gyro Amplifiers
  - 350-Ω Bridge Signal Conditioning
  - Magnetic Search Coil Amplifiers
  - Hydrophone Amplifiers

DW PACKAGE
(TOP VIEW)

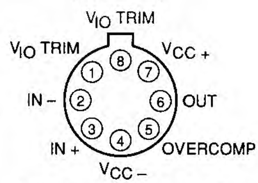


NC – No internal connection

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L package) is in electrical contact with the case.

description

The LT1028 features excellent noise performance combined with high-speed specifications, distortion-free output, and true precision parameters. Although the LT1028 input stage operates at collector currents of nearly 1 mA to achieve low voltage noise, the input bias current is only 25 or 30 nA at 25°C. The noise voltage of the LT1028 is less than the noise of a 50-Ω resistor. Therefore, even in very-low-source-impedance transducer or audio amplifier applications, the device's contribution to total system noise will be negligible.

The LT1028AM and LT1028M are characterized for operation over the full military temperature range of −55°C to 125°C. The LT1028AC and LT1028C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE: SMALL OUTLINE (DW)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to [illegible]	40 µV	—	LT[illegible]	LT1028ACL	LT[illegible]CP
	80 µV	LT1028ACDW	LT[illegible]G	LT[illegible]	LT[illegible]P
[illegible] to 125°C	40 µV	—	LT[illegible]MJG	LT[illegible]	—
	80 µV	—	LT[illegible]MJG	LT[illegible]	—

TEXAS INSTRUMENTS

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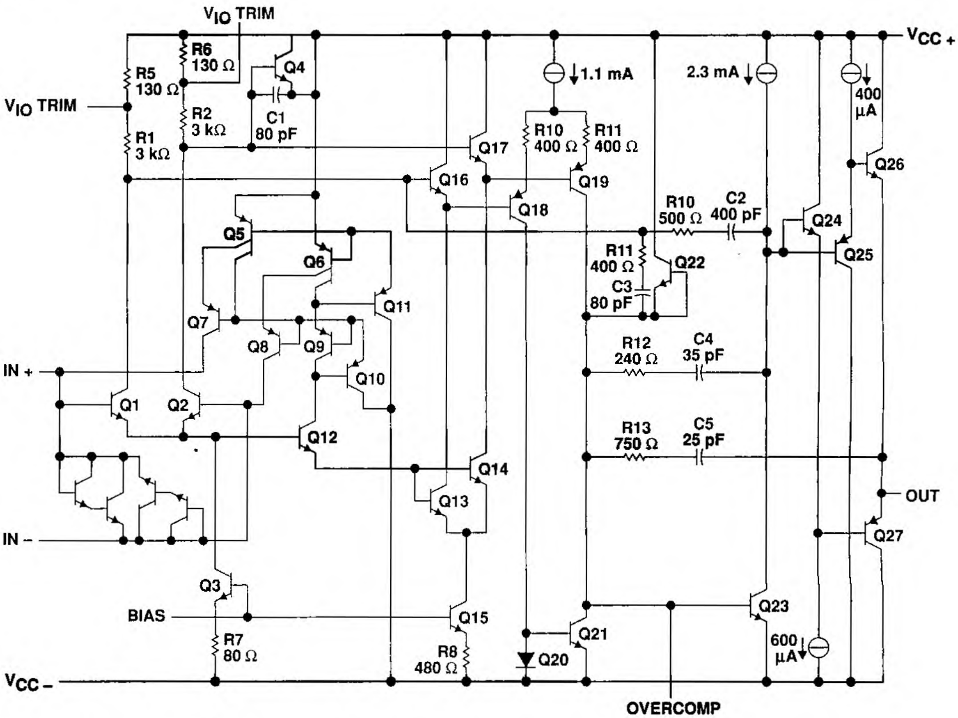
schematic



All component and current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1):	LT1028AM, LT1028M	22 V
	LT1028AC, LT1028C	16 V
Supply voltage, V_{CC-} (see Note 1)	LT1028AM, LT1028M	− 22 V
	LT1028AC, LT1028C	− 16 V
Differential input current (see Note 2)		± 25 mA
Input voltage range, V_I (any input, see Note 1)		V_{CC} ±
Duration of output short-circuit at (or below) 25°C (see Note 2)		unlimited
Operating free-air temperature, T_A:	LT1028AM, LT1028M	− 55°C to 125°C
	LT1028AC, LT1028C	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The specified values for this parameter takes into account junction temperature increase due to supply and output currents.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1028M			LT1028AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	80		10	40	μV
			– 55°C to 125°C			180			120	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.25	1		0.2	0.8	μV/°C
	Input offset voltage long-term drift	See Note 4	25°C		0.3			0.3		μV/mo
I_{IO}	Input offset current	$V_{IC} = 0$	25°C		18	100		12	50	nA
			– 55°C to 125°C			180			90	
I_{IB}	Input bias current	$V_{IC} = 0$	25°C		30	180		25	90	nA
			– 55°C to 125°C			300			150	
V_{ICR}	Common-mode input voltage range			± 11	± 12.2		± 11	± 12.2		V
			– 55°C to 125°C	± 10.3			± 10.3			
V_{OM}	Maximum peak output voltage swing	$R_L \geq 2$ kΩ	25°C	± 12	± 13		± 12.3	± 13		V
			– 55°C to 125°C	± 10.3			± 10.3			
		$R_L \geq 600$ Ω	25°C	± 10.5	± 12.2		± 11	± 12.2		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 12$ V, $R_L \geq 2$ kΩ	25°C	5	30		7	30		V/μV
		$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	– 55°C to 125°C	2			3			
		$V_O = \pm 10$ V, $R_L \geq 1$ kΩ	25°C	3.5	20		5	20		
			– 55°C to 125°C	1.5			2			
		$V_O = \pm 10$ V, $R_L \geq 600$ Ω	25°C	2	15		3	15		
r_{ic}	Common-mode input resistance		25°C		300			300		MΩ
r_{id}	Differential-mode input resistance		25°C		20			20		kΩ
c_i	Input capacitance		25°C		5			5		pF
z_o	Output impedance	$V_O = 0$, $I_O = 0$, Open loop	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 11$ V	25°C	110	126		114	126		dB
		$V_{IC} = \pm 10.3$ V	– 55°C to 125°C	100			106			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18V	25°C	110	132		117	133		dB
		$V_{CC\pm} = \pm 4.5$ V to ± 16V	– 55°C to 125°C	104			110			
I_{CC}	Supply current		25°C		7.6	10.5		7.4	9.5	mA
			– 55°C to 125°C			13			11.5	

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Input offset voltage long-term drift refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	LT1028C MIN	LT1028C TYP	LT1028C MAX	LT1028AC MIN	LT1028AC TYP	LT1028AC MAX	UNIT
V_{IO}	Input offset voltage	See Note 3	25°C		20	80		10	40	μV
			0°C to 70°C			125			80	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.2	1		0.1	0.8	μV/°C
	Input offset voltage long-term drift	See Note 4	25°C		0.3			0.3		μV/mo
I_{IO}	Input offset current	$V_{IC} = 0$	25°C		18	100		12	50	nA
			0°C to 70°C			130			65	
I_{IB}	Input bias current	$V_{IC} = 0$	25°C		30	180		25	90	nA
			0°C to 70°C			240			120	
V_{ICR}	Common-mode input voltage range		25°C	± 11	± 12.2		± 11	± 12.2		V
			0°C to 70°C	± 10.5			± 10.5			
V_{OM}	Maximum peak output voltage swing	$R_L \geq 2$ kΩ	25°C	± 12	± 13		± 12.3	± 13		V
			0°C to 70°C	± 11.5			± 11.5			
		$R_L \geq 600$ Ω	25°C	± 10.5	± 12.2		± 11	± 12.2		
		RL ≥ 600 Ω, See Note 2	70°C	± 9	± 10.5		± 9.5	± 11		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 12$ V, $R_L \geq 2$ kΩ	25°C	5	30		7	30		V/μV
		$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	0°C to 70°C	3			5			
		$V_O = \pm 10$ V, $R_L \geq 1$ kΩ	25°C	3.5	20		5	20		
			0°C to 70°C	2.5			4			
		$V_O = \pm 10$ V, $R_L \geq 600$ Ω	25°C	2	15		3	15		
r_{ic}	Common-mode input resistance		25°C		300			300		MΩ
r_{id}	Differential-mode input resistance		25°C		20			20		kΩ
c_i	Input capacitance		25°C		5			5		pF
z_o	Output impedance	$V_O = 0$, $I_O = 0$, Open loop	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 11$ V	25°C	110	126		114	126		dB
		$V_{IC} = \pm 10.3$ V	0°C to 70°C	106			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18V	25°C	110	132		117	133		dB
		$V_{CC\pm} = \pm 4.5$ V to ± 16V	0°C to 70°C	107			114			
I_{CC}	Supply current		25°C		7.6	10.5		7.4	9.5	mA
			0°C to 70°C			11.5			10.5	

NOTES: 2. The specified values for this parameter takes into account junction temperature increase due to supply and output currents.
3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Input offset voltage long-term drift refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LT1028M, LT1028C			LT1028AM, LT1028AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$A_V = -1$	11	15		11	15		V/µs
V_{NPP}	Peak-to-peak equivalent input noise vlotage	f = 0.1 Hz to 10 Hz		35	90		35	75	nV
V_n	Equivalent input noise voltage	f = 10 Hz, See Note 5		1	1.9		1	1.7	nV/√Hz
		f = 1 kHz		0.9	1.2		0.85	1.1	
I_n	Equivalent input noise current	f = 10 Hz, See Note 6		4.7	12		4.7	10	pA/√Hz
		f = 1 kHz, See Note 6		1	1.8		1	1.6	
[illegible]	Gain bandwidth product	f = 20 kHz	50	75		50	75		MHz

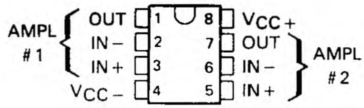
NOTES: 5. 10-Hz equivalent input noise voltage is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

6. Noise current is defined and measured with balanced source resistors. The resulting voltage (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain noise current. Maximum 10-Hz noise current can be inferred from testing at 1 kHz.

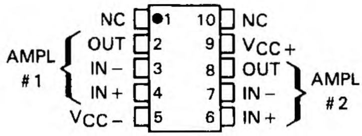
D972, FEBRUARY 1971—REVISED MAY 1988

- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

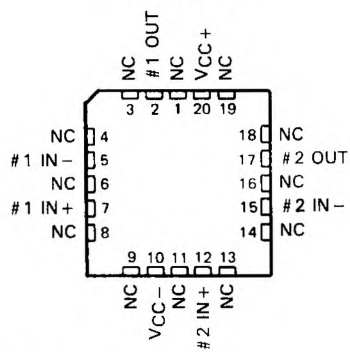
MC1558 . . . JG PACKAGE
MC1458 . . . D, JG, OR P PACKAGE
(TOP VIEW)



MC1558 . . . U FLAT PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

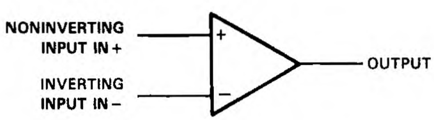
description

The MC1558 and MC1458 are dual general-purpose operational amplifiers with each half electrically similar to the uA741 except that offset null capability is not provided.

The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1558 is characterized for operation over the full military temperature range of −55°C to 125°C; the MC1458 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
MC1558	FK,JG,U	−55°C to 125°C	5 mV
MC1458	D,JG,P	0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e., MC1458DR)

TEXAS INSTRUMENTS
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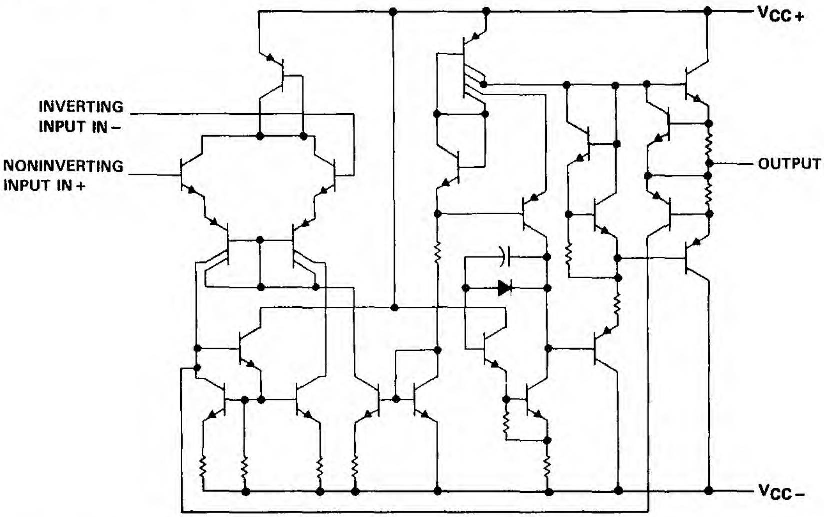
schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC1558	MC1458	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage at either input (see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	65 to 150	°C
Case temperature for 60 seconds: FK package		260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible] mW	5.8 [illegible]	33°C	[illegible] mW	–
FK	680 mW	11.0 mW/°C	88°C	880 mW	275 mW
JG (MC1558)	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
JG (MC1458)	680 mW	6.6 mW/°C	47°C	528 mW	–
P	680 mW	8.0 mW/°C	65°C	640 mW	–
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	[illegible]		20	200		20	[illegible]	nA
			Full range			[illegible]			[illegible]	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	[illegible]		80	[illegible]	nA
			[illegible]			[illegible]			800	
V_{ICR}	Common-mode input voltage range		[illegible]	±12	±13		±12	±13		V
			[illegible]	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	[illegible]	±12	±14		±12	±14		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			
		$R_L = 2\ k\Omega$	25°C	±10	±13		±10	±13		
		$R_L \geq 2\ k\Omega$	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	[illegible]	50	200		20	[illegible]		V/mV
			Full range	25			15			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	$R_L = 2\ k\Omega$, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	$A_{VD} = 1$	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25°C	70	90		70	90		dB
			Full Range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		30	150		30	150	μV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 0$, f = 1 kHz, BW = 1 Hz	25°C		45			45		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	No load, $V_O = 0$	25°C		3.4	5		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	No load, $V_O = 0$	25°C		100	[illegible]		100	170	mW
			[illegible]			[illegible]			[illegible]	
V_{o1}/V_{o2}	Crosstalk attenuation		[illegible]		120			120		dB

†All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1558 is −55°C to 125°C and for MC1458 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

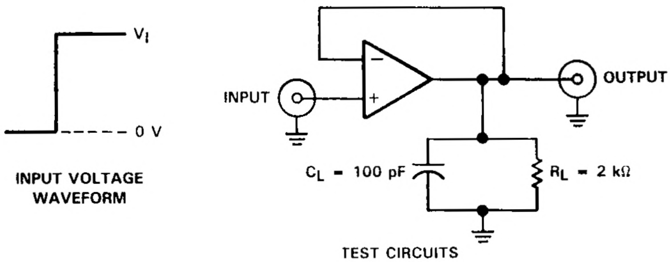


FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

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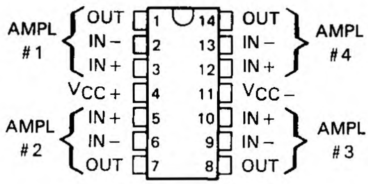
D2517, FEBRUARY 1979—REVISED MAY 1988

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to be Interchangeable with Motorola MC3303, MC3403**

MC3303, MC3403 . . . D, J, OR N PACKAGE
(TOP VIEW)

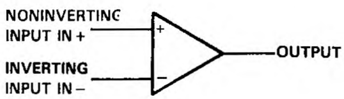


description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} − 1.5 V. Quiescent supply currents are less than one-half those of the uA741.

The MC3303 is characterized for operation from −40°C to 85°C and the MC3403 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

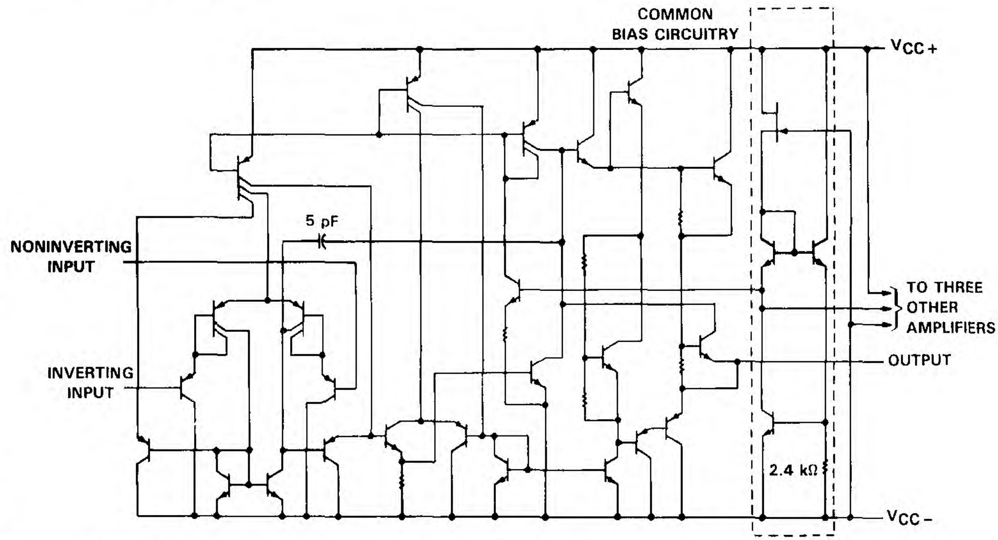


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	MC3403D	MC3403J	MC3403N
−40°C to 85°C	8 mV	MC3303D	MC3303J	MC3303N

D packages are available taped and reeled. Add "R" suffix to the device type when ordering. (e.g., MC3403DR)

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC3303	MC3403	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
[illegible]ly voltage V_{CC+} with respect to V_{CC-}		36	36	V
[illegible]rential input voltage (see Note 2)		±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	[illegible] mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics at specified free-air temperature; V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403

PARAMETER		TEST CONDITIONS†		MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 4	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 4	Full range		10			10		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		30	75		30	50	nA
			Full range			[illegible]			200	
α_{IIO}	Temperature coefficient of input offset current	See Note 4	Full range		50			50		pA/°C
I_{IB}	Input bias current	See Note 4	25°C		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	12	12.5		±12	[illegible]		V
		R_L = 2 kΩ	25°C	10	12		±10	[illegible]		
		R_L = 2 kΩ	Full range	10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±2.5 to ±15 V	25°C		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 4	25°C		2.8	7		2.8	7	mA

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.

§Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 4: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403, and V_O = 7 V for MC3303.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V			−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	$V_{CC+}-1.7$			$V_{CC+}-1.7$			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±15 V to ±2.5 V			150			150	µV/V
I_{CC}	Supply current	No load, V_O = 2.5 V		2.5	7		2.5	7	mA
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403; T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		0.6		V/µs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		µs
t_f	Fall time			0.35		µs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

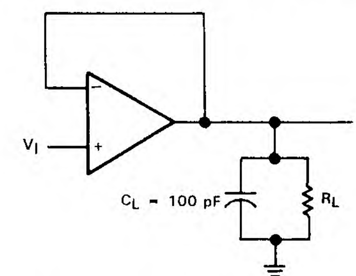


FIGURE 1. UNITY-GAIN AMPLIFIER

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

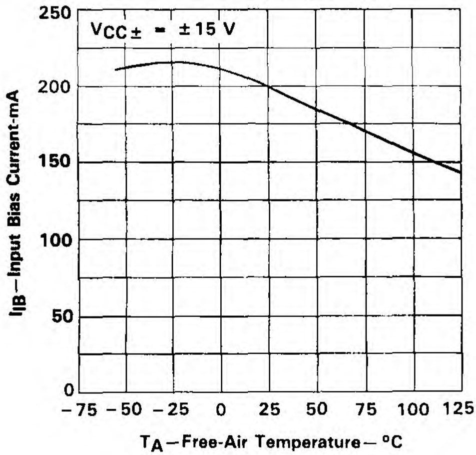


FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

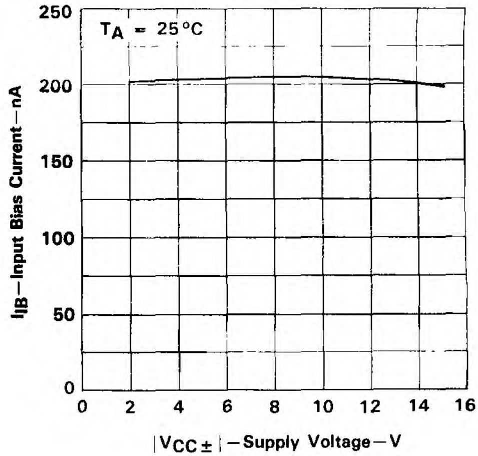


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

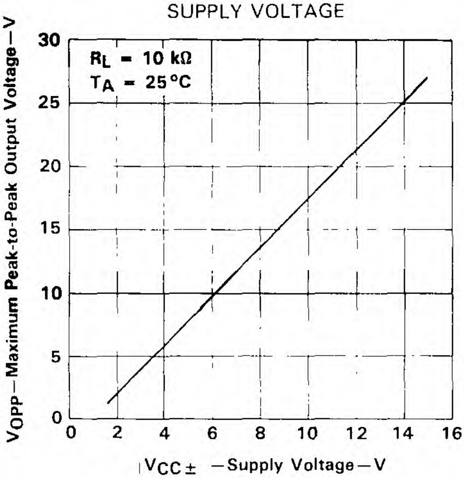


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

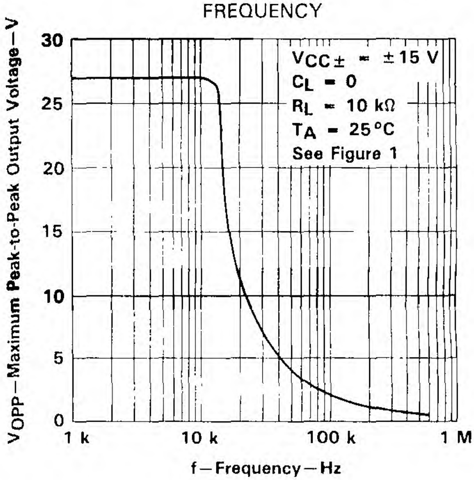


FIGURE 5

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

2

Operational Amplifiers

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

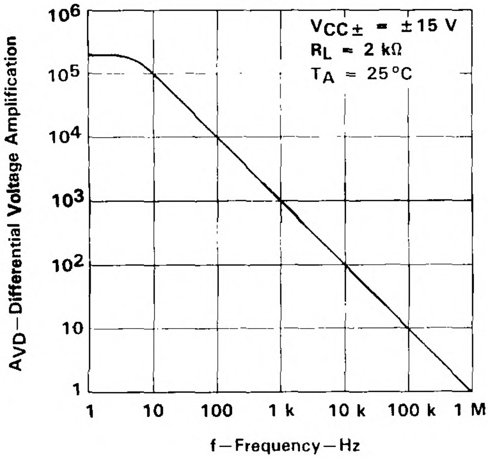


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

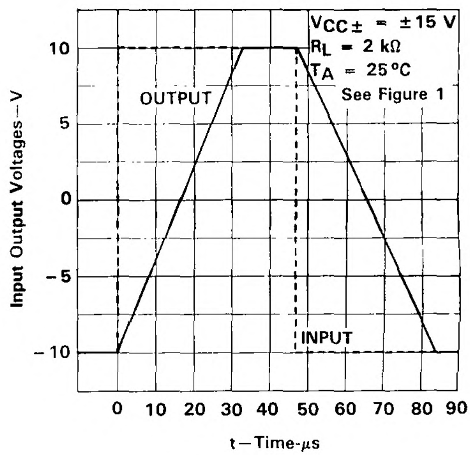


FIGURE 7

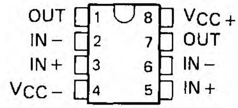
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

NOV · 1979 – REVISED MAY 1988

- Equivalent Input Noise Voltage . . . 5 nV/√Hz Typ at 1 kHz
- Unity-Gain Bandwidth . . . 10 MHz Typ
- Common-Mode Rejection Ratio . . . 100 dB Typ
- High DC Voltage Gain . . . 100 V/m Typ
- Peak-to-Peak Output Voltage Swing . . . 32 V Typ with $V_{CC\pm} = \pm 18$ V and $R_L = 600\ \Omega$
- High Slew Rate . . . 9 V/μs Typ
- Wide Supply Voltage Range . . . ±3 V to ±20 V
- Designed to be Interchangeable with Signetics NE5532 and NE5532A

**NE5532, NE5532A . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)**



description

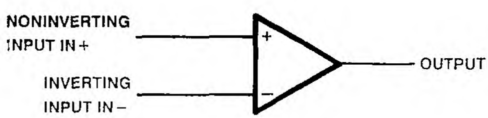
The NE5532 and NE5532A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are internally compensated for unity gain operation. The NE5532A has specified maximum limits for equivalent input noise voltage.

The NE5532 and NE5532A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE	
		CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5532JG NE5532AJG	NE5532P NE5532AP

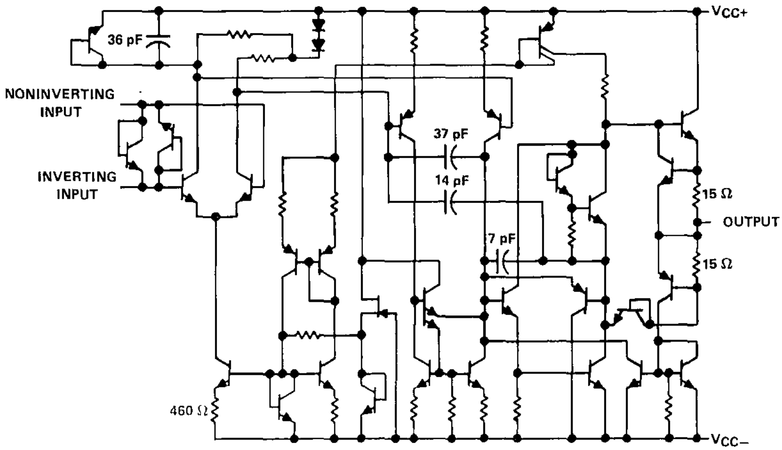
symbol (each amplifier)



TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −22 V
Input voltage, either input (see Notes 1 and 2) . . . . . $V_{CC\pm}$
Input current (see Note 3) . . . . . ±10 mA
Duration of output short-circuit (see Note 4) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

electrical characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	$T_A = 25°C$		0.5	4	mV
			$T_A = 0°C$ to $70°C$			5	
I_{IO}	Input offset current	$T_A = 25°C$			10	150	nA
		$T_A = 0°C$ to $70°C$				200	
I_{IB}	Input bias current	$T_A = 25°C$			200	800	nA
		$T_A = 0°C$ to $70°C$				1000	
V_{ICR}	Common-mode input voltage range			±12	±13		V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		
	[illegible]		[illegible]	60	62		
A_{VD}	Large-signal differential voltage amplification	$R_L \ge 600\ \Omega$, $V_O = \pm10$ V	$T_A = 25°C$	15	50		V/mV
			$T_A = 0°C$ to $70°C$	10			
		$R_L \ge 2\ k\Omega$, $V_O = \pm10$ V	$T_A = 25°C$	25	100		
			$T_A = 0°C$ to $70°C$	15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	$R_L = 600\ \Omega$,	$V_O = \pm10$ V		140		kHz
		$R_L = 600\ \Omega$,	$V_{CC\pm} = \pm18$ V, $V_O = \pm14$ V		100		
B_1	Unity-gain bandwidth	$R_L = 600\ \Omega$,	$C_L = 100$ pF		10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB,	$R_L = 600\ \Omega$, f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm9$ V to ±15 V, $V_O = 0$		80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply current	No load,	$V_O = 0$		8	16	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$V_{o1} = 10$ V peak,	f = 1 kHz		110		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

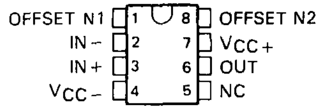
PARAMETER		TEST CONDITIONS	NE5532			NE5532A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/ms
	Overshoot factor	$V_I = 100$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_L = 100$ pF		10%			10%		
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	$nV/\sqrt{Hz}$
		f = [illegible]		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		$pA/\sqrt{Hz}$
		f = 1 kHz		0.7			0.7		

ULTRA-LOW-OFFSET-VOLTAGE OPERATIONAL AMPLIFIERS

D2757, OCTOBER 1983—REVISED JUNE 1988

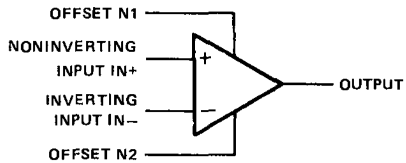
- Ultra-Low Offset Voltage . . .30 μV Typ (OP-07E)
- Ultra-Low Offset Voltage Temperature Coefficient . . . 0.3 μV/°C Typ (OP-07E)
- Ultra-Low Noise
- No External Components Required
- Replaces Chopper Amplifiers at a Lower Cost
- Single-Chip Monolithic Fabrication
- Wide Input Voltage Range 0 to ±14 V Typ
- Wide Supply Voltage Range ±3 V to ±18 V
- Essentially Equivalent to Fairchild μA714 Operational Amplifiers
- Direct Replacement for PMI OP-07C, OP-07D, OP-07E

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



2

Operational Amplifiers

description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP-07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

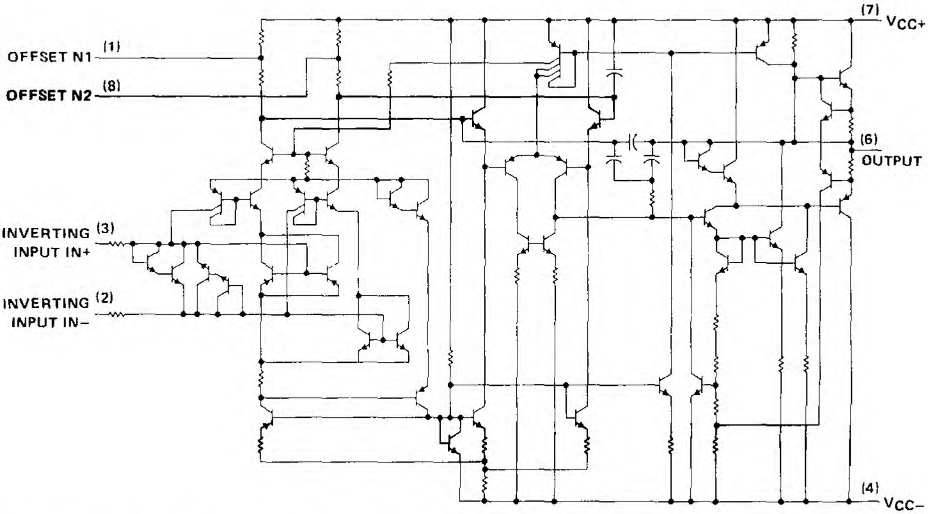
T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	150 μV	OP-07CD OP-07DD	OP-07CJG OP-07DJG	OP-07CP OP-07DP
	75 μV	OP-07ED	OP-07EJG	OP-07EP

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., OP-07CDR)

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	22 V
Supply voltage V_{CC-}	−22 V
Differential input voltage (see Note 2)	±30 V
Input voltage (either input, see Note 3)	±22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		OP-7C MIN	OP-7C TYP	OP-7C MAX	OP-7D MIN	OP-7D TYP	OP-7D MAX	OP-7E MIN	OP-7E TYP	OP-7E MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		60	150		60	150		30	75	μV
			0°C to 70°C		85	250		85	250		45	130	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5		0.3	1.3	μV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5			0.3		μV/mo
	Offset adjustment range	$R_S = 20$ kΩ, See Figure 1	25°C		±4			±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6		0.5	3.8	nA
			0°C to 70°C		1.6	8		1.6	8		0.9	5.3	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50		8	35	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12		±1.2	±4	nA
			0°C to 70°C		±2.2	±9		±3	±14		±1.5	±5.5	
α_{IIB}	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50		13	35	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13	±14		±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \ge 10$ kΩ	25°C	±12	±13		±12	±13		±12.5	±13		V
		$R_L \ge 2$ kΩ		±11.5	±12.8		±11.5	±12.8		±12	±12.8		
		$R_L \ge 1$ kΩ			±12			±12		±10.5	±12		
		$R_L \ge 2$ kΩ	0°C to 70°C	±11	±12.6		±11	±12.6		±12	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 3$ V, $V_O = \pm 0.5$ V, $R_L \ge 500$ kΩ	25°C	100	400			400		150	400		V/mV
		$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	120	400		120	400					
			0°C to 70°C	100	400		100	400		[illegible]	[illegible]		
B_1	Unity gain bandwidth		25°C	0.4	0.6		0.4	0.6		0.4	0.6		MHz
r_i	Input resistance		25°C	8	33		7	31		15	50		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 13$ V, $R_S = 50\ \Omega$	25°C	100	120		94	110		106	123		dB
			0°C to 70°C	97	120		94	106		103	123		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm 3$ V to ± 18 V, $R_S = 50\ \Omega$	25°C		7	32		7	32		5	20	μV/V
			0°C to 70°C		10	51		10	51		7	32	
P_D	Power dissipation	$V_O = 0$, No load	25°C		80	150		80	150		75	120	mW
		$V_{CC\pm} = \pm 3$ V, $V_O = 0$, No load			4	8		4	8		4	6	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6 Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		OP-7C MIN	OP-7C TYP	OP-7C MAX	OP-7D MIN	OP-7D TYP	OP-7D MAX	OP-7E MIN	OP-7E TYP	OP-7E MAX	UNIT
V_n	Equivalent input noise voltage	$T_A = 25°C$	f = 10 Hz		10.5			10.5			10.3		nV/√Hz
			f = 100 Hz		10.2			10.3			10.0		
			f = 1 kHz		9.8			9.8			9.6		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, $T_A = 25°C$			0.38			0.38			0.35		μV
I_n	Equivalent input noise current	$T_A = 25°C$	f = 10 Hz		0.35			0.35			0.32		pA/√Hz
			f = 100 Hz		0.15			0.15			0.14		
			f = 1 kHz		0.13			0.13			0.12		
I_{NPP}	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz, $T_A = 25°C$			15			15			14		pA
SR	Slew rate	$R_L \geq 2$ kΩ, $T_A = 25°C$			0.3			0.3			0.3		V/μs

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

TYPICAL APPLICATION DATA

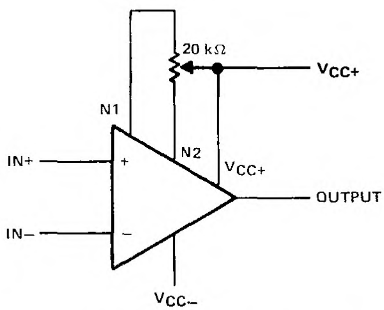


FIGURE 1. INPUT OFFSET VOLTAGE NULL CIRCUIT

D3176, FEBRUARY 1989

- **Direct Replacements for PMI and LTC OP-27 and OP-37 Series**

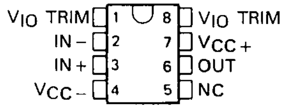
Features of OP-27A, OP-27C, OP-37A, and OP-37C:

- **Maximum Equivalent Input Noise Voltage:**
  3.8 nV/√Hz at 1 kHz
  5.5 nV/√Hz at 10 Hz
- **Very Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 80 nV Typ**
- **Low Input Offset Voltage . . . 25 μV Max**
- **High Voltage Amplification . . . 1 V/μV Min**

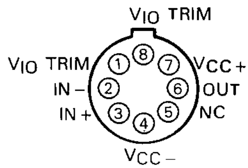
Feature of OP-37 Series:

- **Minimum Slew Rate . . . 11 V/μs**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



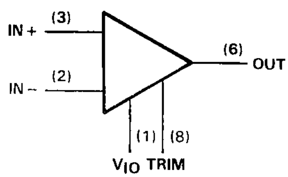
NC—No internal connection

description

The OP-27 and OP-37 operational amplifiers combine outstanding noise performance with excellent precision and high-speed specifications. The wideband noise is only 3 nV/√Hz, and with the 1/f noise corner at 2.7 Hz, low noise is maintained for all low-frequency applications.

The outstanding characteristics of the OP-27 and OP-37 make these devices excellent choices for low-noise amplifier applications requiring precision performance and reliability. Additionally, the OP-37 is free of latch-up in high-gain, large-capacitive-feedback configurations.

symbol



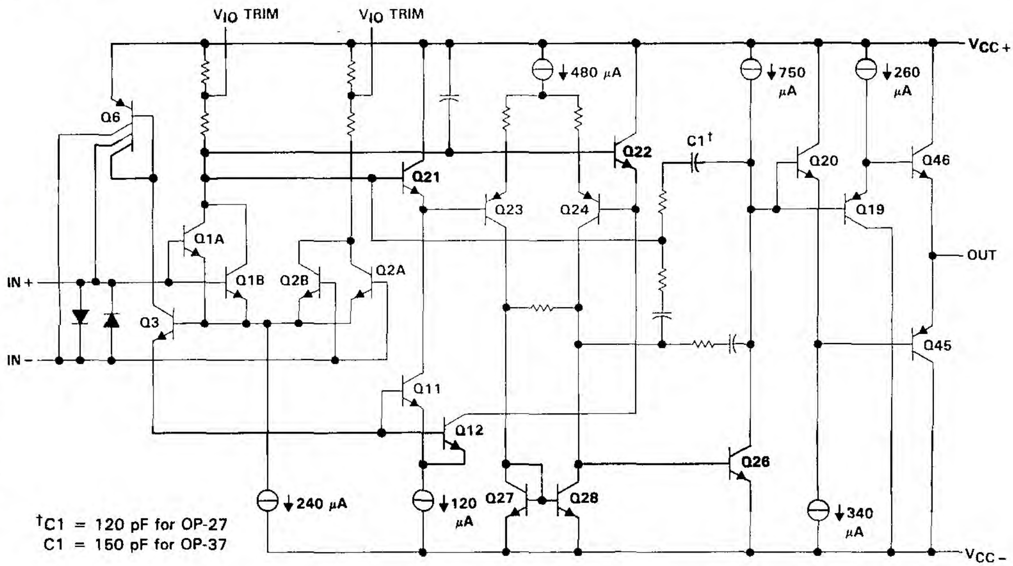
The OP-27 series is compensated for unity gain. The OP-37 series is decompensated for increased bandwidth and slew rate and is stable down to a gain of 5.

The OP-27A, OP-27C, OP-37A, and OP-37C are characterized for operation over the full military temperature range of −55°C to 125°C. The OP-27E, OP-27G, OP-37E, and OP-37G are characterized for operation from −25°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	STABLE GAIN	PACKAGE		
			CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
−25°C to 85°C	25 μV	1	OP27EJG	O [illegible]	OP27EP
		5	OP37EJG	O [illegible]	OP37EP
	100 μV	1	OP27GJG	OP27GL	OP27GP
		5	OP37GJG	OP37GL	OP37GP
−55°C to 125°C	25 μV	1	OP27AJG	OP27AL	OP27AP
		5	OP37AJG	OP37AL	OP37AP
	100 μV	1	OP2[illegible]	OP27CL	OP27CP
		5	OP3[illegible]	OP37CL	OP37CP

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 22 V
Supply voltage, V_{CC-} (see Note 1) . . . . −22 V
Input voltage . . . . $V_{CC\pm}$
Duration of output short circuit . . . . unlimited
Differential input current (see Note 2) . . . . ±25 mA
Continuous power dissipation . . . . see Dissipation Rating Table
Operating free-air temperature range: OP-27A, OP-27C, OP-37A, OP-37C . . . . . . −55°C to 125°C
OP-27E, OP-27G, OP-37E, OP-37G . . . . −25°C to 85°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . 260°C

NOTES: 1. All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} unless otherwise noted.
2. The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG (OP-27A, OP-27C, OP-37A, OP-37C)	1050 mW	8.4 mW/°C	546 mW	210 mW
JG (OP-27E, OP-27G, OP-37E, OP-37G)	825 mW	6.6 mW/°C	429 mW	N/A
L (OP-27A, OP-27C, OP-37A, OP-37C)	825 mW	6.6 mW/°C	429 mW	165 mW
L (OP-27E, OP-27G, OP-37E, OP-37G)	650 mW	5.2 mW/°C	338 mW	N/A
P	1000 mW	8.0 mW/°C	520 mW	N/A

recommended operating conditions

		OP-27A, OP-37A			OP-27C, OP-37C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Common-mode input voltage, V_{ICR}	$V_{CC\pm} = \pm 15$ V, $T_A = 25°C$			±11			±11	V
	$V_{CC\pm} = \pm 15$ V, $T_A = -55°C$ to 125°C			±10.3			±10.2	
Operating free-air temperature, T_A		−55		125	−55		[illegible]	°C

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP-27A, OP-37A			OP-27C, OP-37C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$	25°C		10	[illegible]		30	100	μV
		$R_S = 50\ \Omega$, See Note 3	−55°C to 125°C			60			300	
αV_{IO}	Average temperature coefficient of input offset voltage		−55°C to 125°C		0.2	0.6		0.4	1.8	μV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$	25°C		7	35		12	75	nA
			−55°C to 125°C			50			135	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$	25°C		±10	±40		±15	±80	nA
			−55°C to 125°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−55°C to 125°C	±10.3			±10.2			
V_{OM}	Peak output voltage swing	$R_L \geq 2$ kΩ	25°C	±12	±13.8		±11.5	±13.5		V
		$R_L \geq 0.6$ kΩ		±10	±11.5		±10	±11.5		
		$R_L \geq 2$ kΩ	−55°C to 125°C	±11.5			±10.5			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	[illegible]	[illegible]		700	[illegible]		V/mV
		$R_L \geq 1$ kΩ, $V_O = \pm 10$ V		[illegible]	[illegible]			[illegible]		
		$R_L \geq 0.6$ kΩ, $V_O = \pm 1$ V, $V_{CC} = \pm 4$ V		250	700		200	500		
		$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	−55°C to 125°C	600			300			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	$V_O = 0$, $I_O = 0$	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 11$ V	25°C	114	126		100	120		dB
		$V_{IC} = \pm 10$ V	−55°C to 125°C	108			94			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm} = \pm 4$ V to ±18 V	[illegible]	100	120		94	118		dB
		$V_{CC\pm} = \pm 4.5$ V to ±18 V	−55°C to 125°C	96			86			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV. See Figure 3.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	V
Common-mode input voltage, range	$V_{CC\pm} = \pm 15$ V, $T_A = 25°C$			±11	V
	$V_{CC\pm} = \pm 15$ V, $T_A = -55°C$ to 125°C			±[illegible]	V
Operating free-air temperature, T_A		−25		85	°C

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP-27E, OP-37E			OP-27G, OP-37G			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$ $R_S = 50\ \Omega$, See Note 3	25°C		10	25		30	100	µV
			−25°C to 85°C			50			220	
αV_{IO}	Average temperature coefficient of input offset voltage		−25°C to 85°C		0.2	0.6		0.4	1.8	µV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$	25°C		7	35		12	75	nA
			−25°C to 85°C			50			135	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$	25°C		±10	±40		±15	±80	nA
			−25°C to 85°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−25°C to 85°C	±10.5			±10.5			
V_{OM}	Peak output voltage swing	$R_L \geq 2$ kΩ	25°C	±12	±13.8		±11.5	±13.5		V
		$R_L \geq 0.6$ kΩ	25°C	±10	±11.5		±10	±11.5		
		$R_L \geq 2$ kΩ	−25°C to 85°C	±11.7			±11			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	[illegible]	[illegible]		700	[illegible]		V/mV
		$R_L \geq 1$ kΩ, $V_O = \pm 10$ V	25°C	[illegible]	[illegible]					
		$R_L \geq 0.6$ kΩ, $V_O = \pm 1$ V, $V_{CC} = \pm 4$ V	25°C	250	700		200	500		
		$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	−25°C to 85°C	750			450			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	$V_O = 0$, $I_O = 0$	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 11$ V	25°C	114	[illegible]		[illegible]	120		dB
		$V_{IC} = \pm 10$ V	−25°C to 85°C	110			[illegible]			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm} = \pm 4$ V to ±18 V	25°C	100	120		94	118		dB
		$V_{CC\pm} = \pm 4.5$ V to ±18 V	−25°C to 85°C	97			90			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 µV. See Figure 3.

OP-27 operating characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	OP-27A, OP-27E			OP-27C, OP-27G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 1$, $R_L \geq 2$ kΩ	1.7	2.8		1.7	2.8		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, RS = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω,		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 100 kHz	5	8		5	8		MHz

OP-37 operating characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	OP-37A, OP-37E			OP-37C, OP-37G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 5$, $R_L \geq 2$ kΩ	11	17		11	17		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, R_S = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 10 kHz	45	63		45	63		MHz
		$A_V \geq 5$, f = 1 MHz		40			40		

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power-on	2
		vs Time (long-term drift)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{ICR}	Common-mode input voltage range	vs Supply voltage	6
V_{OM}	Maximum peak output voltage	vs Load resistance	7
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	8, 9
A_{VD}	Differential voltage amplification	vs Supply voltage	10
		vs Load resistance	11
		vs Frequency	12, 13, 14
CMRR	Common-mode rejection ratio	vs Frequency	15
k_{SVR}	Supply voltage rejection ratio	vs Frequency	16
SR	Slew rate	vs Temperature	17
		vs Supply voltage	18
		vs Load resistance	19
ϕ_m	Phase margin	vs Temperature	20, 21
ϕ	Phase shift	vs Frequency	12, 13
V_n	Equivalent input noise voltage	vs Bandwidth	22
		vs Source resistance	23
		vs Supply voltage	24
		vs Temperature	25
		vs Frequency	26
I_n	Equivalent input noise current	vs Frequency	27
GBW	Gain bandwidth product	vs Temperature	20, 21
I_{OS}	Short-circuit output current	vs Time	28
I_{CC}	Supply current	vs Supply voltage	29
	Pulse response	Small-signal	30, 32
		Large-signal	31, 33

TYPICAL CHARACTERISITCS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNIT
vs
FREE-AIR TEMPERATURE

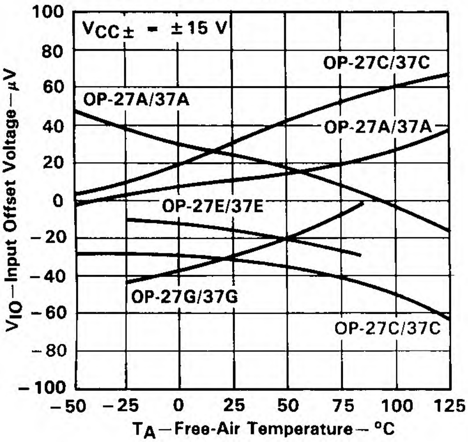


FIGURE 1

WARM-UP CHANGE IN
INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

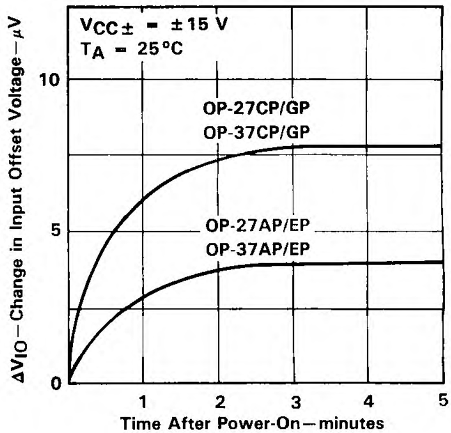


FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

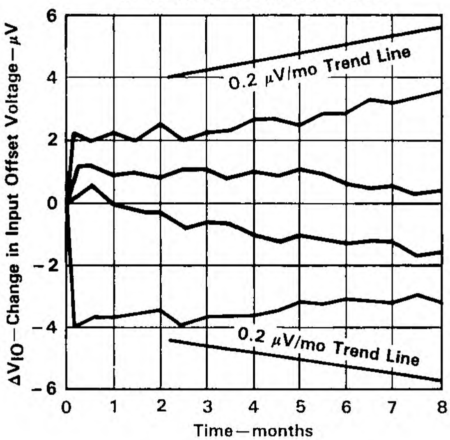


FIGURE 3

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

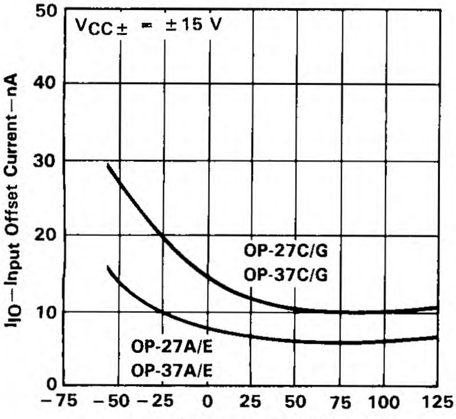


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

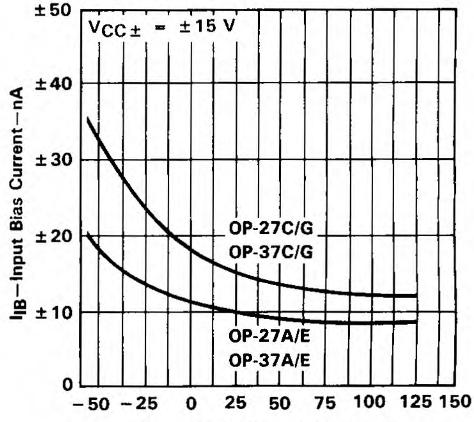


FIGURE 5

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs SUPPLY VOLTAGE

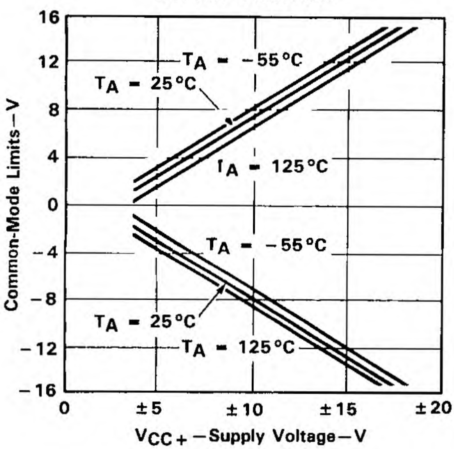


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

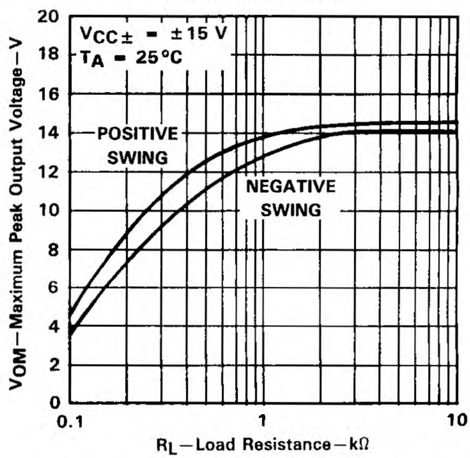


FIGURE 7

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS

OP-27
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

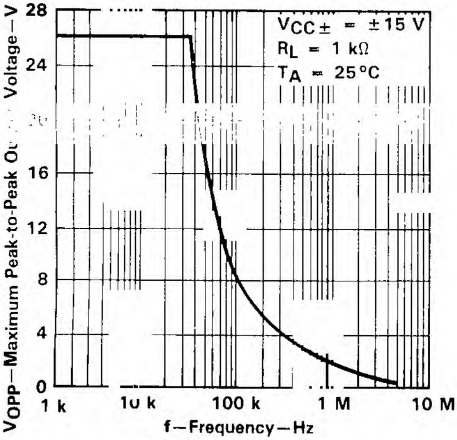


FIGURE 8

OP-37
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

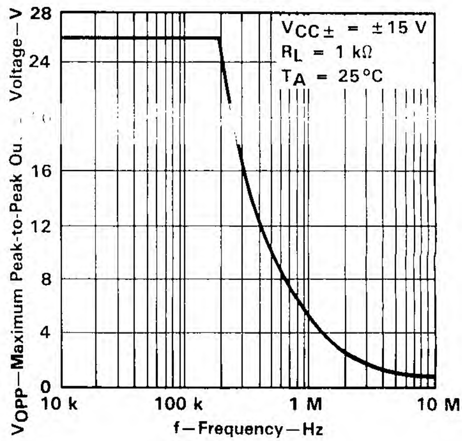


FIGURE 9

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
TOTAL SUPPLY VOLTAGE

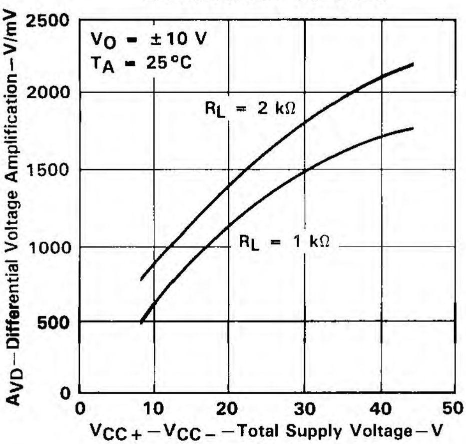


FIGURE 10

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

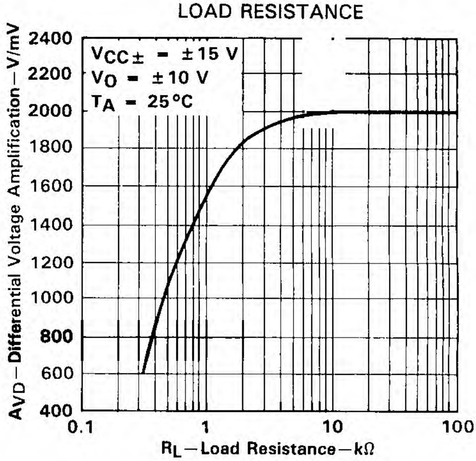


FIGURE 11

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

OP-27
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

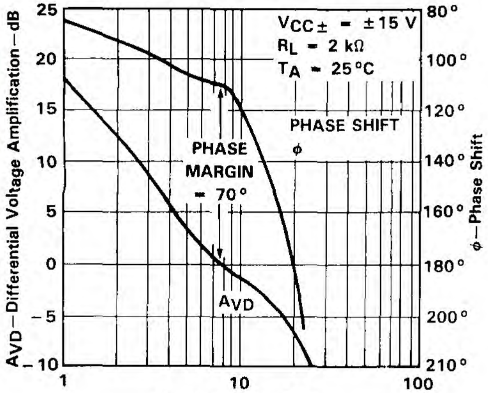


FIGURE 12

OP-37
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

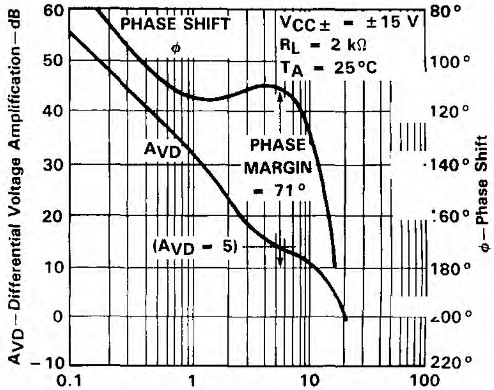


FIGURE 13

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

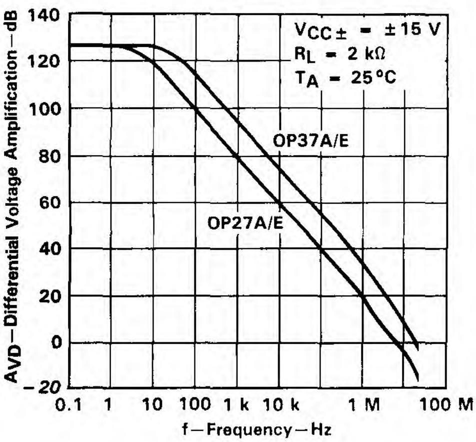


FIGURE 14

OP-27A, OP-27E, OP-37A, OP-37E
COMMON-MODE REJECTION RATIO vs FREQUENCY

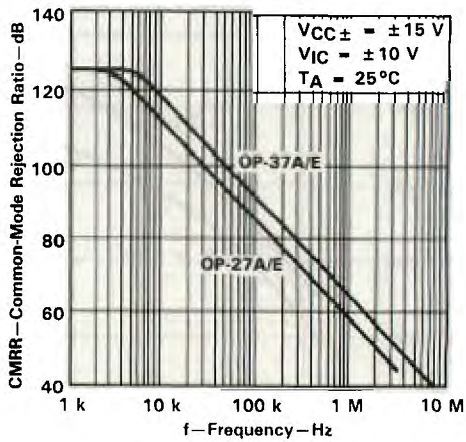


FIGURE 15

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TYPICAL CHARACTERISTICS†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

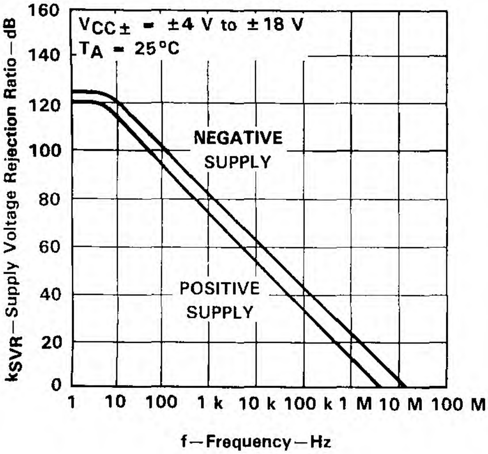


FIGURE 16

SLEW RATE
vs
FREE-AIR TEMPERATURE

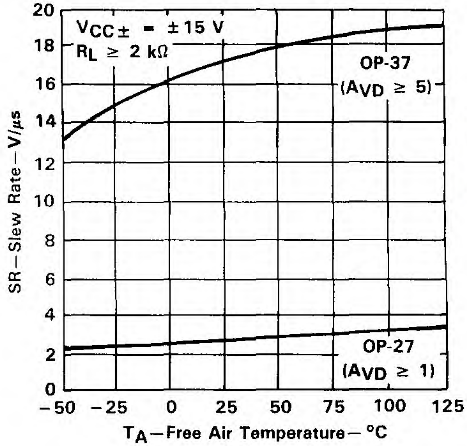


FIGURE 17

OP-37
SLEW RATE
vs
SUPPLY VOLTAGE

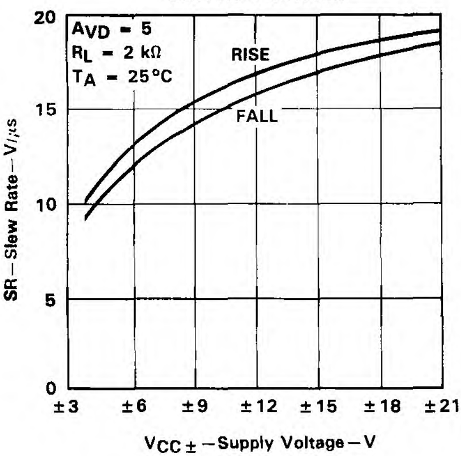


FIGURE 18

OP-37
SLEW RATE
vs
LOAD RESISTANCE

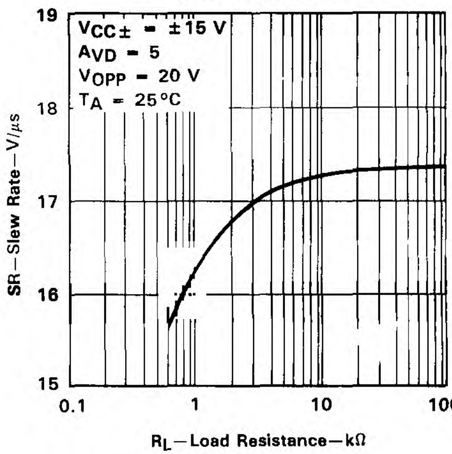


FIGURE 19

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

OP-27
PHASE MARGIN AND
GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

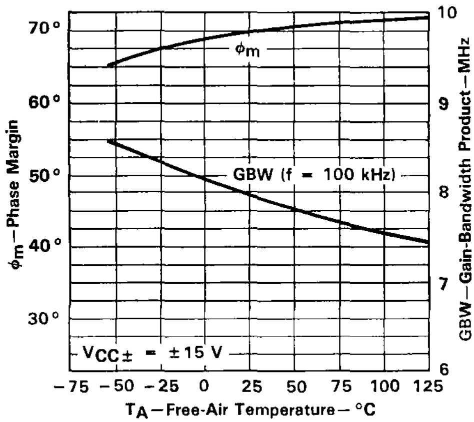


FIGURE 20

OP-37
PHASE MAGIN AND
GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

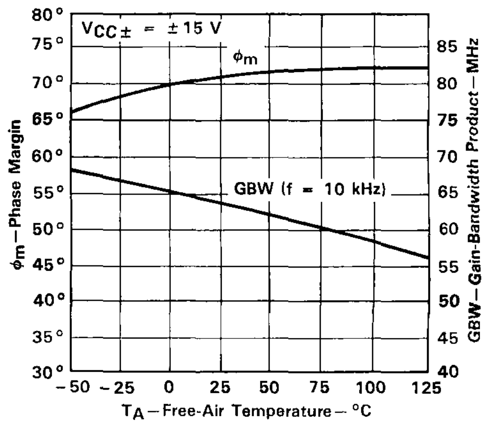


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
vs
BANDWIDTH

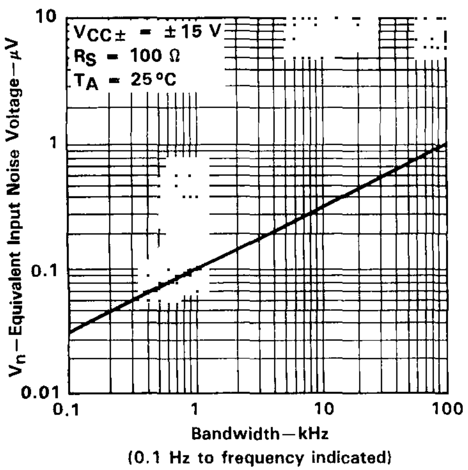


FIGURE 22

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

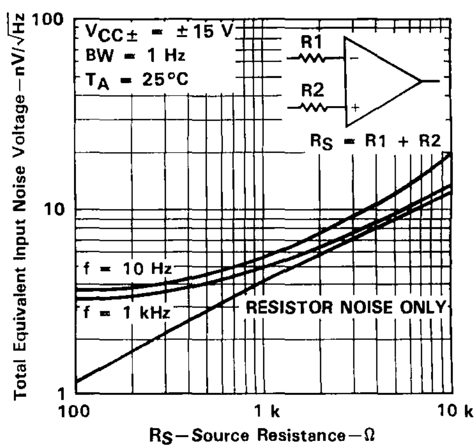


FIGURE 23

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
TOTAL SUPPLY VOLTAGE

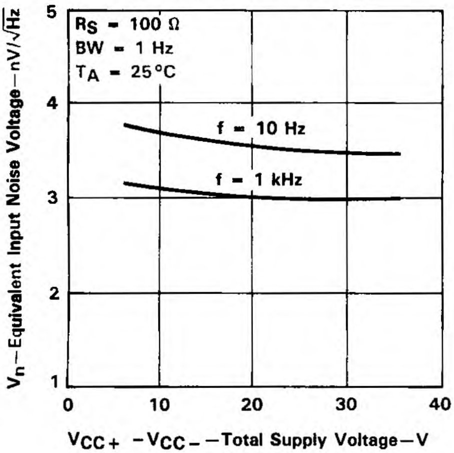


FIGURE 24

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREE-AIR TEMPERATURE

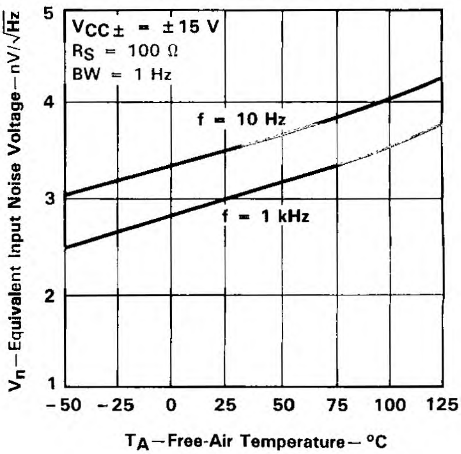


FIGURE 25

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

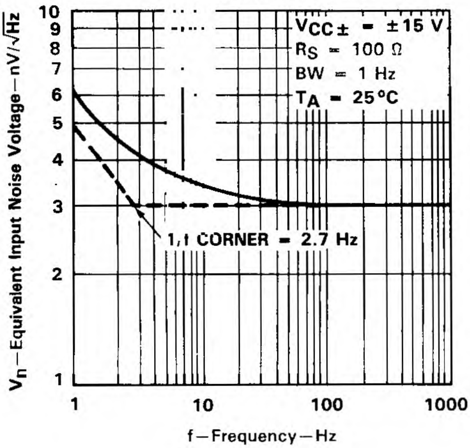


FIGURE 26

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

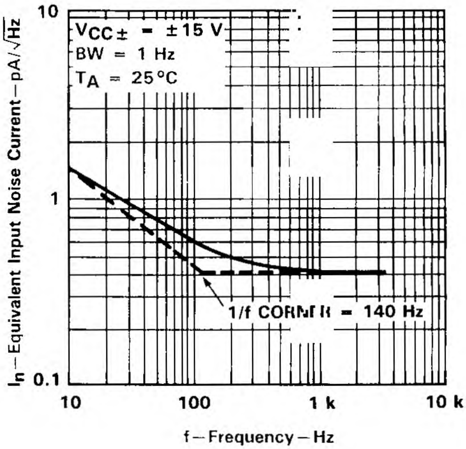


FIGURE 27

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

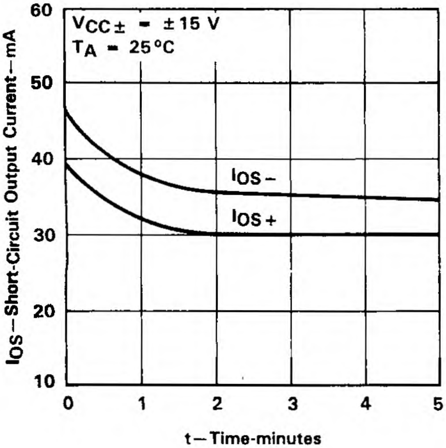


FIGURE 28

SUPPLY CURRENT
vs
TOTAL SUPPLY VOLTAGE

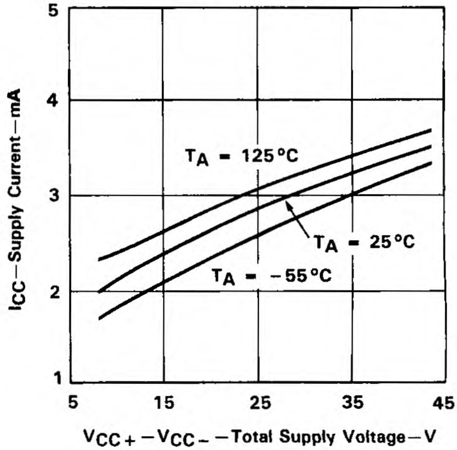


FIGURE 29

OP-27
VOLTAGE FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

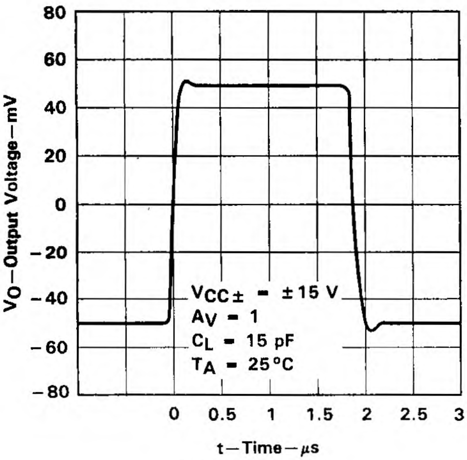


FIGURE 30

OP-27
VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

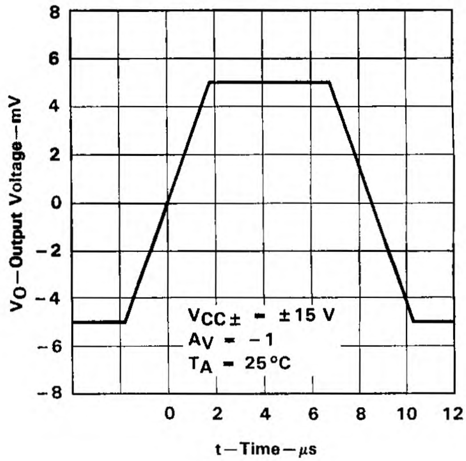


FIGURE 31

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS

OP-37
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

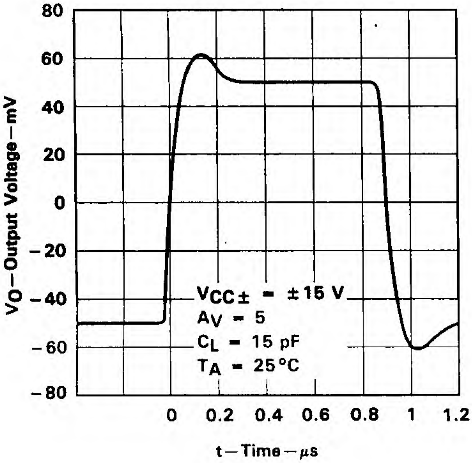


FIGURE 32

OP-37
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

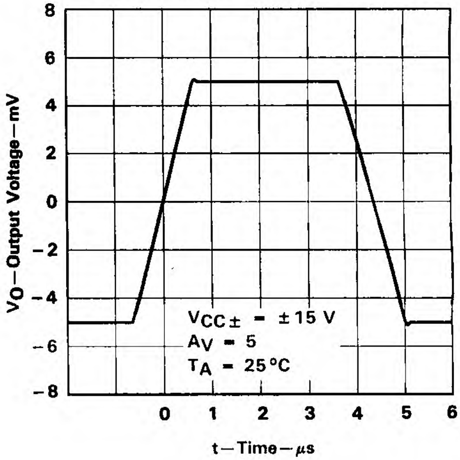


FIGURE 33

TYPICAL APPLICATION DATA

general

The OP-27 and OP-37 series devices may be inserted directly into OP-07, OP-05, μA725, and SE5534 sockets with or without removing external compensation or nulling components. In addition, the OP-27 and OP-37 may be fitted to μA741 sockets by removing or modifying external nulling components.

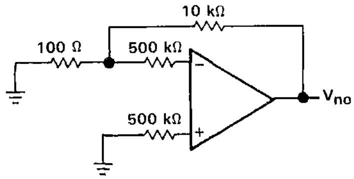
noise testing

Figure 34 shows a test curcuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the OP-27 and OP-37. The frequency response of this noise tester indicates that the 0.1-Hz corner is defined by only one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.

TYPICAL APPLICATION DATA

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement correlates well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 35 shows a circuit measuring current noise and the formula for calculating current noise.



$$I_n = \frac{[V_{no}^2 - (130\ \text{nV})^2]^{1/2}}{1\ \text{M}\Omega \times 100}$$

FIGURE 35. CURRENT NOISE TEST CIRCUIT AND FORMULA

offset voltage adjustment

The input offset voltage and temperature coefficient of the OP-27 and OP-37 are permanently trimmed to a low level at wafer testing. However, if further adjustment of V_{IO} is necessary, using a 10-kΩ nulling potentiometer, as shown in Figure 36, does not degrade the temperature coefficient $\alpha_{V_{IO}}$. Trimming to a value other than zero creates an $\alpha_{V_{IO}}$ of V_{IO}/300 μV/°C. For example, if V_{IO} is adjusted to 300 μV, the change in $\alpha_{V_{IO}}$ is 1 μV/°C.

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be inproved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 37 has an approximate null range of ±200 μV.

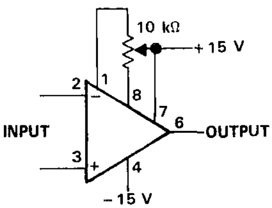


FIGURE 36. STANDARD INPUT OFFSET VOLTAGE ADJUSTMENT

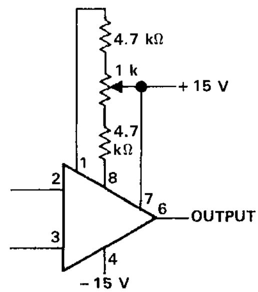


FIGURE 37. INPUT OFFSET VOLTAGE ADJUSTMENT WITH IMPROVED SENSITIVITY

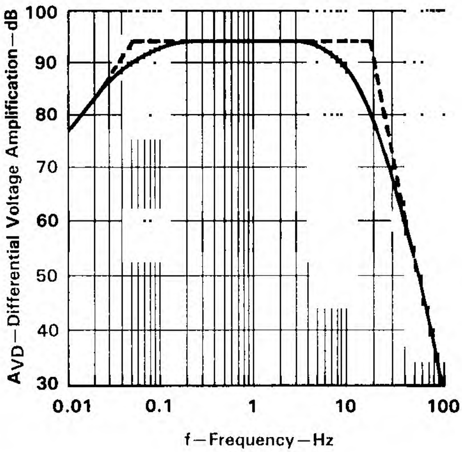
offset voltage and drift

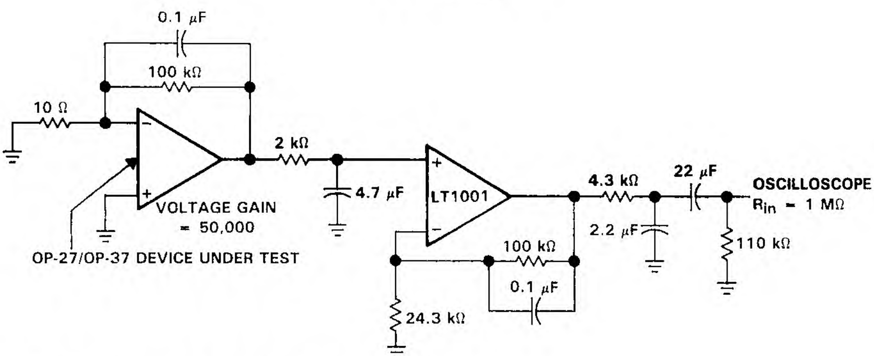
Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent temperature coefficient $\alpha_{V_{IO}}$ of the amplifier. Air currents should be minimized, package leads should be short, and the two input leads should be close together and at the same temperature.

The circuit shown in Figure 38 measures offset voltage. This circuit can also be used as the burn-in configuration for the OP-27 and OP-37, with the supply voltage increased to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, and A_{VD} = 100.

TYPICAL APPLICATION DATA

noise testing (continued)





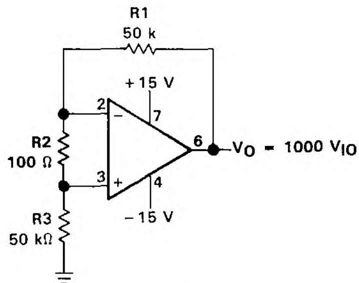
NOTE: All capacitor values are for non-polarized capacitors only.

FIGURE 34. 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE TEST CIRCUIT AND FREQUENCY RESPONSE

Measuring the typical 80-nV peak-to-peak noise performance of the OP-27 and OP-37 requires the following special test precautions:

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 4 μV due to the chip temperature increasing from 10 °C to 20 °C starting from the moment the power supplies are turned on. In the 10-s measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. For similar reasons, the device should be well shielded from air currents to eliminate the possiblity of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
3. Sudden motion in the vicinity of the device should be avoided, as it produces a feedthrough effect that increases observed noise.

TYPICAL APPLICATION DATA



NOTE Resistors must have low thermoelectric potential.

FIGURE 38. TEST CIRCUIT FOR OFFSET VOLTAGE AND OFFSET VOLTAGE TEMPERATURE COEFFICIENT

unity gain buffer applications

The resulting output waveform when $R_f \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (> 1 V) is shown in the pulsed-operation diagram in Figure 39.

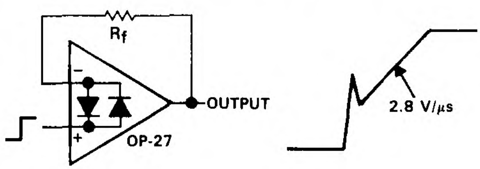


FIGURE 39. PULSED OPERATION

During the initial (fast-feedthrough-like) portion of the output waveform, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements (load current ≤ 20 mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs. When $R_f > 2\ k\Omega$, a pole is created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f eliminates this problem.

TEXAS INSTRUMENTS
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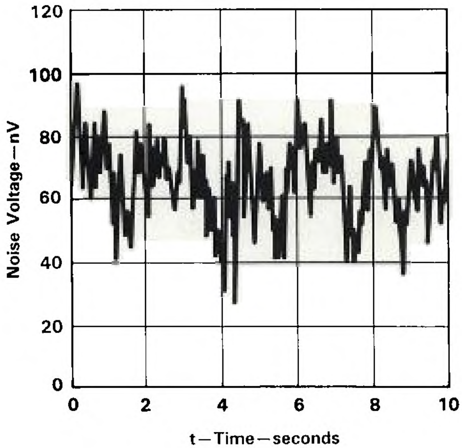
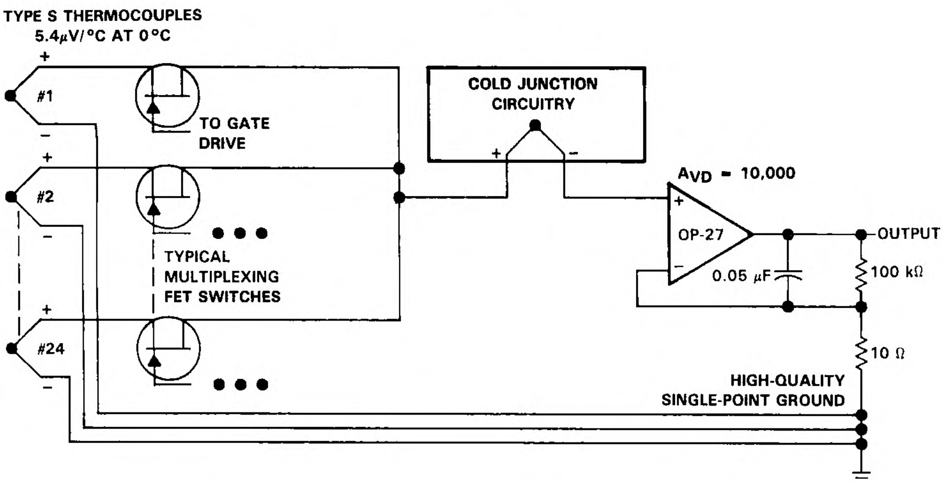
TYPICAL APPLICATION





NOTE A: If 24 channels are multiplexed per second, and the output is required to settle to 0.1% accuracy, the amplifier's bandwidth cannot be limited to less than 30 Hz. The peak-to-peak noise contribution of the OP-27 will still be only 0.11 μV, which is equivalent to an error of only 0.02°C.

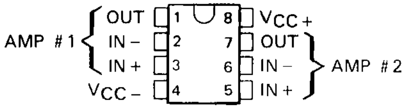
FIGURE 40. LOW-NOISE, MULTIPLEXED THERMOCOUPLE AMPLIFIER AND 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE

DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

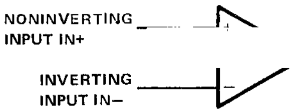
D2785, OC 983–REVISED JUNE 1988

- Matched Gain and Offset Between Amplifiers
- Unity-Gain Bandwidth . . . 3 MHz Min
- Slew Rate . . . 1.5 V/ns Min
- Low Equivalent Input Noise Voltage . . . 2 μV/√Hz Max (20 Hz to 20 kHz)
- No Frequency Compensation Required
- No Latch Up
- Wide Common-Mode Voltage Range
- Low Power Consumption
- Designed to be Interchangeable with Raytheon RC4559

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
RC4559	D,P	−0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e.,RC4559DR)

description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . 18 V
Supply voltage V_{CC-} (see Note 1) . . . . −18 V
Differential input voltage (see Note 2) . . . . ±30 V
Input voltage (any input, see Notes 1 and 3) . . . . ±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4) . . . . unlimited
Continuous total dissipation . . . . 500 mW
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	6	mV
			0°C to 70°C			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	nA
			0°C to 70°C			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		40	[illegible]	nA
			0°C to 70°C			[illegible]	
V_I	Input voltage range		25°C	±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L \geq 3$ kΩ	25°C	±12	±13		V
		$R_L = 600$ Ω	25°C	±9.5	±10		
		$R_L \geq 2$ kΩ	0°C to 70°C	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 2$ kΩ	25°C	20	[illegible]		V/mV
			0°C to 70°C	15			
B_{OM}	Maximum output-swing bandwidth	$V_{OPP} = 20$ V, $R_L = 2$ kΩ	25°C	24	32		kHz
B_1	Unity-gain bandwidth		25°C	3	4		[illegible]
r_i	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$	25°C	80	100		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_O = 0$	25°C		10	75	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 20 Hz to 20 kHz	25°C		1.4	2	μV
I_n	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		pA
I_{CC}	Supply current (both amplifiers)	No load, No signal	25°C		3.3	5.6	mA
			0°C		4	6.6	
			70°C		3	5	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 10 kHz	25°C		90		dB
			25°C		90		

† All characteristics are specified under open-loop operation, unless otherwise noted.

matching characteristics at $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$		±0.2		[illegible]
I_{IO}	Input offset current	$V_O = 0$		±7.5		nA
I_{IB}	Input bias current	$V_O = 0$		±15		nA
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 2$ kΩ		±1		dB

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

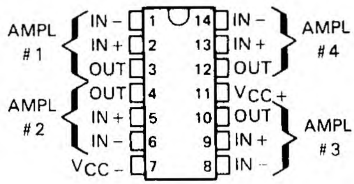
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		80		μs
	Overshoot	$C_L = 100$ pF		18%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF	1.5	2		V/μs

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

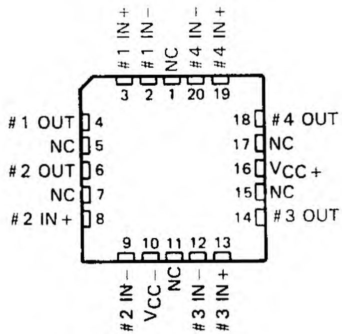
D2142, MARCH 1978—REVISED NOVEMBER 1988

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Designed to be Interchangeable with Raytheon RM4136, RV4136, and RC4136**
- Low Noise . . . 8 nV/$\sqrt{Hz}$ Typ at 1 kHz

RM4136 . . . J OR W PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGE
(TOP VIEW)



RM4136
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

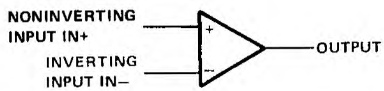
description

The RM4136, RV4136, and RC4136 are quad high-performance operational amplifiers with each amplifier electrically similar to the uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4136 is characterized for operation over the full military temperature range of −55°C to 125°C, the RV4136 is characterized for operation from −40°C to 85°C, and the RC4136 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

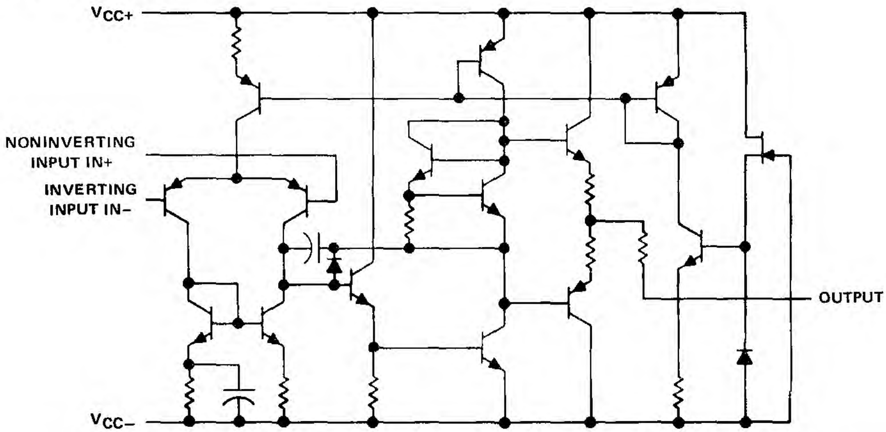


AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT (W)
0°C to 70°C	6 mV	RC4136D	—	RC4136J	RC4136N	—
−40°C to 85°C	6 mV	RV4136D	—	RV4136J	RV4136N	—
−55°C to 125°C	4 mV	—	RM4136FK	RM4136J	—	RM4136W

The D packages are available taped and reeled. Add the suffix R to the device type. (e.g., RC4136DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4136	RV4136	RC4136	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation [illegible]			
Operating free-air temperature range		−55 to 125	−40 to 85	[illegible] 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	494 mW	–
FK	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J (RM4136)	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J (others)	800 mW	8.2 mW/°C	52°C	656 mW	533 mW	–
N	800 mW	9.2 mW/°C	63°C	736 mW	598 mW	–
W	800 mW	8.0 mW/°C	50°C	640 mW	520 mW	200 mW

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		RM4136			RV4136			RC4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.5	4		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	150		5	200		5	200	nA
			Full range			500			500			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		140	400		140	500		140	500	nA
			Full range			1500			1500			800	
V_I	Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	350		20	300		20	300		V/mV
			Full range	25			15			15			
B_1	Unity-gain bandwidth		25°C		3.5			3			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50$ Ω	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$	25°C		30	150		30	150		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, BW = 1 Hz, f = 1 kHz, $R_S = 100$ Ω	25°C		8			8			8		nV/$\sqrt{Hz}$
I_{CC}	Supply current (All four amplifiers)	$V_O = 0$, No load	25°C		5	11.3		5	11.3		5	11.3	mA
			MIN T_A		6	13.3		6	13.7		6	13.7	
			MAX T_A		4.5	10		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)	$V_O = 0$, No load	25°C		150	340		150	340		150	340	mW
			MIN T_A		180	400		180	400		180	400	
			MAX T_A		135	300		135	300		135	300	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, f = 10 kHz, $R_S = 1$ kΩ	25°C		105			105			105		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for RM4136, −40°C to 85°C for RV4136, and 0°C to 70°C for RC4136.

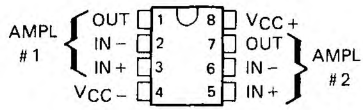
operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		RM4136			RV4136, RC4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		0.13			0.13		µs
	Overshoot factor	$C_L = 100$ pF			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF	$R_L = 2$ kΩ,		1.7			1.7		V/µs

D2141, MARCH 1976—REVISED DECEMBER 1988

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Unity Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers
- Low Noise . . . 8 nV/$\sqrt{Hz}$ Typ at 1 kHz
- Designed to be Interchangeable with Raytheon RM4558, RV4558, and RC4558

D, JG, OR P PACKAGE
(TOP VIEW)



description

The RM4558, RV4558, and RC4558 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

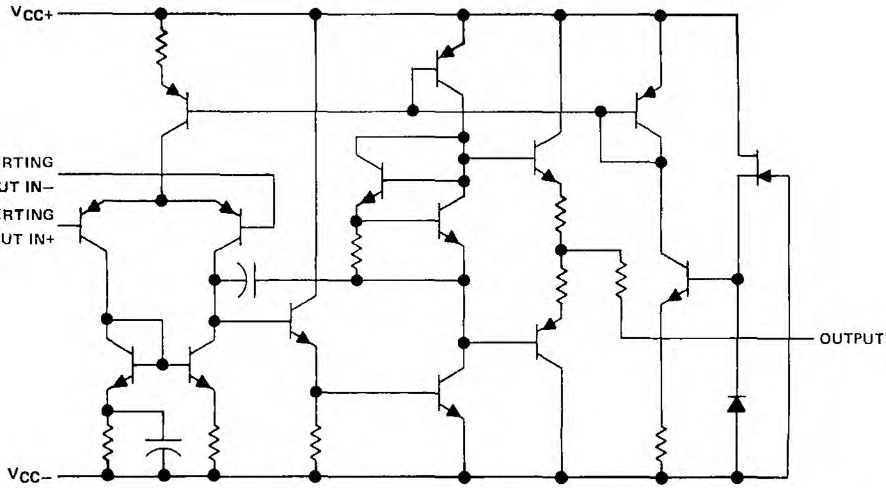
The RM4558 is characterized for operation over the full military temperature range of −55°C to 125°C, the RV4558 is characterized for operation from −40°C to 85°C, and the RC4558 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGES		
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	6 mV	RC4558D	RC4558JG	RC4558P
−40°C to 85°C	6 mV	RV4558D	RV4558JG	RV4558P
−55°C to 125°C	5 mV	—	RM4558JG	—

The D packages are available taped and reeled. Add the suffix "R" to the device type (e.g., RC4558DR).

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	RM4558	RV4558	RC4558	UNIT
Supply voltage V_{CC+} (see Note 1)	22	18	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−18	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	[illegible] mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
JG (RM4558)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (RV4558) (RC4558)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		RM4558			RV4558			RC4558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.5	5		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	200		5	200		5	[illegible]	nA
			Full [illegible]			[illegible]			[illegible]			[illegible]	
I_{IB}	Input bias current	$V_O = 0$	[illegible]		140	[illegible]		140	[illegible]		150	[illegible]	nA
			Full range			1500			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum output voltage swing	$R_L = 10$ kΩ	25°	±12	±14		±12	±14		±12	±14		V
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full [illegible]	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ,	[illegible]	50	350		20	300		20	300		V/mV
		$V_O = \pm 10$ V	[illegible]	25			15			15			
B_1	Unity-gain bandwidth		[illegible]	2	3.5			3			3		[illegible]
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		[illegible]
CMRR	Common-mode rejection ratio		25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 15$ V to ± 9 V	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 100$ Ω, f = 1 kHz, BW = 1 Hz	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (Both amplifiers)	No load, $V_O = 0$	25°C		2.5	5.6		2.5	5.6		2.5	5.6	mA
			MIN T_A		3	6.6		3	6.6		3	6.6	
			MAX T_A		2	5		2.3	5		2.3	5	
P_D	Total power dissipation (Both amplifiers)	No load, $V_O = 0$	25°C		75	170		75	170		75	170	mW
			MIN T_A		90	200		90	200		90	200	
			MAX T_A		60	150		70	150		70	150	
V_{o1}/V_{o2}	Crosstalk attenuation — Open loop	$R_S = 1$ kΩ,	25°C		85			85			85		dB
	$A_{VD} =$ [illegible]	[illegible] = 10 kHz	25°C		[illegible]			105			105		

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for RM4558, −40°C to 85°C for RV4558, and 0°C to 70°C for RC4558.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

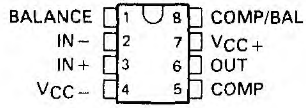
PARAMETER		TEST CONDITIONS	RM4558			RV4558			RC4558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		0.13			0.13			0.13		ns
	Overshoot	$C_L = 100$ pF		5%			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF	1.1	1.7		1.1	1.7		1.1	1.7		V/μs

2 Operational Amplifiers

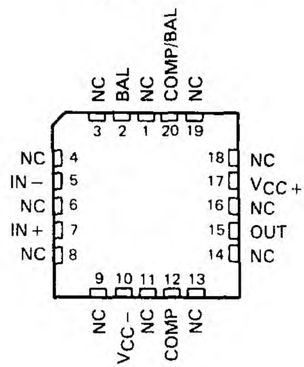
D2532, JULY 1979—REVISED MAY 1988

- Equivalent Input Noise Voltage 3.5 nV/$\sqrt{Hz}$ Typ
- Unity-Gain Bandwidth . . . . . . 10 MHz Typ
- Common-Mode Rejection Ratio 100 dB Typ
- High DC Voltage Gain . . . . 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 32 V Typ with $V_{CC\pm}$ = ±18 V and R_L = 600 Ω
- High Slew Rate . . . . 13 V/μs Typ
- Wide Supply Voltage Range ±3 V to ±20 V
- Low Harmonic Distortion
- Designed to be Interchangeable with Signetics SE5534, SE5534A, NE5534, and NE5534A

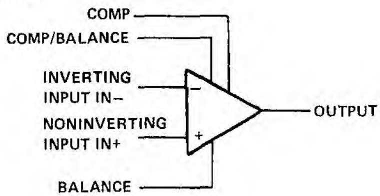
SE5534, SE5534A . . . JG PACKAGE
NE5534, NE5534A . . . D, JG OR P PACKAGE
(TOP VIEW)



SE5534, SE5534A
FK CHIP CARRIER PACKAGE
(TOP VIEW)



symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5534D	—	NE5534JG	NE5534P
		NE5534AD	—	NE5534AJG	NE5534AP
−55°C to 125°C	2 mV	—	SE5534FK	SE5534JG	—
		—	SE5534AFK	SE5534AJG	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., NE5534DR).

SE5534A FROM TI NOT RECOMMENDED FOR NEW DESIGNS

description

The SE5534, SE5534A, NE5534, and NE5534A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

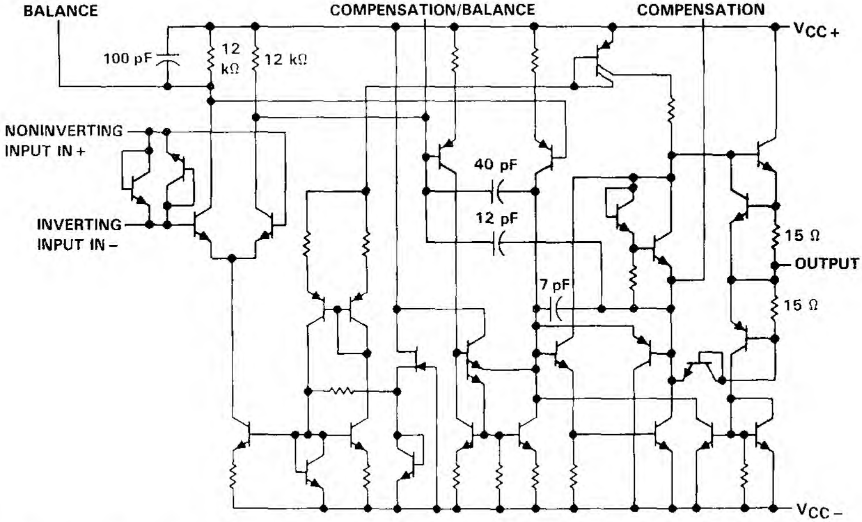
These operational amplifiers are internally compensated for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between pins 5 and 8. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability.

description (continued)

For the NE5534A, a maximum limit is specified for equivalent input noise voltage.

The SE5534 and SE5534A are characterized for operation over the full military temperature range of −55 °C to 125 °C; the NE5534 and NE5534A are characterized for operation from 0 °C to 70 °C.

schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage either input (see Notes 1 and 2)	V_{CC+}
Input current (see Note 3)	±10 mA
Duration of output short-circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: SE5534, SE5534A	−55 °C to 125 °C
NE5534, NE5534A	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C
Case temperature for 60 seconds: FK package	260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260 °C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
FK (see Note 5)	1375 mW	11.0 mW/°C	880 mW	275 mW
JG (SE5534__)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (NE5534__)	825 mW	6.6 mW/°C	528 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	N/A

NOTE 5: For the FK package, power rating and derating factor will vary with actual mounting technique used. The values stated here are believed to be conservative.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SE5534, SE5534A MIN	SE5534, SE5534A TYP	SE5534, SE5534A MAX	NE5534, NE5534A MIN	NE5534, NE5534A TYP	NE5534, NE5534A MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		0.5	2		0.5	4	mV
			T_A = full range			3			5	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		10	200		20	300	nA
			T_A = full range			500			400	
I_{IB}	Input bias current	$V_O = 0$	$T_A = 25°C$		400	800		500	1500	nA
			T_A = full range			1500			2000	
V_{ICR}	Common-mode input voltage range			±12	±13		±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 600\ \Omega$	$V_{CC\pm} = \pm 15$ V	24	26		24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		30	32		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 600\ \Omega$	$T_A = 25°C$	50	100		25	100		V/mV
			T_A = full range	25			15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	$C_C = 0$		6			6		V/mV
			$C_C = 22$ pF		2.2			2.2		
B_{OM}	Maximum-output-swing bandwidth	$V_O = \pm 10$ V,	$C_C = 0$		200			200		kHz
		$V_O = \pm 10$ V,	$C_C = 22$ pF		95			95		
		$V_{CC\pm} = \pm 18$ V, $R_L = 600\ \Omega$,	$V_O = \pm 14$ V, $C_C = 22$ pF		70			70		
B_1	Unity-gain bandwidth	$C_C = 22$ pF,	$C_L = 100$ pF		10			10		MHz
r_i	Input resistance			50	100		30	100		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB, $C_C = 22$ pF,	$R_L = 600\ \Omega$, f = 10 kHz		0.3			0.3		Ω
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$ min,	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$,	$R_S = 50\ \Omega$	86	100		80	100		dB
I_{OS}	Output short-circuit current				38			38		mA
I_{CC}	Supply current	No load, $V_O = 0$	$T_A = 25°C$		4	6.5		4	8	mA
			T_A = full range			9				

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is $T_A = -55°C$ to 125°C for SE5534 and SE5534A and 0°C to 70°C for NE5534 and NE5534A.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SE5534, NE5534 MIN	SE5534, NE5534 TYP	SE5534, NE5534 MAX	SE5534A, NE5534A MIN	SE5534A, NE5534A TYP	SE5534A, NE5534A MAX	UNIT
SR	Slew rate at unity gain	$C_C = 0$		13			13		V/μs
		$C_C = 22$ pF		6			6		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 22$ pF, $C_L = 100$ pF		20			20		ns
	Overshoot factor			20%			20%		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 47$ pF, $C_L = 500$ pF		50			50		ns
	Overshoot factor			35%			35%		
V_n	Equivalent input noise voltage	f = 30 Hz		7			5.5	7	nV/√Hz
		f = 1 kHz		4			3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz		2.5			1.5		pA/√Hz
		f = 1 kHz		0.6			0.4		
F	Average noise figure	$R_S = 5$ kΩ, f = 10 Hz to 20 kHz					0.9		dB

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT
and INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

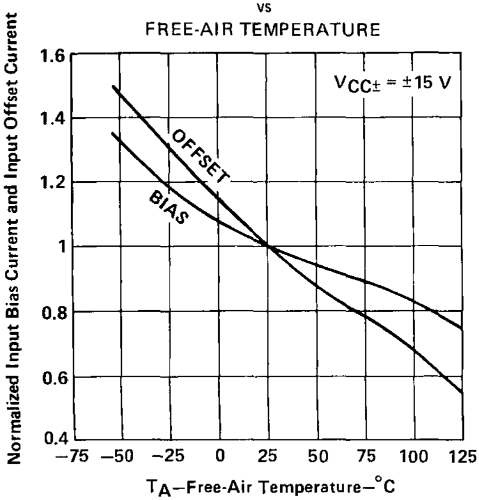


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

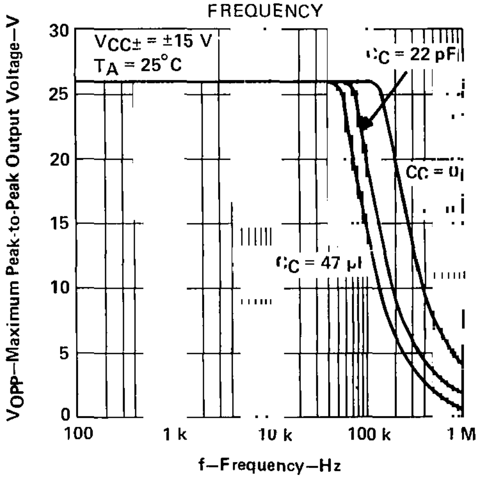


FIGURE 2

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

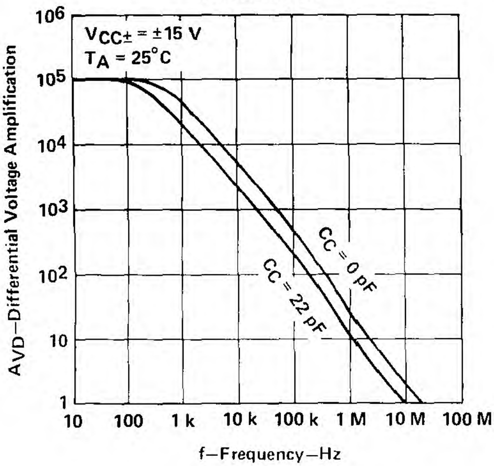


FIGURE 3

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

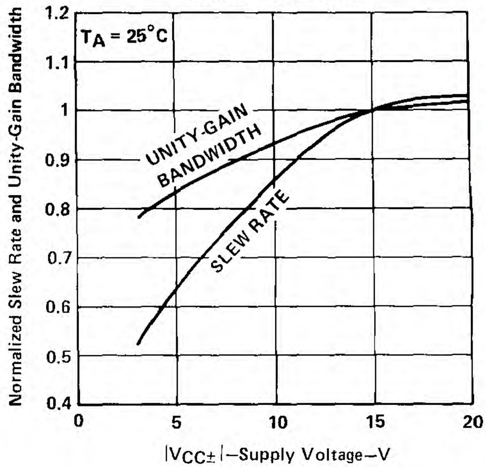


FIGURE 4

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

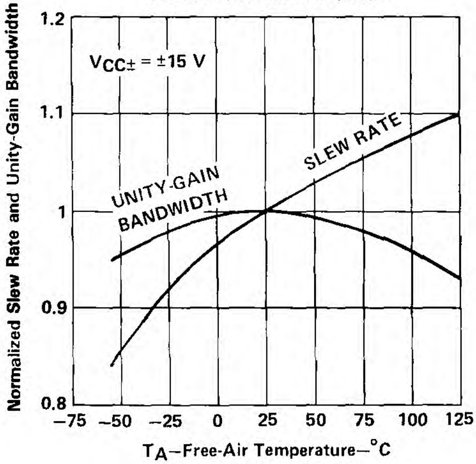


FIGURE 5

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

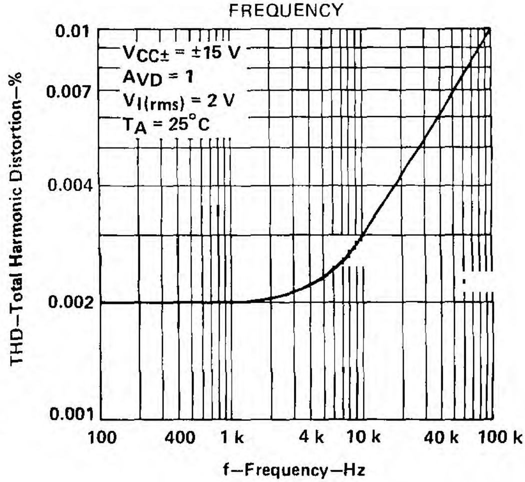


FIGURE 6

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

2

Operational Amplifiers

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

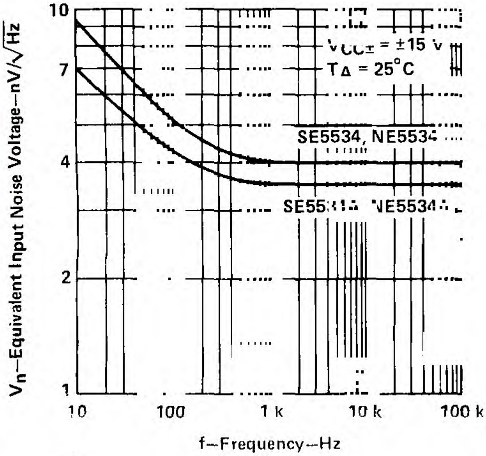


FIGURE 7

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

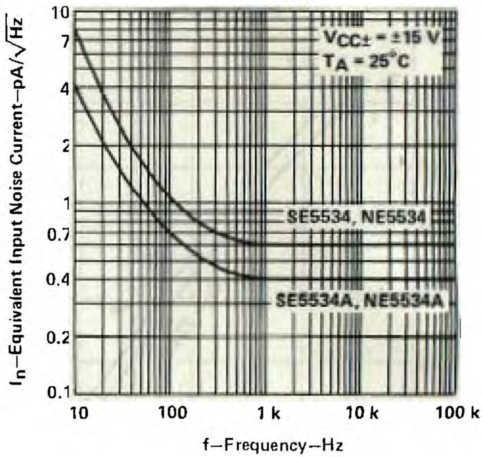


FIGURE 8

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

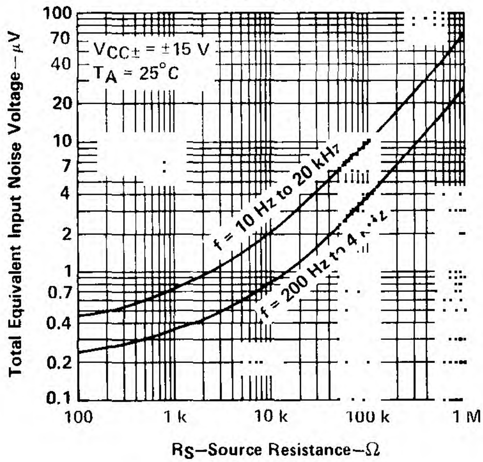


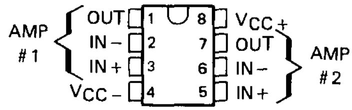
FIGURE 9

D1661, SEPTEMBER 1973—REVISED JULY 1988

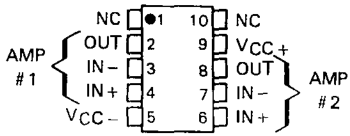
- Very Low Power Consumption
- Power Dissipation with ±2-V Supplies . . . 170 μW Typ
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Input Offset Voltage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Popular Dual Op Amp Pin-Out

TL022M IS NOT RECOMMENDED FOR NEW DESIGNS

TL022M . . . JG PACKAGE
TL022C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TL022M . . . U FLAT PACKAGE
(TOP VIEW)



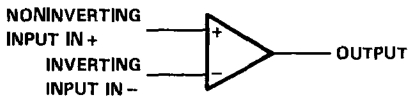
NC—No internal connection

description

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL022C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	5 mV	TL022CD	TL022CJG	TL022CP	—
−55°C to 125°C	5 mV	—	TL022MJG	—	TL022MU

The D package is available taped and reeled. Add the suffix R to the device type (i.e. TL022CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL022M	TL022C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
[illegible]rential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to [illegible]	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		[illegible]	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible] mW	5.8 mW/°C	33°C	464 mW	—
JG (TL022M)	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
JG (TL022C)	680 mW	6.6 mW/°C	47°C	528 mW	—
P	680 mW	8.0 mW/°C	65°C	640 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		50	100		100		nA
			Full range			250				
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	20	26		20	26		V
		$R_L \geq 10\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplication	$R_L \geq 10\ k\Omega$, $V_O = \pm 10$ V	25°C	72	86		60	80		dB
			Full range	66			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $R_S = 50\ \Omega$	25°C		30	150		30	200	µV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, $B = 1$ Hz, $f = 1$ kHz	25°C		50			50		$nV/\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	No load, $V_O = 0$	25°C		130			130		µA
			Full range							
P_D	Total dissipation (both amplifiers)	No load, $V_O = 0$	25°C		3.9	6		3.9	7.5	mW
			Full range			6			7.5	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022M is −55°C to 125°C and for TL022C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10\ k\Omega$,		0.3			0.3		µs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

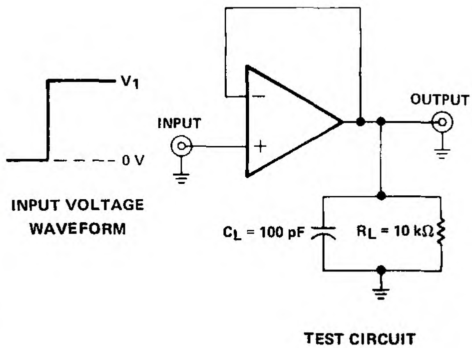


FIGURE 1. RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

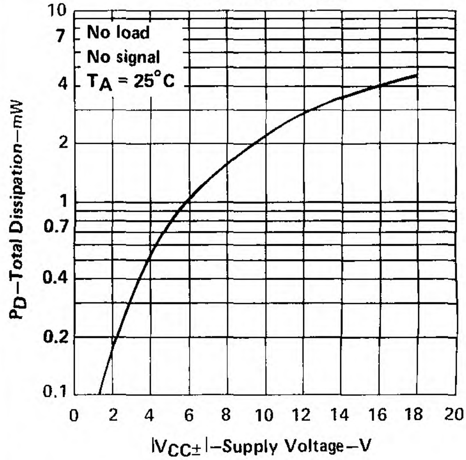
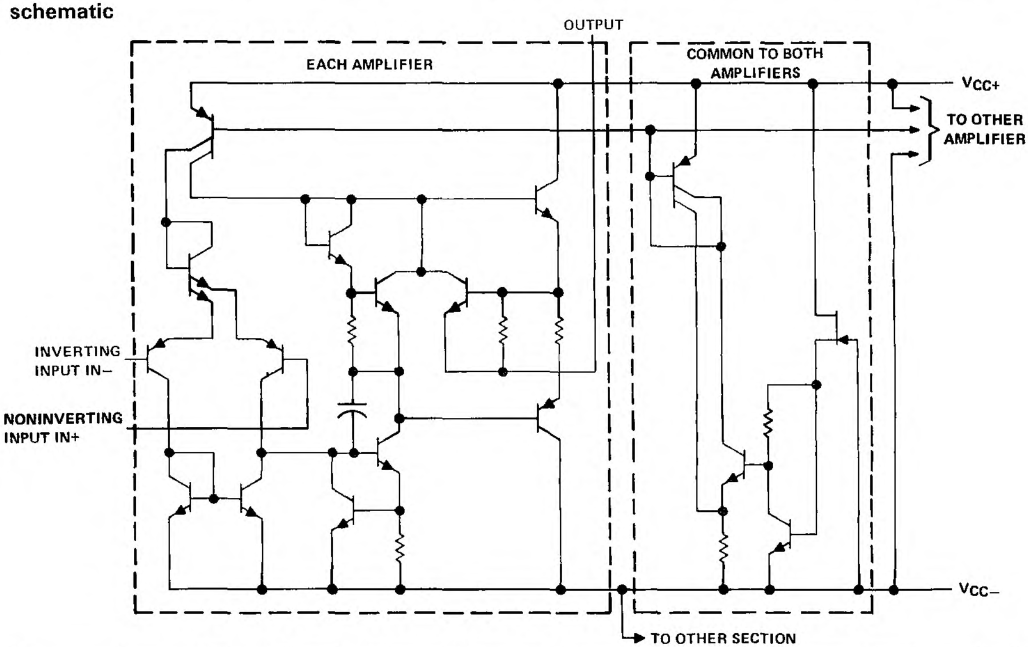


FIGURE 2

schematic

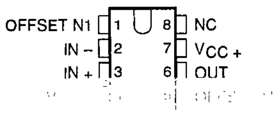


TL031, TL031A
ENHANCED JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

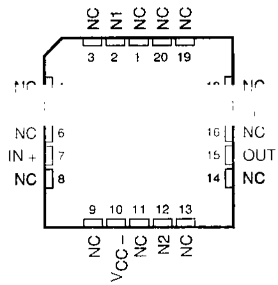
D3151, JULY 1988 – REVISED JANUARY 1989

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 6.5 mW Typ**
- **Output Short-Circuit Protection**

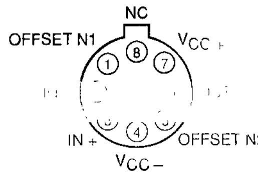
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

description

The TL031 and TL031A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

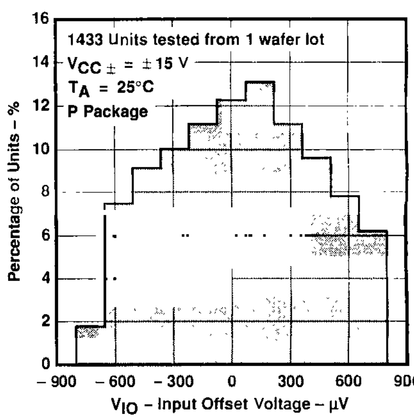
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL031 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL031 has been designed to be functionally compatible and pin compatible with the TL061.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE: SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	T[illegible]	—	TL031ACJG	TL031ACL	TL031ACP
	1.5 mV	[illegible]	—	TL031CJG	TL031CL	TL031CP
[illegible] to 85°C	0.8 mV	[illegible]	—	T[illegible]JG	[illegible]	TL031AIP
	1.5 mV	[illegible]	—	T[illegible]G	T[illegible]	TL031IP
–55°C to 125°C	0.8 mV	TL[illegible]	TL031AMFK	T[illegible]	T[illegible]	[illegible]
	1.5 mV	TL0[illegible]	TL031MFK	T[illegible]	T[illegible]	TL031MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL031CDR).

DISTRIBUTION OF TL031A
INPUT OFFSET VOLTAGE



TEXAS INSTRUMENTS
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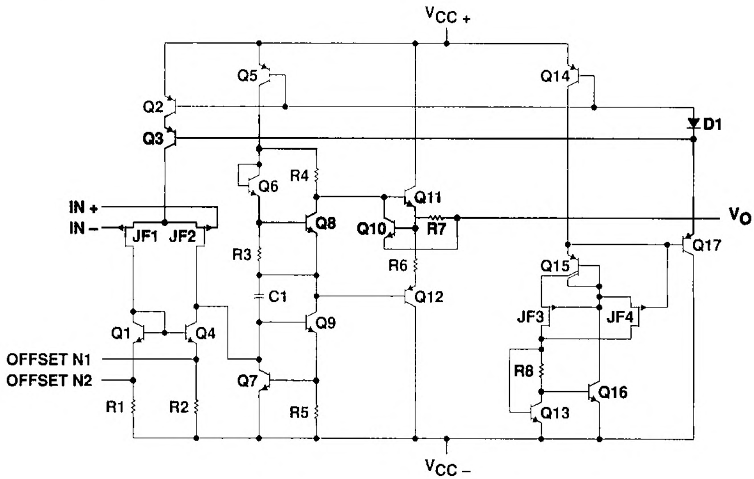
description (continued)

Two offset voltage grades are available: TL031 (1.5 mV max) and TL031A (800 μV max).

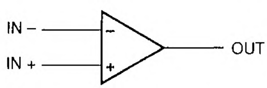
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic



symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . − 18 V
Differential input voltage (see Note 2) . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . ± 15 V
Input current, I_I (each input) . . . . ± 1 mA
Output current, I_O . . . . ± 40 mA
Total current into V_{CC+} terminal . . . . 160 mA
Total current out of V_{CC-} terminal . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . − 55°C to 125°C
I-suffix . . . . − 40°C to 85°C
C-suffix . . . . 0°C to 70°C
Storage temperature range . . . . − 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply v[illegible] : V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1.5		4	− 1.5		4	− 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	− 11.5		14	− 11.5		14	− 11.5		14	
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031M	25°C		0.54	3.5		0.5	1.5	mV
				Full range			6.5			4.5	
			TL031AM	25°C		0.41	2.8		0.34	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL031M	25°C to 125°C		5.1			4.3		µV/°C
			TL031AM	25°C to 125°C		5.1			4.3		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				−55°C		1.1	2.5		4.7	8.4	
				125°C		1.8	2.5		5.8	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192			217		µA
				−55°C		114			156		
				125°C		178	250		197	280	

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1, See Note 7	25°C		2.0		2	2.9		V/µs
			− 55°C		1.4		1.2	1.9		
			125°C		2.4		1.2	3.5		
SR −	Negative slew rate at unity gain		25°C		3.9		3	5.1		V/µs
			− 55°C		3.2		2.5	4.6		
			125°C		4.1		2.5	4.7		
t_r	Rise time	$V_{IPP} = \pm 10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2	25°C		138			132		ns
			− 55°C		142			123		
			125°C		166			158		
t_f	Fall time		25°C		138			132		ns
			− 55°C		142			123		
			125°C		166			158		
	Overshoot factor		25°C		11%			5%		
			− 55°C		16%			6%		
			125°C		14%			8%		
V_n	Equivalent input noise voltage, TL031M	$R_S = 100\ \Omega$, See Figure 3, f = 10 Hz	25°C		61			61		nV/√Hz
		f = 1 kHz			41			41		
	TL031AM	f = 10 Hz	25°C		61			61		
		f = 1 kHz			41			41		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4	25°C		1			1.1		MHz
			− 55°C		1			1.1		
			125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4	25°C		61°			65°		
			− 55°C		57°			64°		
			125°C		59°			62°		

NOTE 7: For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL031I	25°C to 85°C		6.5			6.2		µV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				−40°C		1.4	2.5		5.4	8.4	
				85°C		1.9	2.5		6.2	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	[illegible]		[illegible]	280	µA
				−40°C		144	[illegible]		181	[illegible]	
				85°C		189	250		207	280	

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

8. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2.0		2	2.9		V/μs
			− 40°C		1.6		1.5	2.1		
			85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			− 40°C		3.3		3.2	4.8		
			85°C		4.1		3.2	4.9		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			− 40°C		132			123		
			85°C		154			146		
t_f	Fall time		25°C		138			132		ns
			− 40°C		132			123		
			85°C		154			146		
	Overshoot factor		25°C		11%			5%		
			− 40°C		[illegible]			5%		
			85°C		[illegible]			7%		
V_n	Equivalent input noise voltage (see Note 9), TL031I	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		61			61		nV/√Hz
	TL031I	f = 1 kHz			41			41		
	TL031AI	f = 10 Hz	25°C		61			61		
	TL031AI	f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			− 40°C		1			1.1		
			85°C		0.9			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			− 40°C		60°			65°		
			85°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ± 5 V, V_{IPP} = ± 1 V; for $V_{CC\pm}$ = ± 15 V, V_{IPP} = ± 5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	[illegible]		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	[illegible]		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	− [illegible]		V
				0°C	−3	−4.1		−12.5	− [illegible]		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	[illegible]		
r_i	Input resistance			25°C		10^{12}			[illegible]		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				0°C		1.8	2.5		6.3	8.4	
				70°C		1.9	2.5		6.3	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	250		217	280	µA
				0°C		184	250		211	280	
				70°C		189	250		210	280	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

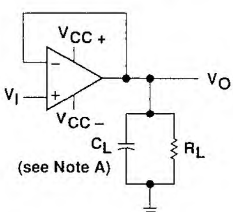
8. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2.0		2	2.9		V/μs
			0°C		1.8		1.5	2.6		
			70°C		2.2		2	3.2		
SR –	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			0°C		3.7		3.2	5.0		
			70°C		4.0		3.2	5.0		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138					ns
			0°C		134					
			70°C		150			142		
t_f	Fall time		25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
	Overshoot factor		25°C		11%			5%		
			0°C		10%			4%		
			70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9), TL031C	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		61			61		nV/√Hz
		f = 1 kHz			41			41		
	TL031AC	f = 10 Hz	25°C		61			61		
		f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			0°C		1			1.1		
			70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			0°C		61°			65°		
			70°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

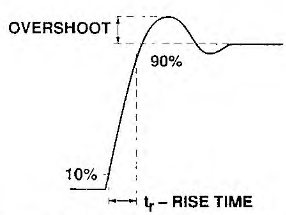


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

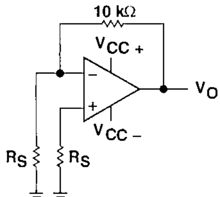
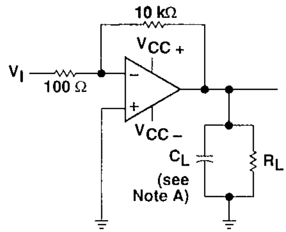


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

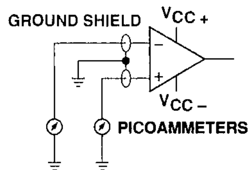


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL031 and TL031A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE

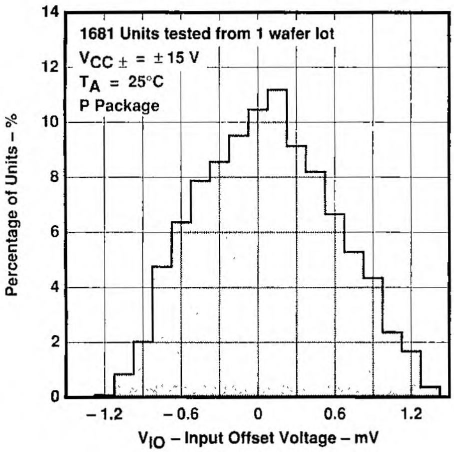

FIGURE 6

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

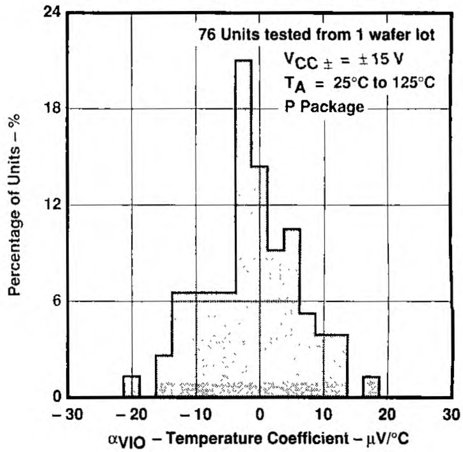

FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

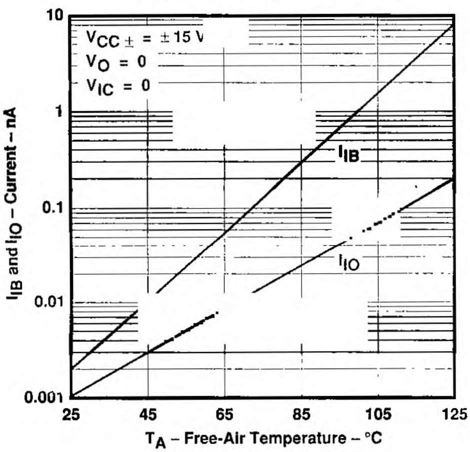

FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

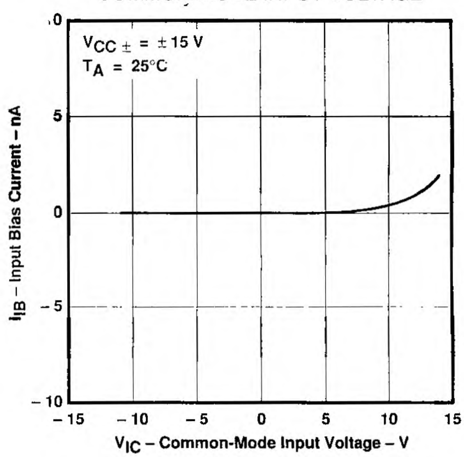

FIGURE 9

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

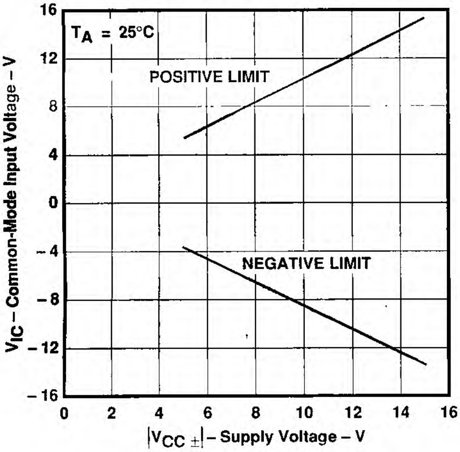

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

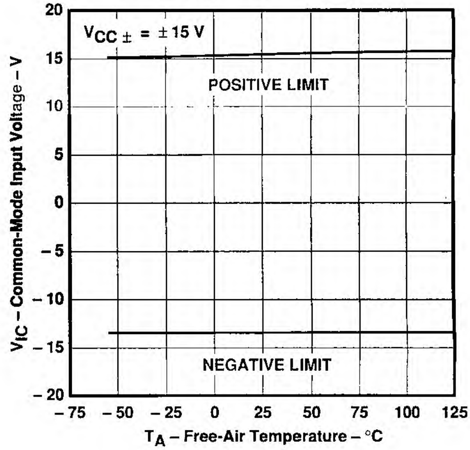

FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

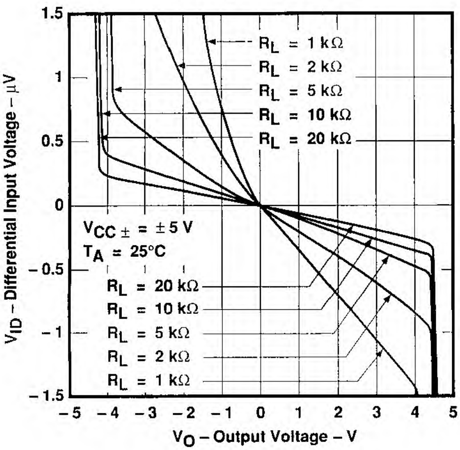

FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

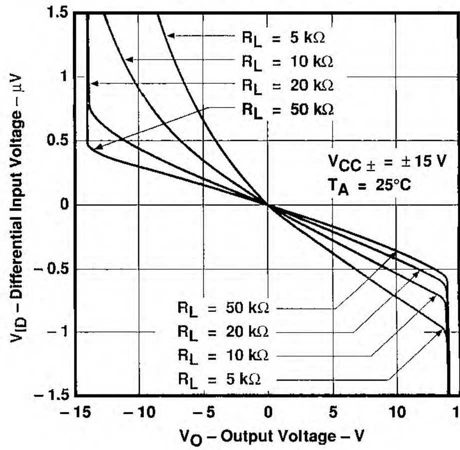

FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

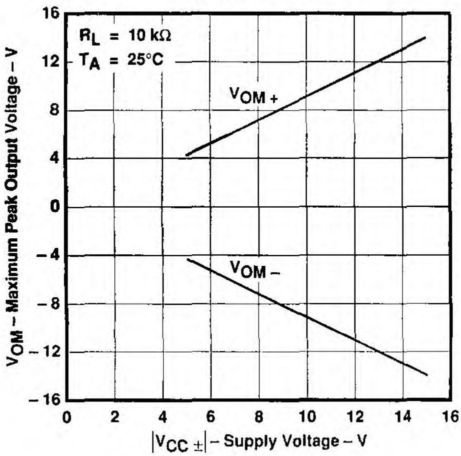

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

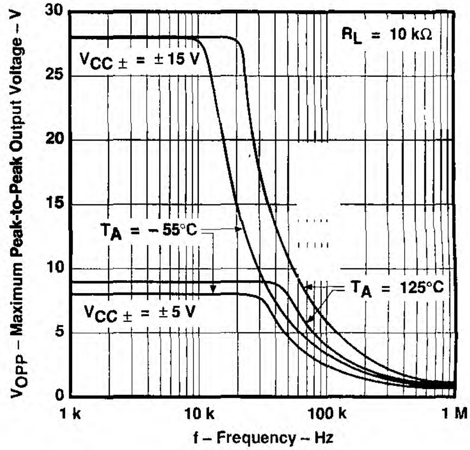

FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

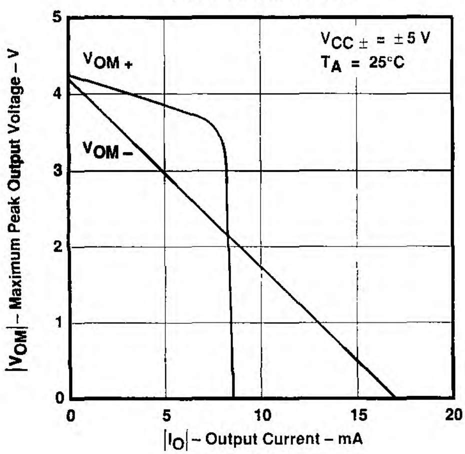

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

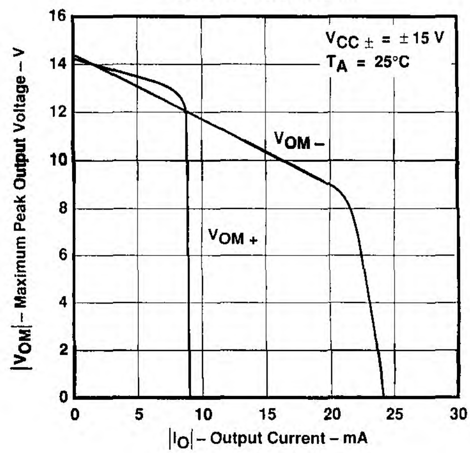

FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

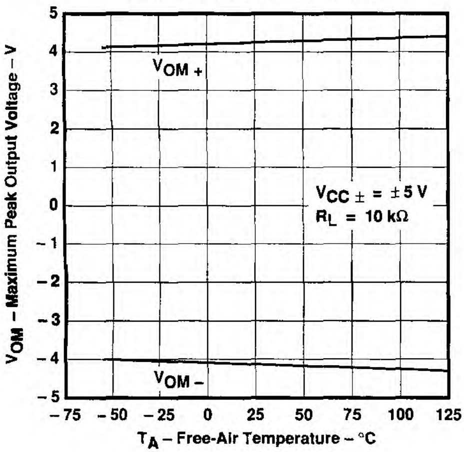

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

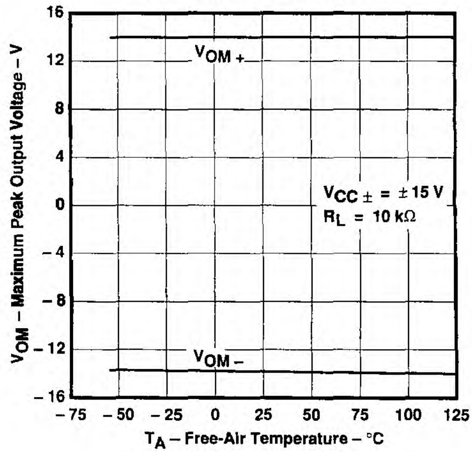

FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

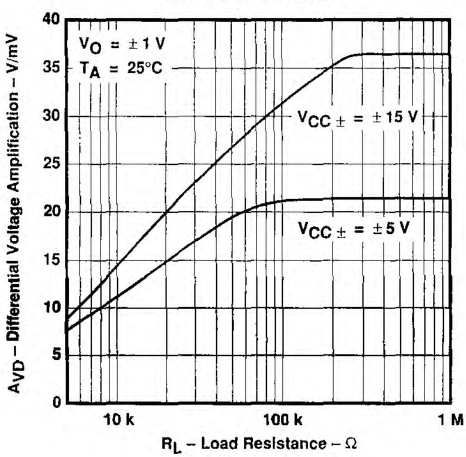

FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

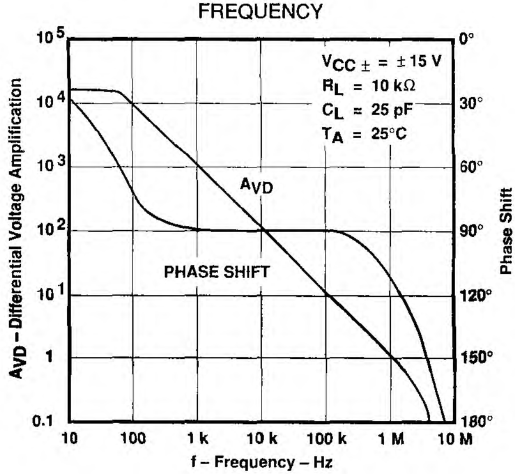

FIGURE 21

2

Operational Amplifiers

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

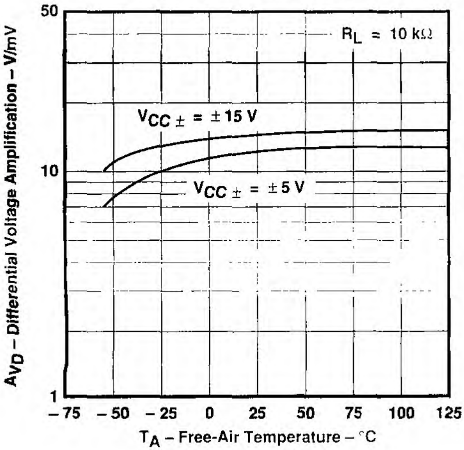

FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

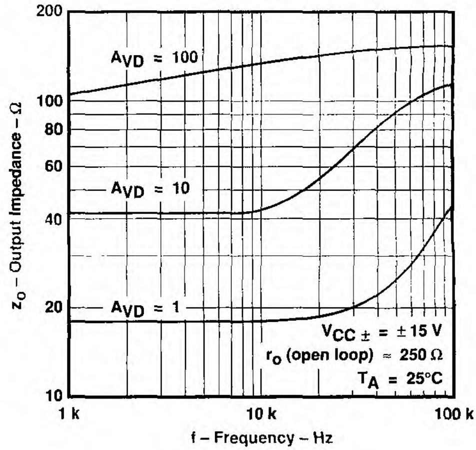

FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

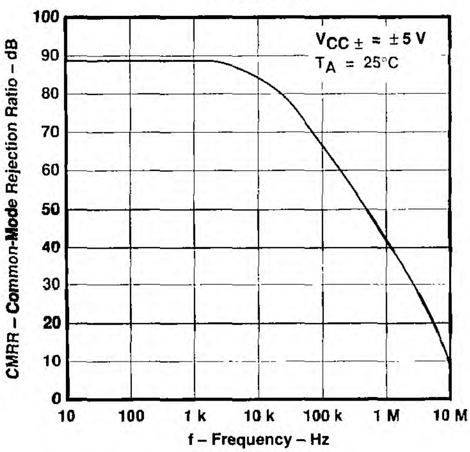

FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

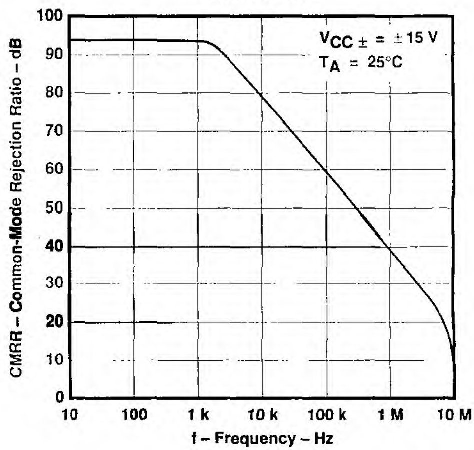

FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

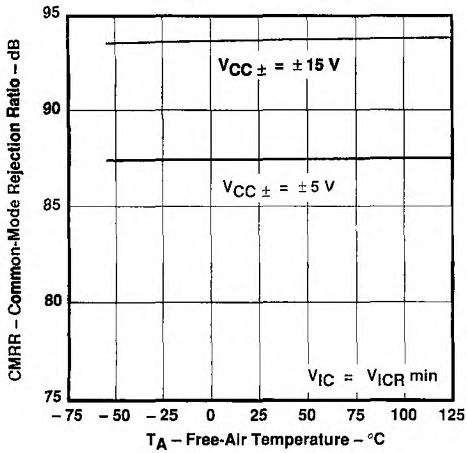

FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

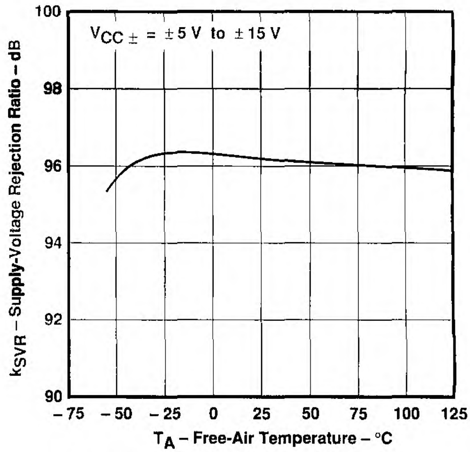

FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

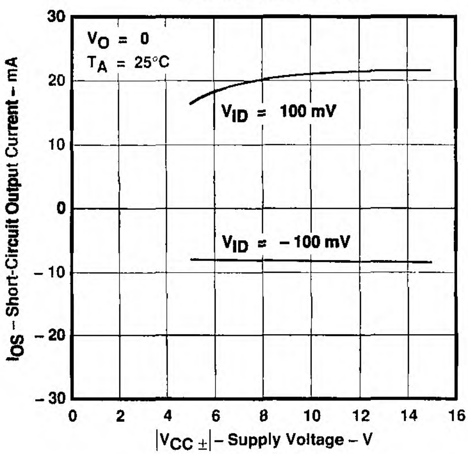

FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

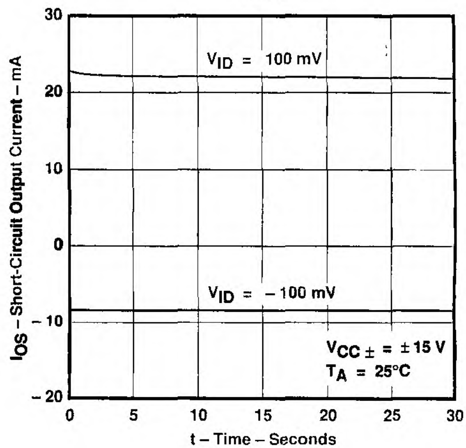

FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

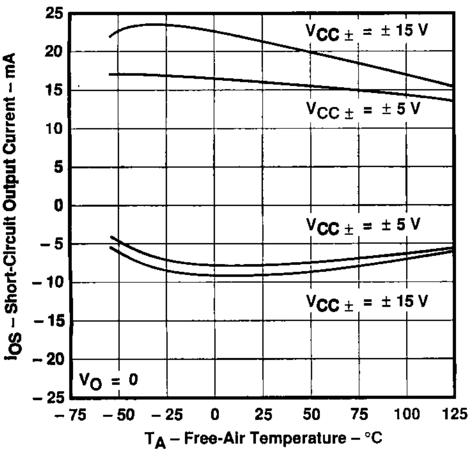

FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

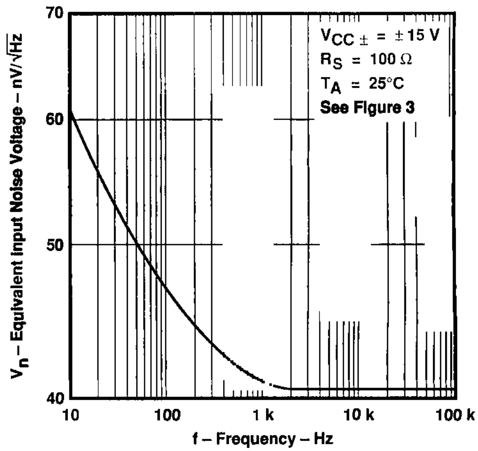

FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

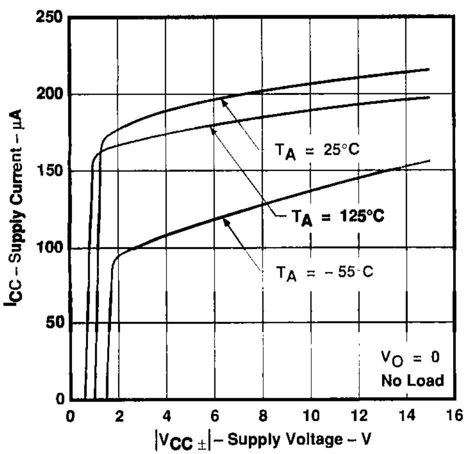

FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

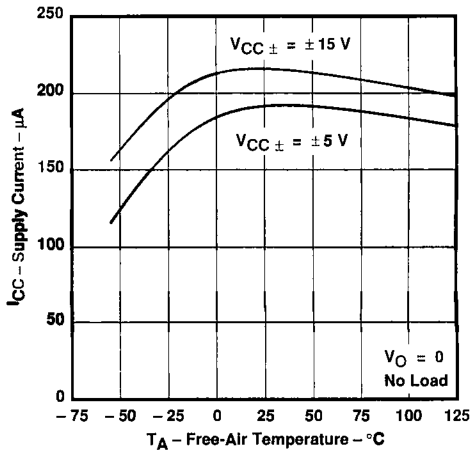

FIGURE 33

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

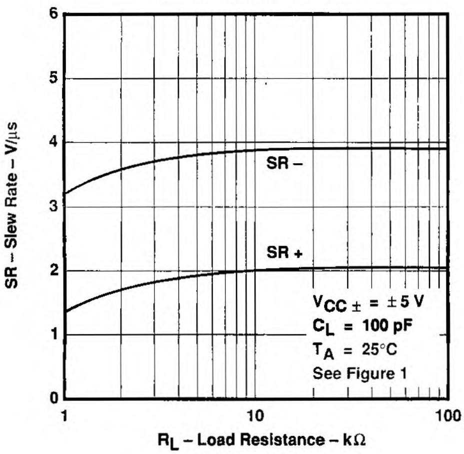


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

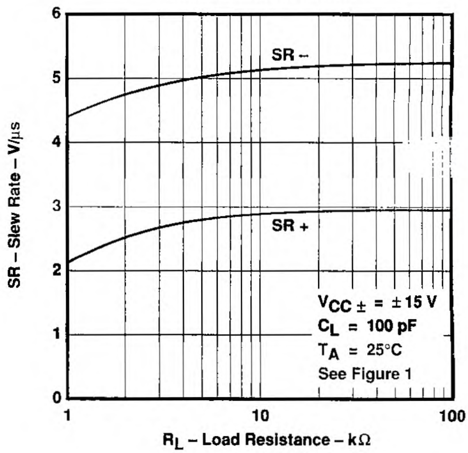


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

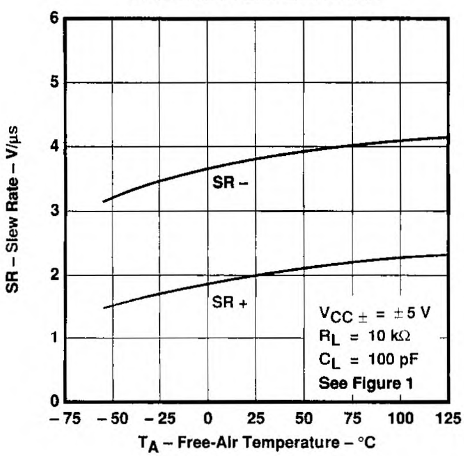


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

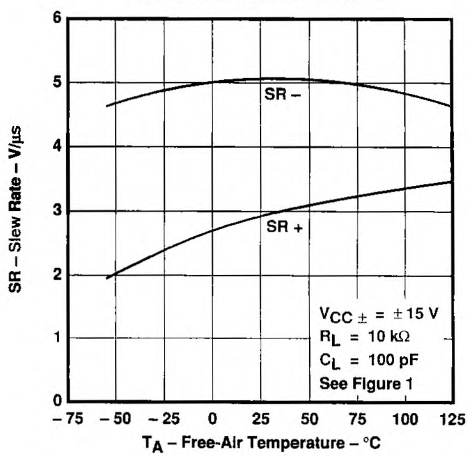


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

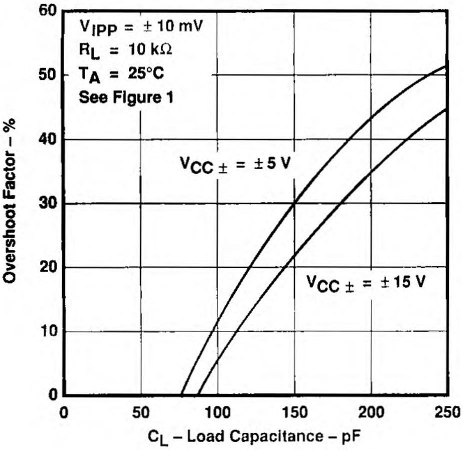


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

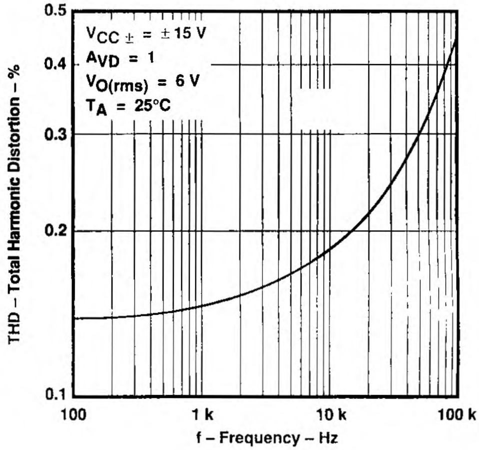


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

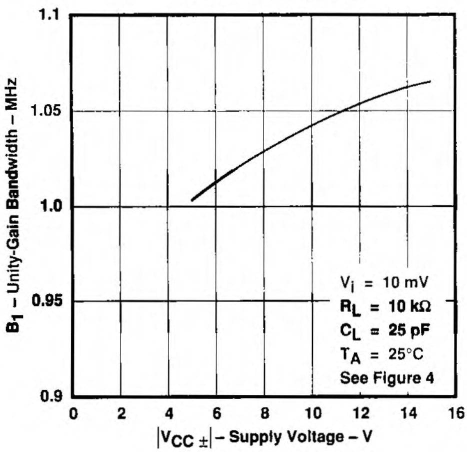


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

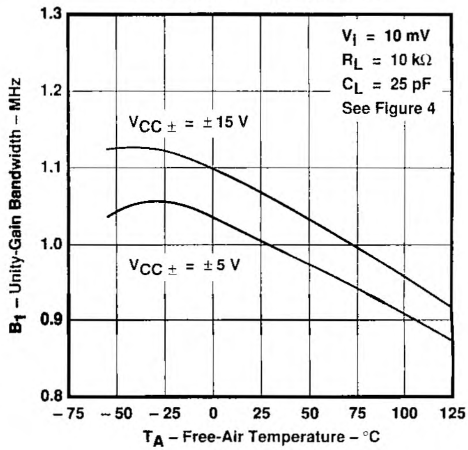


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

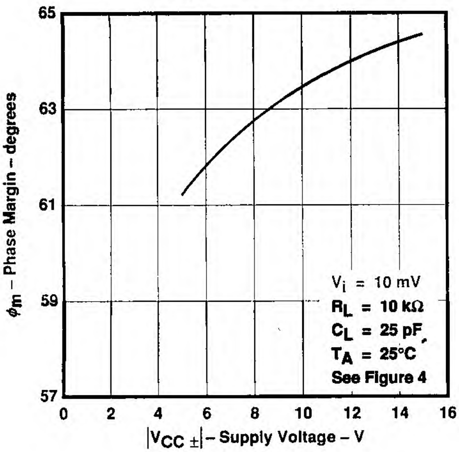


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

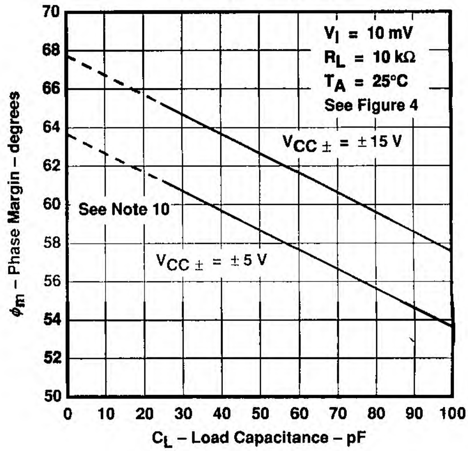


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

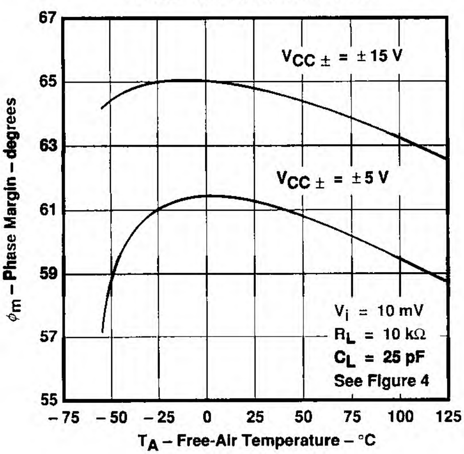


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

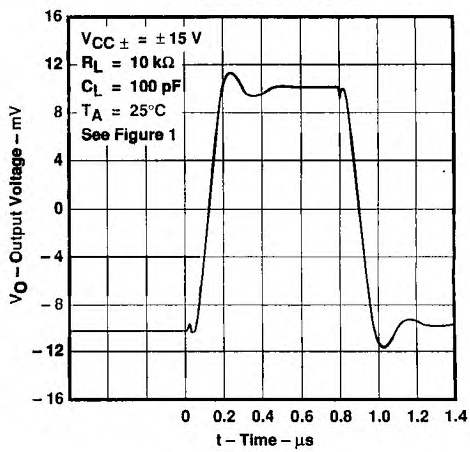


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

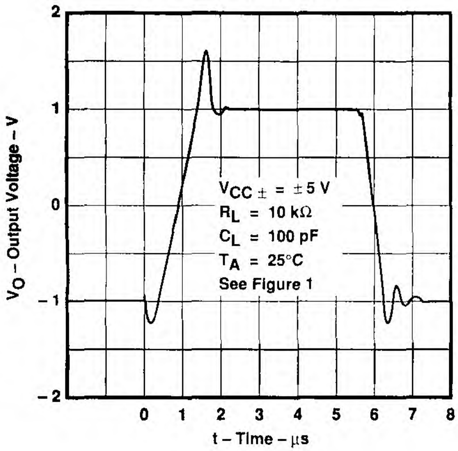


FIGURE 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

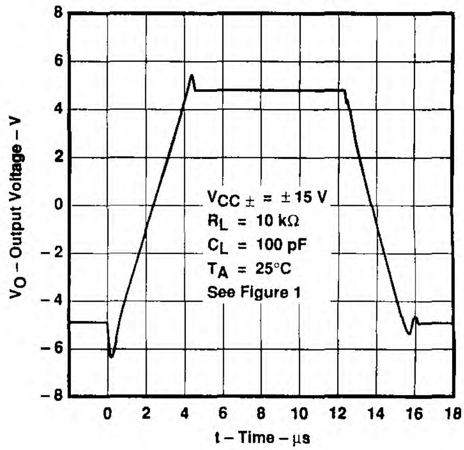


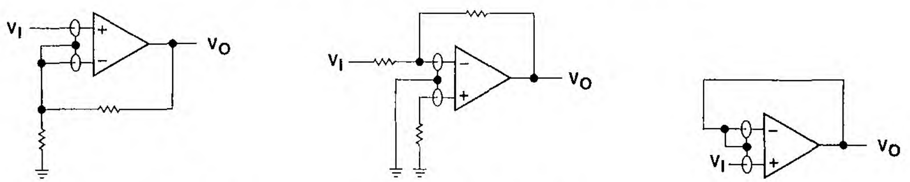
FIGURE 47

TYPICAL APPLICATION DATA

input characteristics

The TL031 and TL031A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL031 and TL031A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



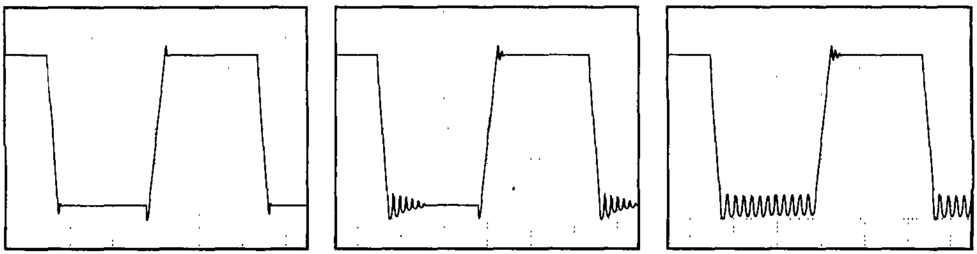
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 48. USE OF GUARD RINGS

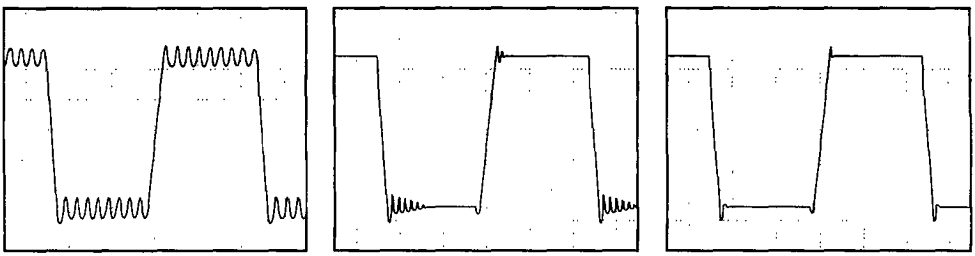
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL031 and TL031A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

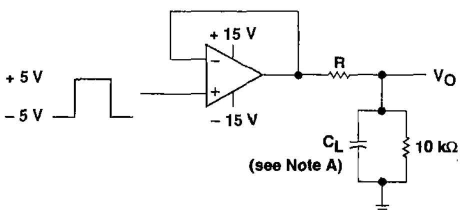


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

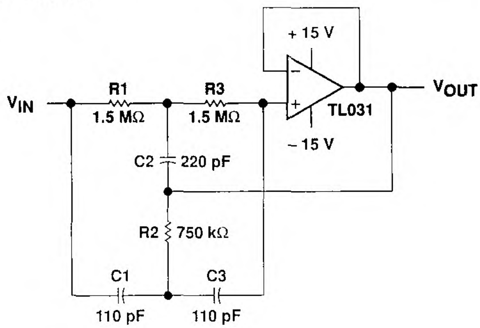
TYPICAL APPLICATION DATA

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. The circuit in Figure 51 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown in Figure 51, the center frequency is 1 kHz. Note that C1 = C3 = C2 ÷ 2 and also that R1 = R3 = 2 × R2. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.



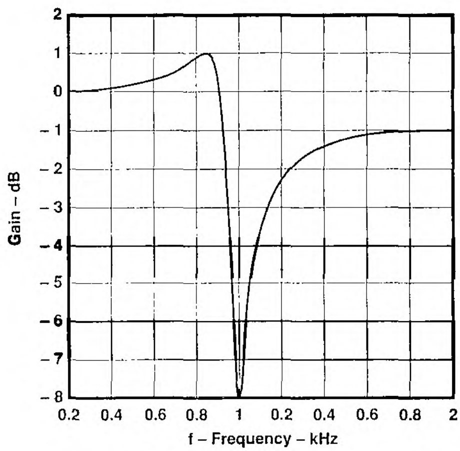


FIGURE 51. HIGH-Q NOTCH FILTER

TYPICAL APPLICATION DATA

transimpedance amplifier

The low-power precision TL031 allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL031A greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves ten-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F \left(\frac{R1 + R2}{R2} \right)$$

Using the resistor values shown in the schematic, for a 1-nA input current, the output voltage equals − 0.1 V. If the V_O limit for the TL031A is measured to be ± 12 V, the maximum input current for these resistor values is ± 120 nA. Similarly, one LSB on a ten-bit scale corresponds to 12 mV of output voltage or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = -\left[V_{IO} + R_F(I_{IN} + I_{IB})\right]\left(\frac{R1 + R2}{R2} \right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL031A inputs as shown in Figure 52.

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

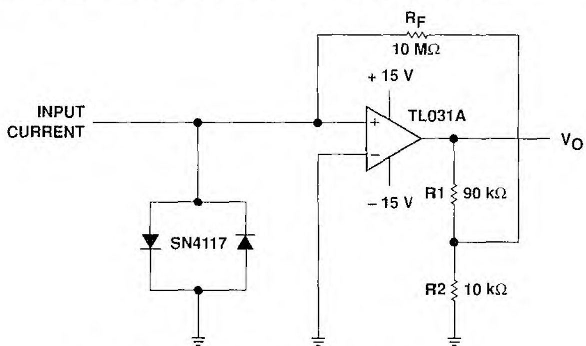


FIGURE 52. TRANSIMPEDANCE AMPLIFIER

2

Operational Amplifiers

TYPICAL APPLICATION DATA

4- to 20-mA current loops

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 53 requires three wires from the transmitting to receiving circuitry while the second variation in Figure 54 requires only two wires but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL031A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL031A is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA}$$

The circuits presently provide 4-to 20-mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL031A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA} - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA..

Thanks to the low power consumption of the TL031A, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

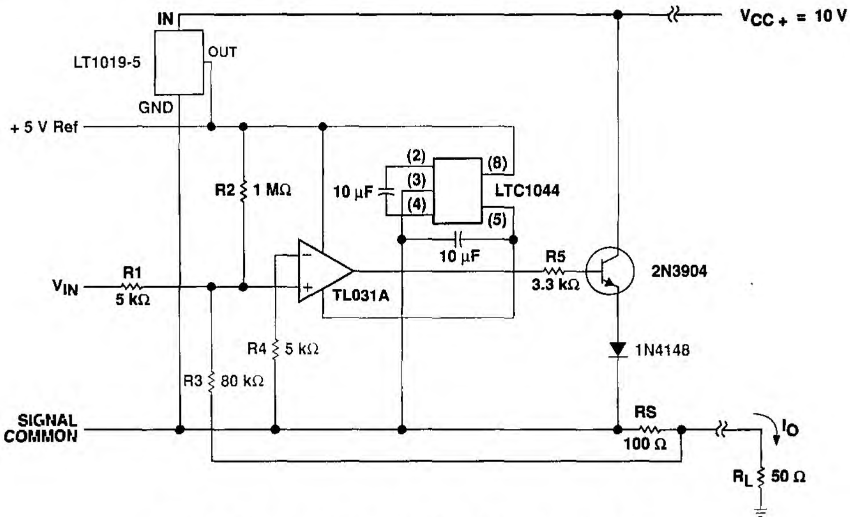


FIGURE 53. 2-WIRE 4- TO 20-mA CURRENT LOOP

TYPICAL APPLICATION DATA

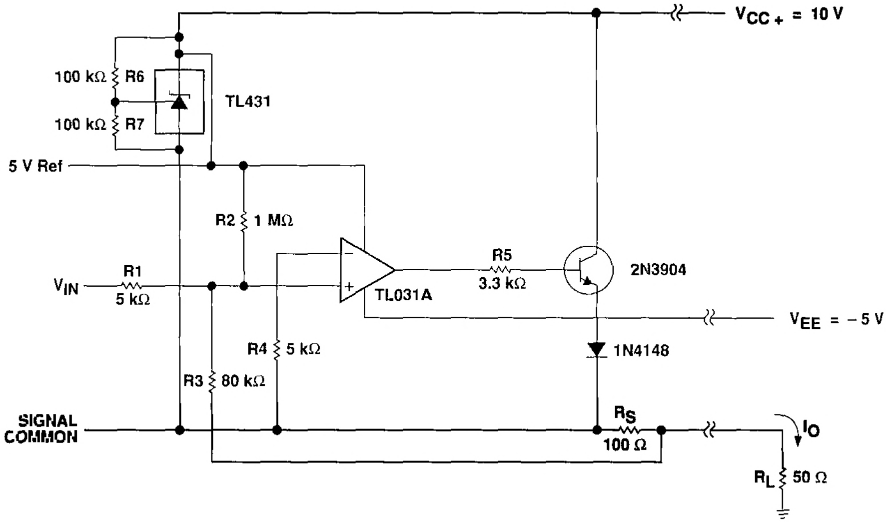
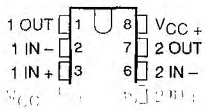


FIGURE 54. 3-WIRE 4- TO 20-mA CURRENT LOOP

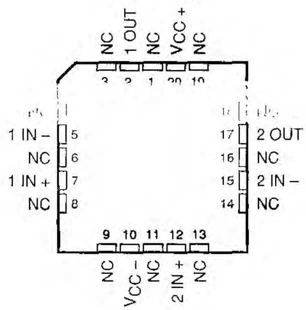
D3152, JULY 1988 – REVISED JANUARY 1989

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 13 mW Typ**
- **Output Short-Circuit Protection**

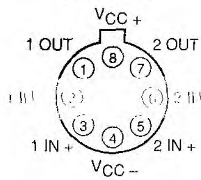
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

description

The TL032 and TL032A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

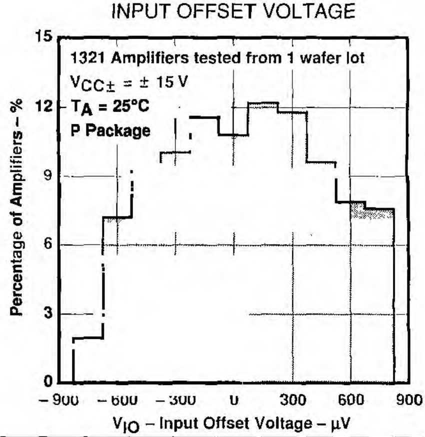
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL032 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL032 has been designed to be

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	[illegible]	—	[illegible]	TL032ACL	[illegible]
	1.5 mV	[illegible]	—	[illegible]	TL032CL	[illegible]
−40°C to 85°C	0.8 mV	TL032AID	—	[illegible]	[illegible]	[illegible]
	1.5 mV	[illegible]	—	[illegible]	[illegible]	[illegible]
−55°C to 125°C	0.8 mV	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	1.5 mV	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TL032CDR).

DISTRIBUTION OF TL032A
INPUT OFFSET VOLTAGE



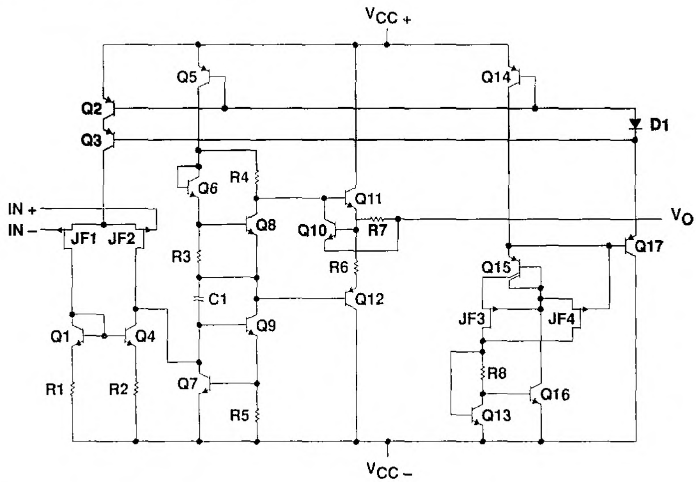
description (continued)

functionally compatible and pin compatible with the TL062. Two offset voltage grades are available: TL032 (1.5 mV max) and TL032A (800 µV max).

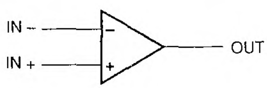
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . – 18 V
Differential input voltage (see Note 2) . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . ± 15 V
Input current, I_I (each input) . . . . ± 1 mA
Output current, I_O (each output) . . . . ± 40 mA
Total current into V_{CC+} terminal . . . . 160 mA
Total current out of V_{CC-} terminal . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . – 55°C to 125°C
I-suffix . . . . – 40°C to 85°C
C-suffix . . . . 0°C to 70°C
Storage temperature range . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply [illegible], V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm}$ = ± 15 V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032M	25°C		0.69	3.5		0.57	1.5	mV
				Full range			6.5			4.5	
			TL032AM	·		0.53	2.8		0.39	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL032M	25°C to 125°C		9.7			9 7		µV/°C
			TL032AM	25°C to 125°C		9.7			9.7		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11 5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				−55°C		2.3	5		9.4	17	
				125°C		3.6	5		11.8	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	··	µA
				−55°C			500		312		
				125°C			500		394		
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR−	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/μs
					−55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL032M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AM		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 7: For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032I	25°C to 85°C		11.4			10.8		µV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				−40°C		2.9	5		10.9	17	
				85°C		3.7	5		12.4	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434		µA
				−40°C		288	500		362		
				85°C		372	500		414	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2		2	2.9		V/μs
			− 40°C		1.6		1.5	2.1		
			85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			− 40°C		3.3		3.2	4.8		
			85°C		4.1		3.2	4.9		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			− 40°C		132			123		
			85°C		154			146		
t_f	Fall time		25°C		138			132		ns
			− 40°C		132			123		
			85°C		154			146		
	Overshoot factor		25°C		11%			5%		
			− 40°C		12%			5%		
			85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9) — TL032I	R_S = 100 Ω, See Figure 3; f = 10 Hz	25°C		49			49		nV/√Hz
		f = 1 kHz			41			41		
	TL032AI	f = 10 Hz	25°C		49			49		
		f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			− 40°C		1			1.1		
			85°C		0.9			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			− 40°C		60°			65°		
			85°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032C	25°C to 70°C		11.5			10.8		µV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5 4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4			5	15.2		
r_i	Input resistance			25°C		·			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				0°C		3.7	5		12.7	17	
				70°C		3.8	5		12.6	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434		µA
				0°C		368	500		422		
				70°C		378	500		420	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

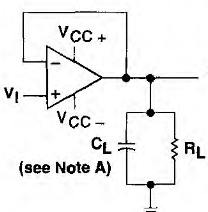
8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR+	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2		2	2.9		V/µs
			0°C		1.8		1.5	2.6		
			70°C		2.2		2	3.2		
SR−	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/µs
			0°C		3.7		3.2	5.0		
			70°C		4		3.2	5.0		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
t_f	Fall time		25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
	Overshoot factor		25°C		11%			5%		
			0°C		10%			4%		
			70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9), TL032C	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		49			49		nV/√Hz
	TL032C	f = 1 kHz			41			41		
	TL032AC	f = 10 Hz	25°C		49			49		
	TL032AC	f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			0°C		1			1.1		
			70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			0°C		61°			65°		
			70°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

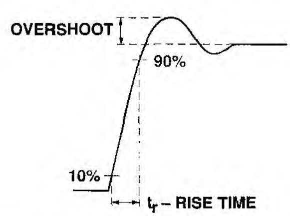


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

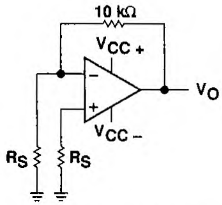
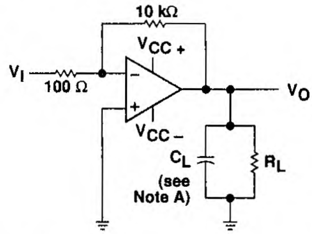


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

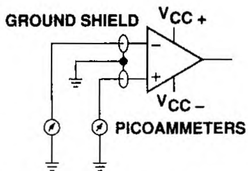


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL032 and TL032A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE

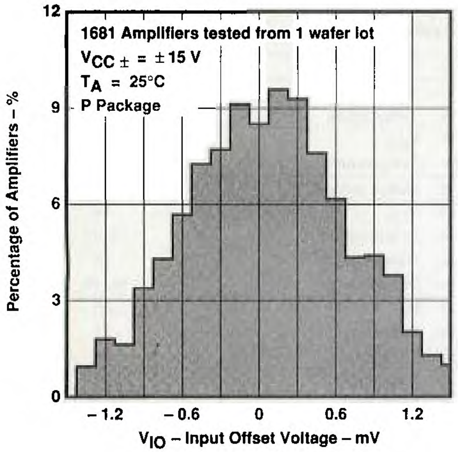


FIGURE 6

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

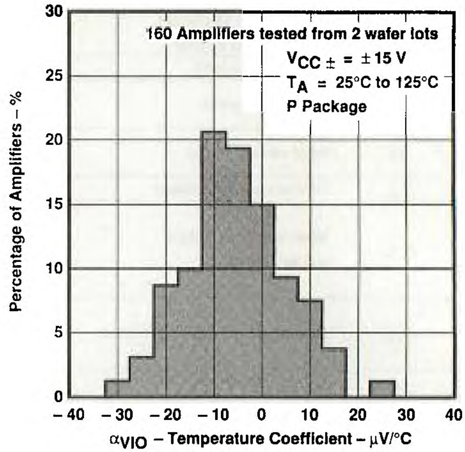


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

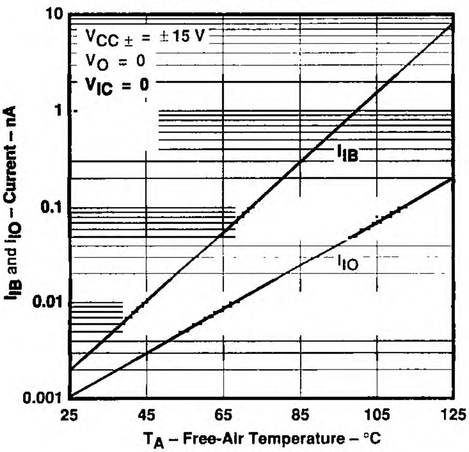


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

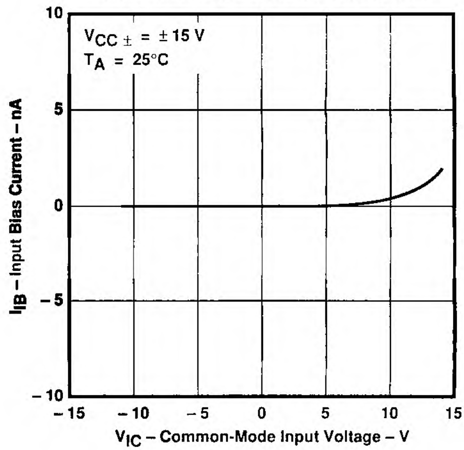


FIGURE 9

TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

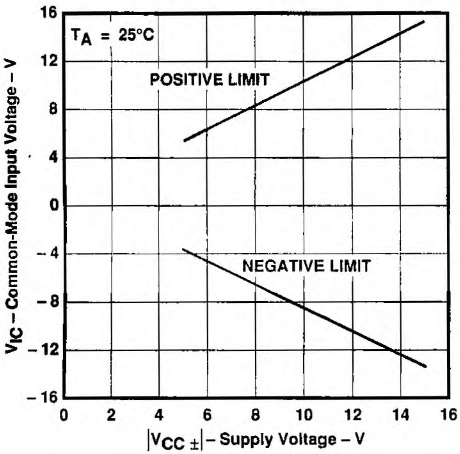


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

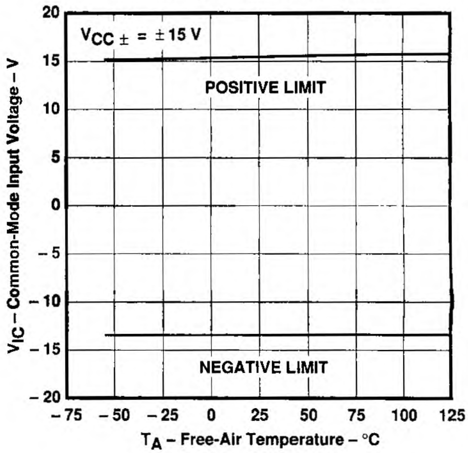


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

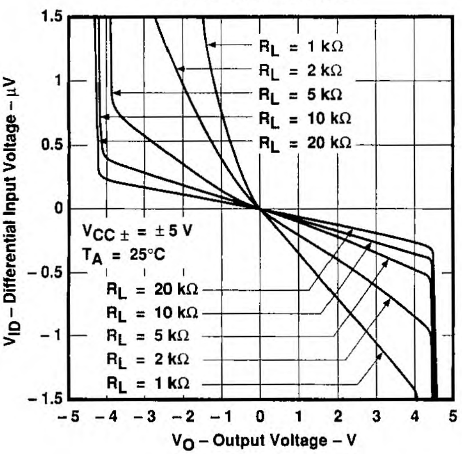


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

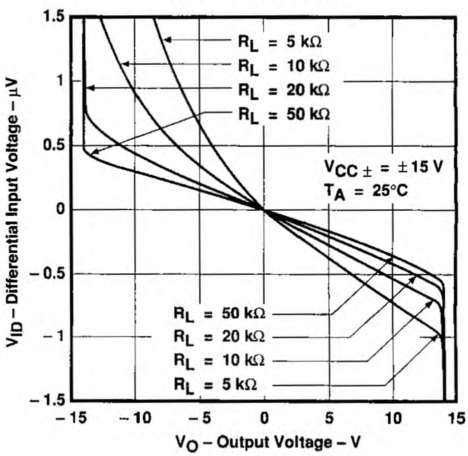


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

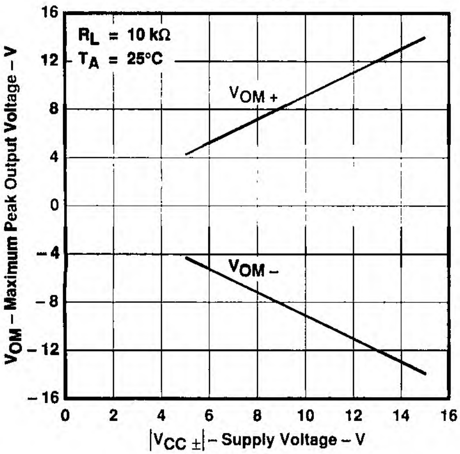


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

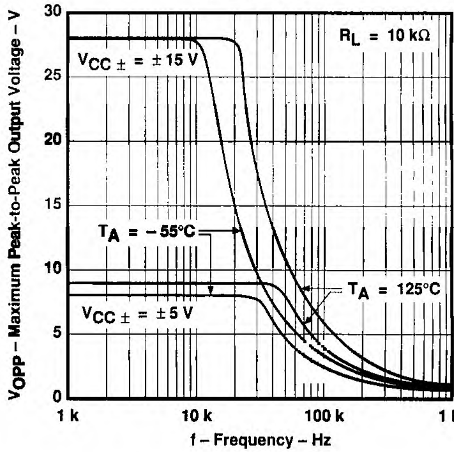


FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

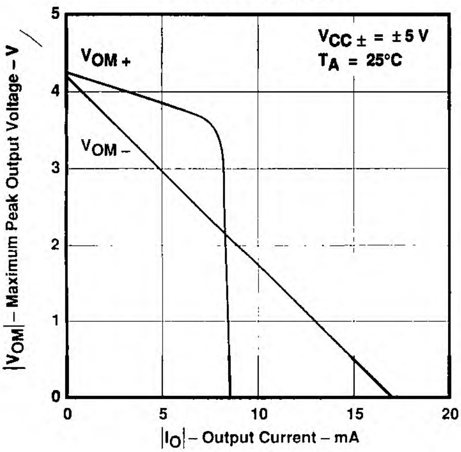


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

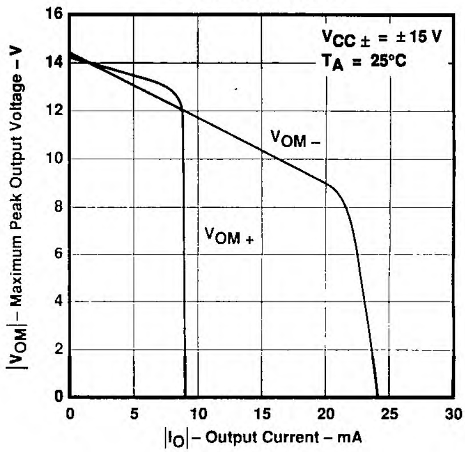


FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

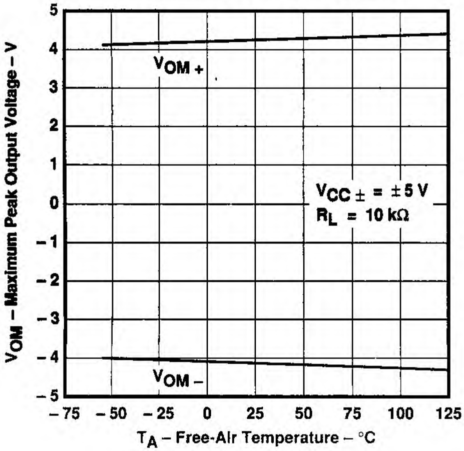


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

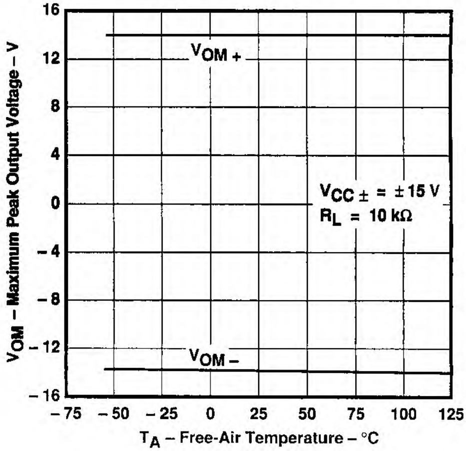


FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

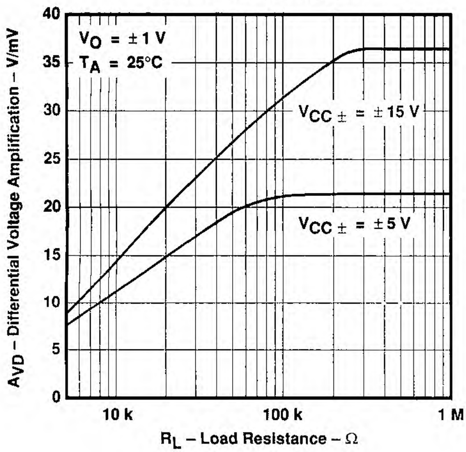


FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

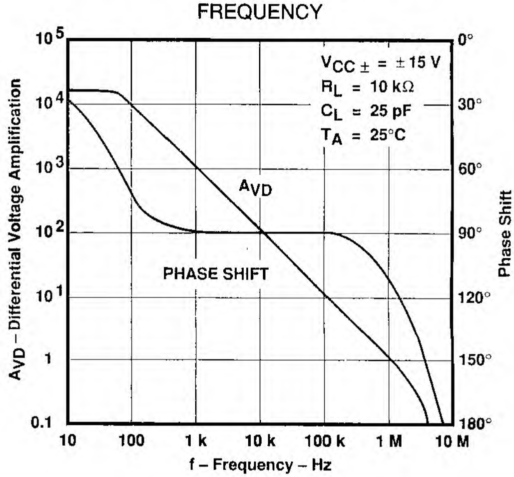


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

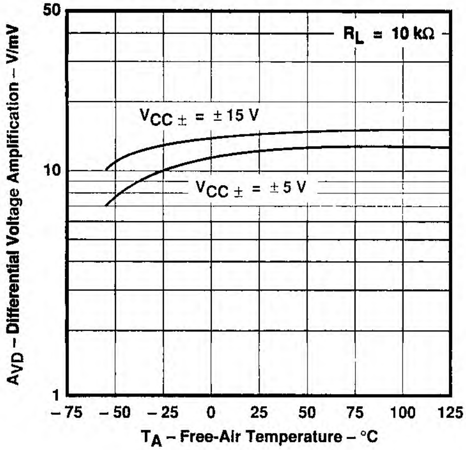


FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

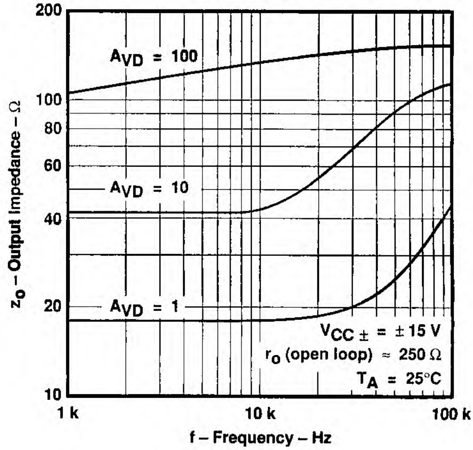


FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

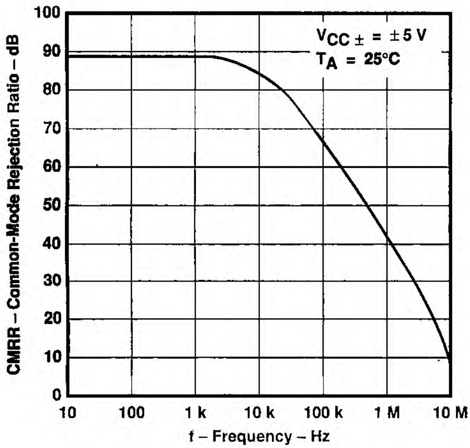


FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

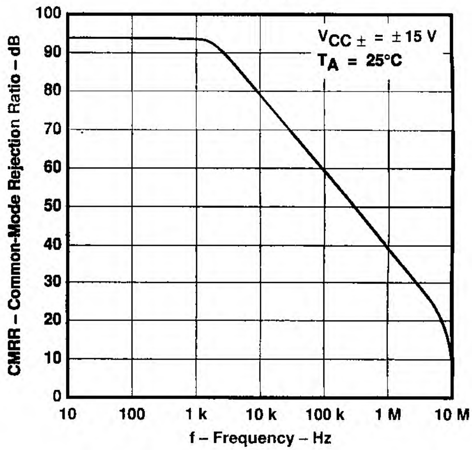


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

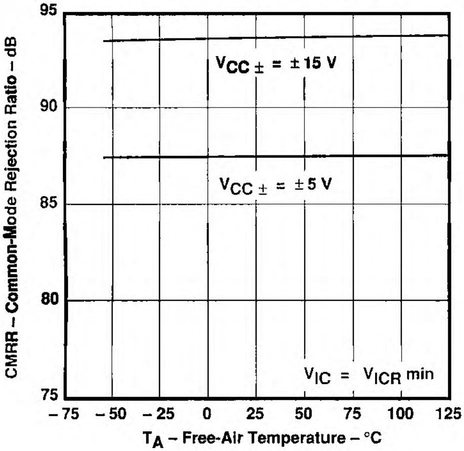


FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

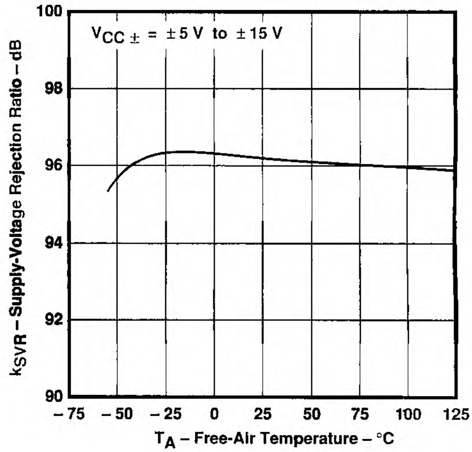


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

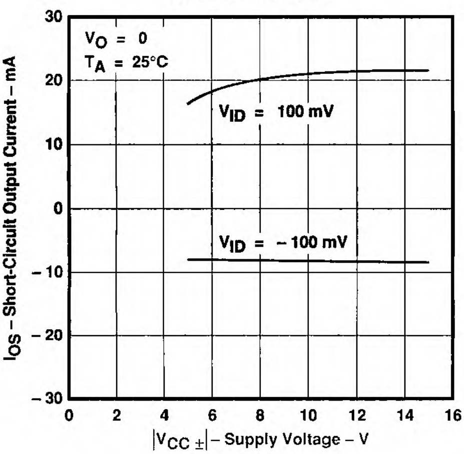


FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

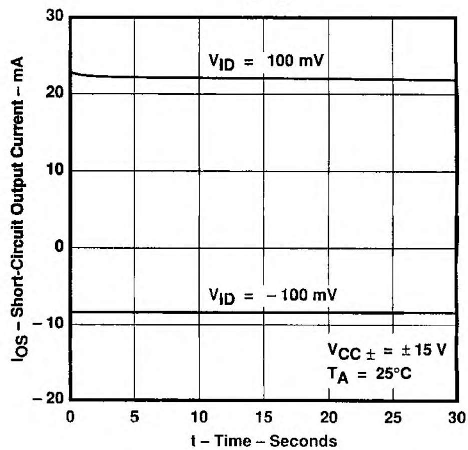


FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

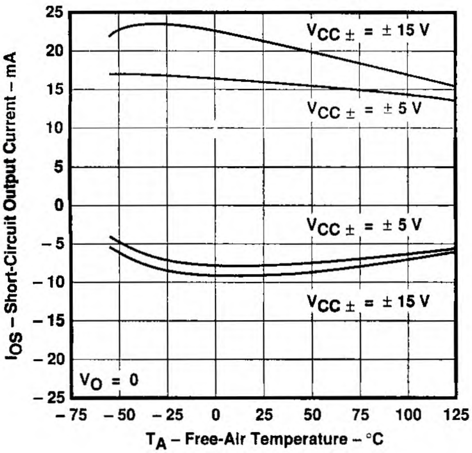


FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

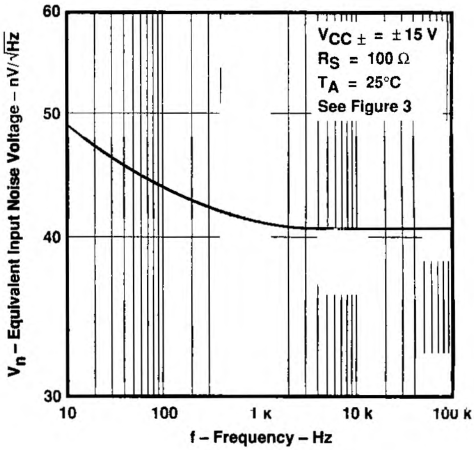


FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

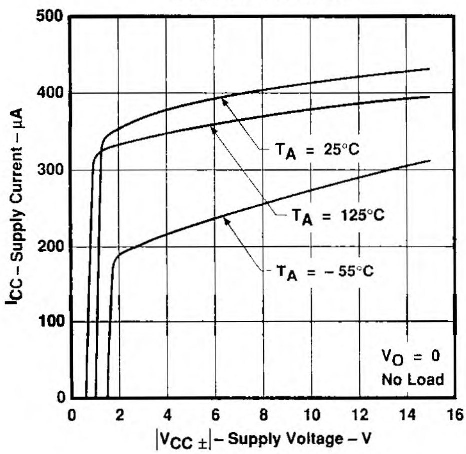


FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

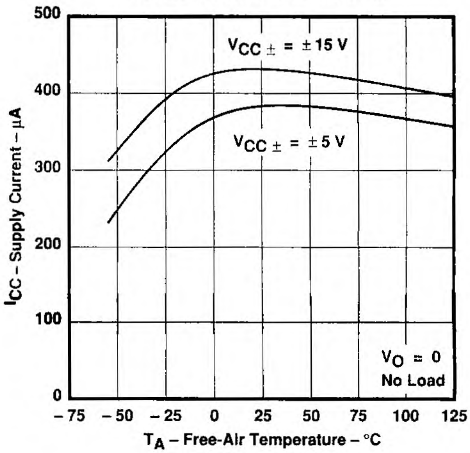


FIGURE 33

TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

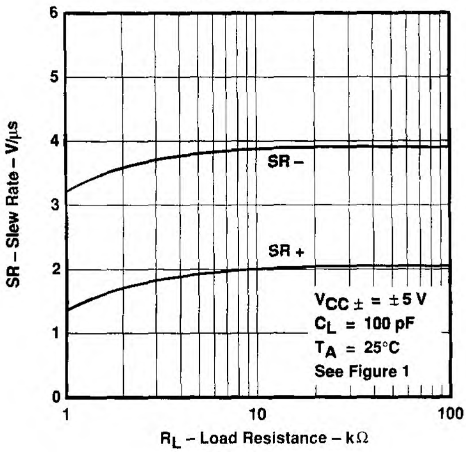


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

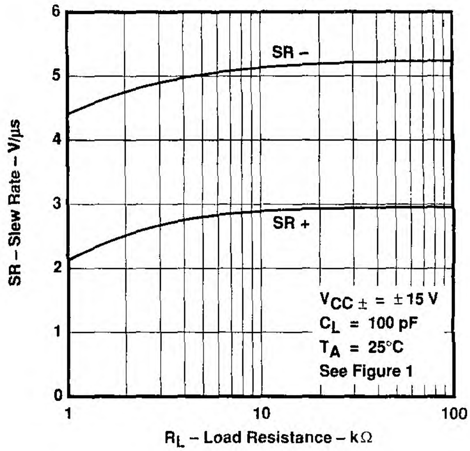


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

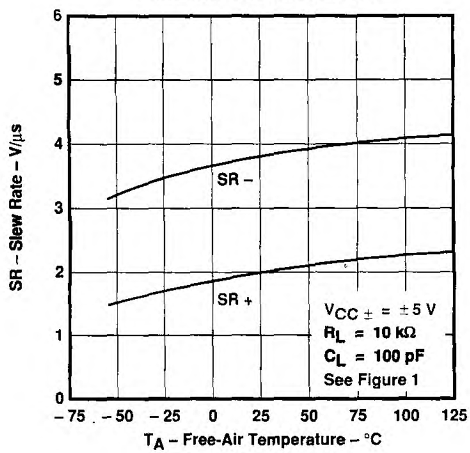


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

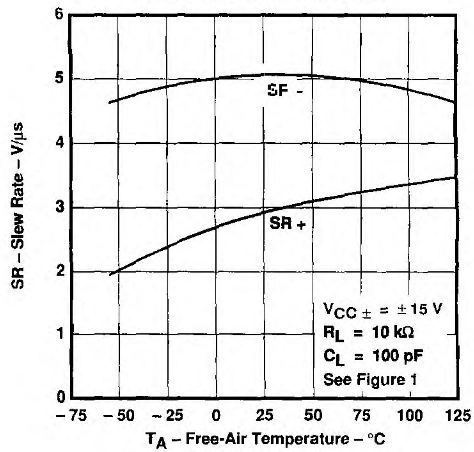


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

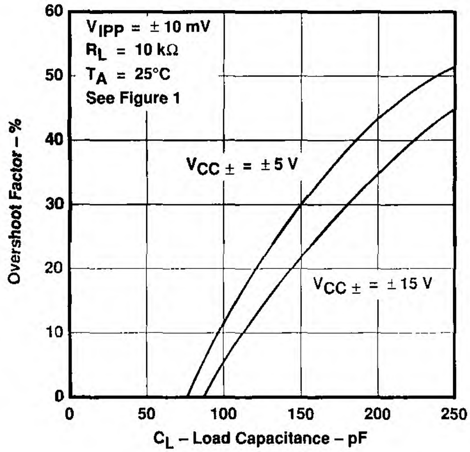


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

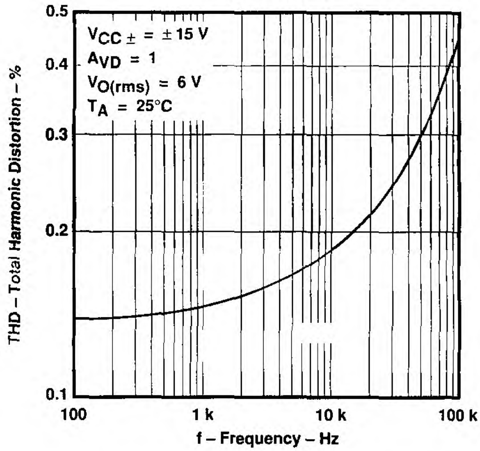


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

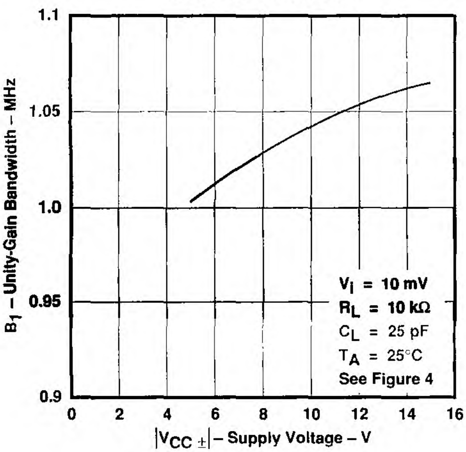


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

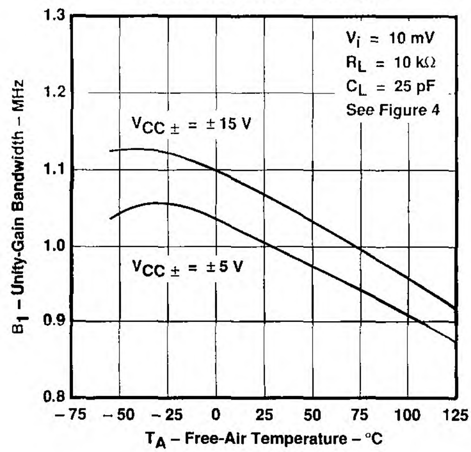


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

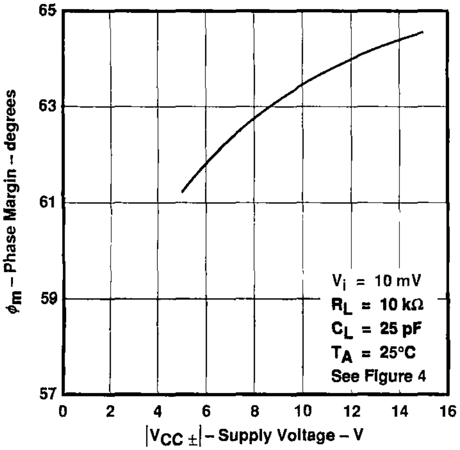


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

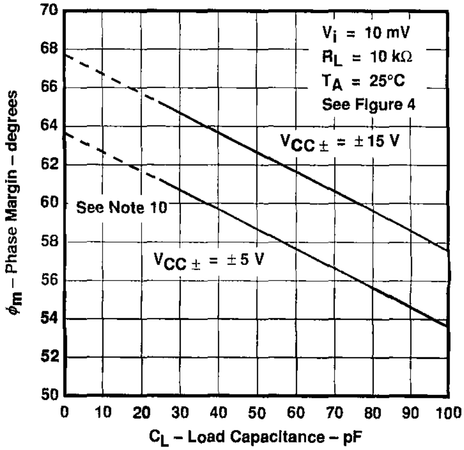


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

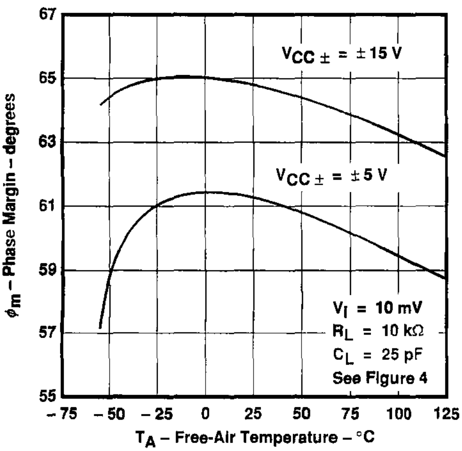


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

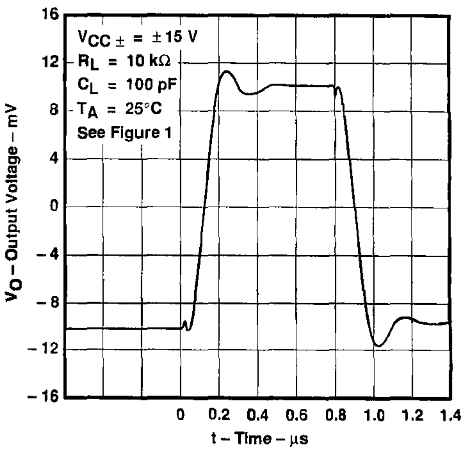


FIGURE 45

2 Operational Amplifiers

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

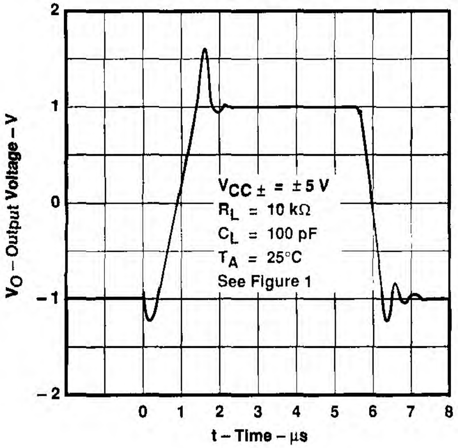


FIGURE 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

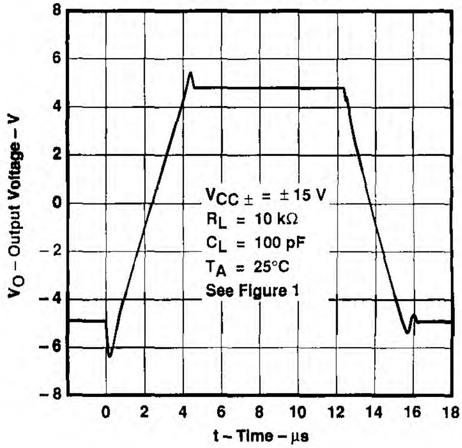


FIGURE 47

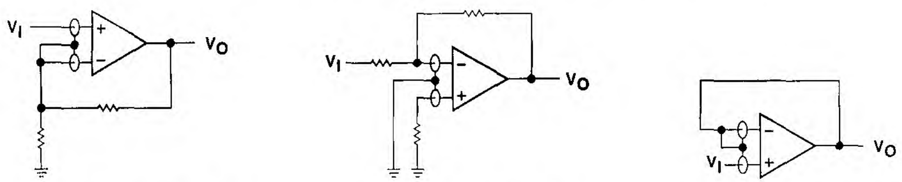
TYPICAL APPLICATION DATA

input characteristics

The TL032 and TL032A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL032 and TL032A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 48. USE OF GUARD RINGS

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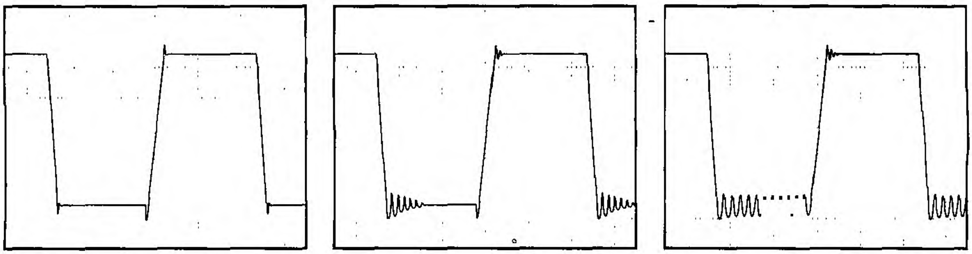
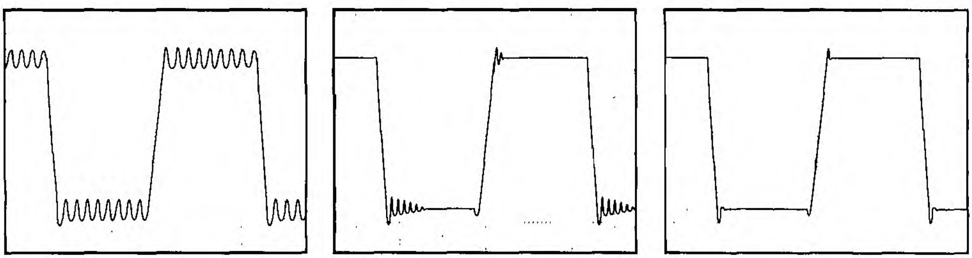
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL032 and TL032A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

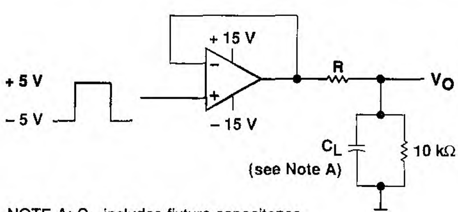


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

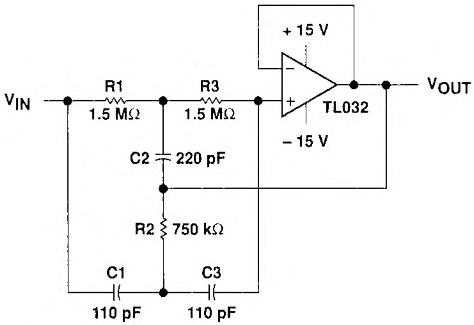
TYPICAL APPLICATION DATA

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. This circuit provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown below, the center frequency is 1 kHz. Note that $C1 = C3 = C2 \div 2$ and also that $R1 = R3 = 2 \times R2$. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.



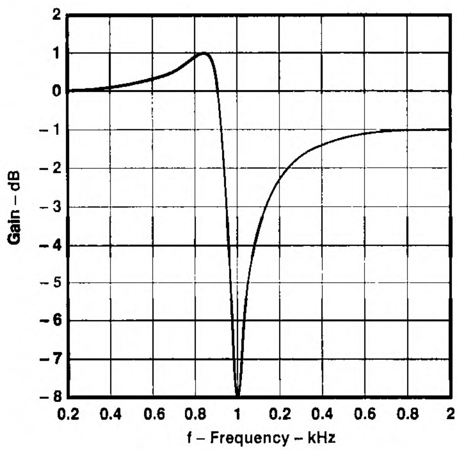


FIGURE 51. HIGH-Q NOTCH FILTER

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TYPICAL APPLICATION DATA

2-wire 4- to 20-mA current loop

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuit benefits from the high input impedance of the TL032A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the TL032A's non-inverting input is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA}$$

The current presently provides 4 to 20 mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL032A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA} - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Thanks to the low-power consumption of the TL032A, this circuit has at least 2 mA available to drive the actual sensor from the 5-V reference node.

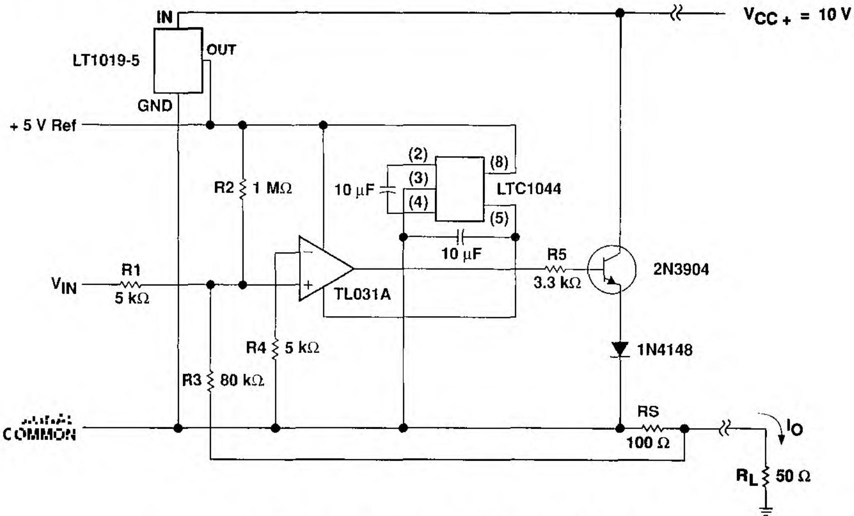

FIGURE 52. 2-WIRE 4- TO 20-mA CURRENT LOOP

TYPICAL APPLICATION DATA

low-level light detector preamplifier

Applications that need to detect small currents require high input impedance operational amplifiers; otherwise, the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL032 allows even the small currents resulting from low-level light to be detected.

In this circuit, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4l both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.

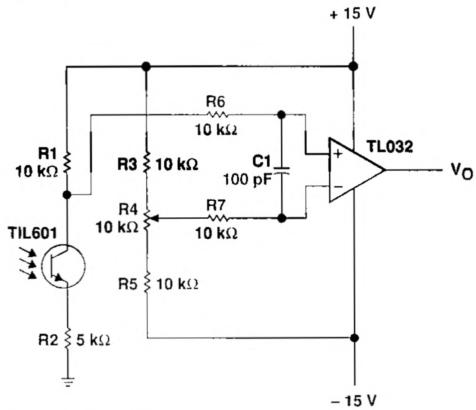

FIGURE 53. LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

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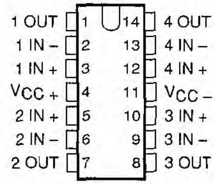
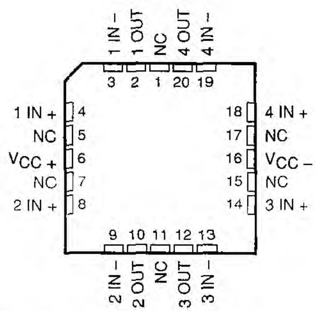
- **Maximum Offset Voltage . . . 1.5 mV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 26 mW Typ**
- **Output Short-Circuit Protection**
- **Monolithic Construction**

D, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL034 and TL034A quadruple operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL034 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL034 has been designed to be functionally compatible and pin compatible with the TL064.

Two offset voltage grades are available:
TL034 (4 mV max) and TL034A (1.5 mV max).

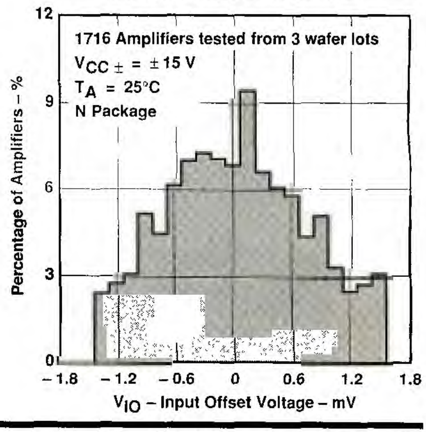
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	TL034ACD	——	TL034ACJ	TL034ACN
	4 mV	TL034CD	——	TL034CJ	TL034CN
– 40°C to 85°C	1.5 mV	TL034AID	——	TL034AIJ	TL0[illegible]
	4 mV	TL034ID	——	TL034IJ	T[illegible]
– [illegible] to 125°C	1.5 mV	TL0[illegible]	TL034AMFK	[illegible]AMJ	T[illegible]N
	4 mV	TL0[illegible]	TL0[illegible]	[illegible]MJ	TL0[illegible]

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL034CDR).

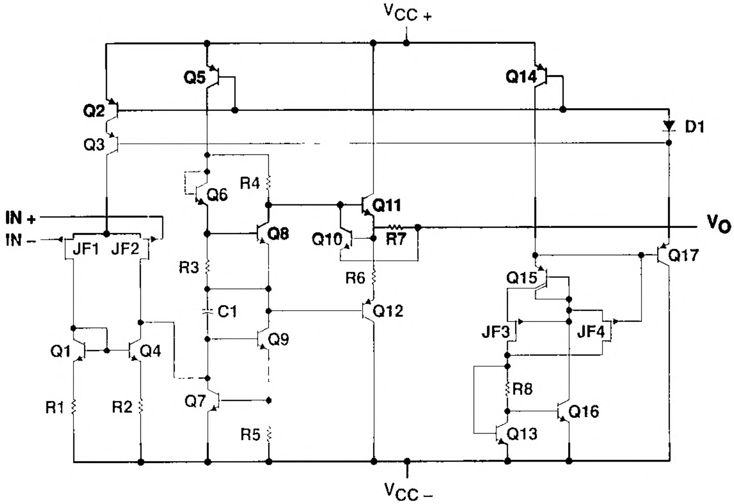
DISTRIBUTION OF TL034A
INPUT OFFSET VOLTAGE



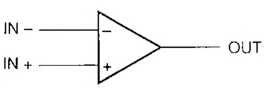
description (continued)

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 40 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	– 55°C to 125°C
I-suffix	– 40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE TA = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm}$ = ± 15 V	– 11.5		14	– 11.5		14	– 11.5		14	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

	PARAMETER	TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034M	25°C		0.91	6		0.78	[illegible]	mV
				Full range			11			9	
			TL034AM	25°C		0.7	3.5		0.58	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL034M	25°C to 125°C		10.6			10.9		µV/°C
			TL034AM	25°C to 125°C		10.6			10.9		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	[illegible]		4	15		
r_i	Input resistance			25°C		[illegible]			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				−55°C		4.6	10		18.7	34	
				125°C		7.1	10		[illegible]	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		[illegible]	1.12	mA
				−55°C		0.46	1		0.62	1.12	
				125°C		0.71	1		0.79	1.12	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			[illegible]		dB

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

2

Operational Amplifiers

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2		2	2.9		V/μs
			– 55°C		1.4		1.2	1.9		
			125°C		2.4		1.2	3.5		
SR –	Negative slew rate at unity gain		25°C		3.9		3	5.1		V/μs
			– 55°C		3.2		2.5	4.6		
			125°C		4.1		2.5	4.7		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			– 55°C		142			123		
			125°C		166			158		
t_f	Fall time		25°C		138			132		ns
			– 55°C		142			123		
			125°C		166			158		
	Overshoot factor		25°C		11%			5%		
			– 55°C		16%			6%		
			125°C		14%			8%		
V_n	Equivalent input noise voltage, TL034M	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		83			83		nV/√Hz
		f = 1 kHz			43			43		
	Equivalent input noise voltage, TL034AM	f = 10 Hz	25°C		83			83		
		f = 1 kHz			43			43		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			– 55°C		1			1.1		
			125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			– 55°C		57°			64°		
			125°C		59°			62°		

NOTE 7: For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					[illegible]	TYP	MAX	[illegible]	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034I	25°C		0.91	6		0.79	4	mV
				Full range			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL034I	25°C to 85°C		11.5			11.6		μV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	[illegible]		2	200	pA
				85°C		0.2	[illegible]		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	[illegible]		5	15.3		
r_i	Input resistance			25°C		[illegible]			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				−40°C		5.8	10		21.7	34	
				85°C		7.4	10		24.8	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				−40°C		0.58	1		0.72	1.12	
				85°C		0.74	1		[illegible]	1.12	
V_{O1}/V_{O2}	Cros [illegible]	$A_{VD} = 100$		25°C		[illegible]			[illegible]		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

8. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2		[illegible]	2.9		V/μs
			−40°C		1.6		1.5	2.1		
			85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			−40°C		3.3		3.2	4.8		
			85°C		4.1		3.2	4.9		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			−40°C		132			123		
			85°C		154			146		
t_f	Fall time		25°C		138			132		ns
			−40°C		132			123		
			85°C		154			146		
	Overshoot factor		25°C		11%			5%		
			−40°C		12%			5%		
			85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9) — TL034I	R_S = 100 Ω, See Figure 3; f = 10 Hz	25°C		83			83		nV/√Hz
	TL034I	f = 1 kHz			43			43		
	TL034AI	f = 10 Hz	25°C		83			83		
	TL034AI	f = 1 kHz			43			43	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			−40°C		1			1.1		
			85°C		0.9			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			−40°C		60°			65°		
			85°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

	PARAMETER	TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034C	25°C		0.91	6		0.79	4	mV
				Full range			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL034C	25°C to 70°C		11.6			12		μV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	[illegible]		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	−3	−4.2		−12.5	[illegible]		V
				0°C	−3	−4.1		−12.5	[illegible]		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				0°C		7.4	10		25.3	34	
				70°C		7.6	10		[illegible]	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		[illegible]	1.12	mA
				0°C		0.74	1		0.85	1.12	
				70°C		0.76	1		0.84	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.
8. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

2

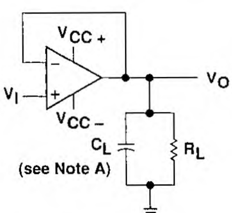
Operational Amplifiers

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7	25°C		2		2	2.9		V/µs
			0°C		1.8		1.5	2.6		
			70°C		2.2		2	3.2		
SR –	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/µs
			0°C		3.7		3.2	5.0		
			70°C		4		3.2	5.0		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			0°C		134			127		
			70°C		[illegible]			142		
t_f	Fall time		25°C		[illegible]			132		ns
			0°C		[illegible]			127		
			70°C		150			142		
	Overshoot factor		25°C		11%			5%		
			0°C		[illegible]			4%		
			70°C		[illegible]			6%		
V_n	Equivalent input noise voltage (see Note 9), TL034C	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		83			83		nV/√Hz
	TL034C	f = 1 kHz			43			43		
	TL034AC	f = 10 Hz	25°C		83			83		
	TL034AC	f = 1 kHz			43			43	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			0°C		1			1.1		
			70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			0°C		61°			65°		
			70°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

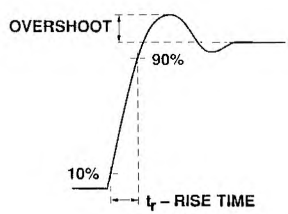


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

2 Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION

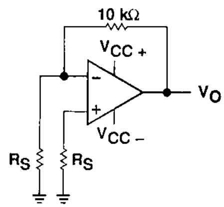
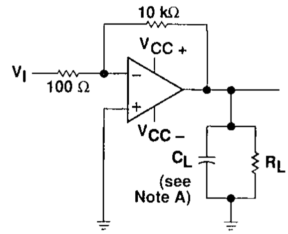


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

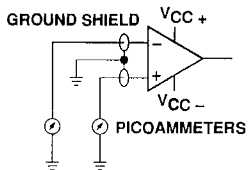


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL034 and TL034A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	[illegible]
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_{ID}	[illegible]ential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 16, 17 15 18, 19
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	20 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	24, 25 26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	28 29 30
I_{CC}	Supply current	vs V_{CC} vs Temperature	32 33
SR	Slew rate	vs R_L vs Temperature	34, 35 36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	40 41
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	42 43 44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal Large-signal	45 46, 47

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE

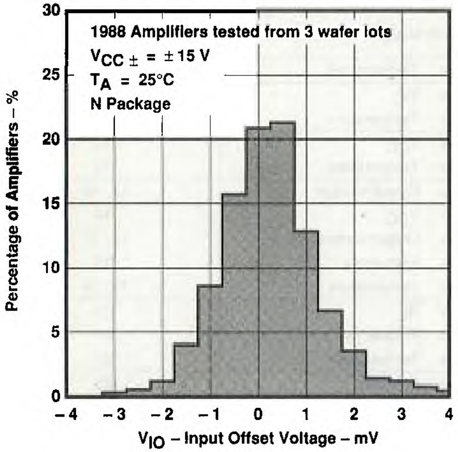

FIGURE 6

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

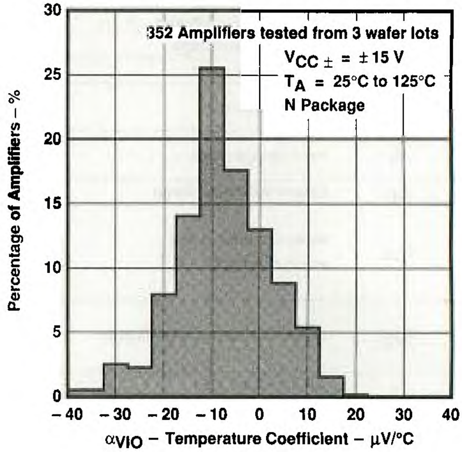

FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

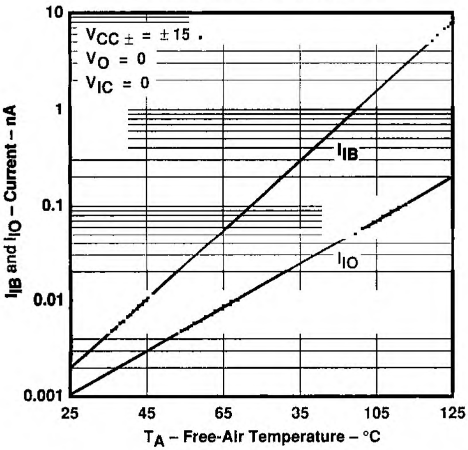

FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

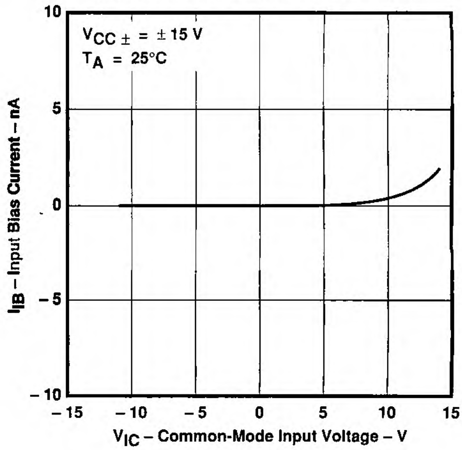

FIGURE 9

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

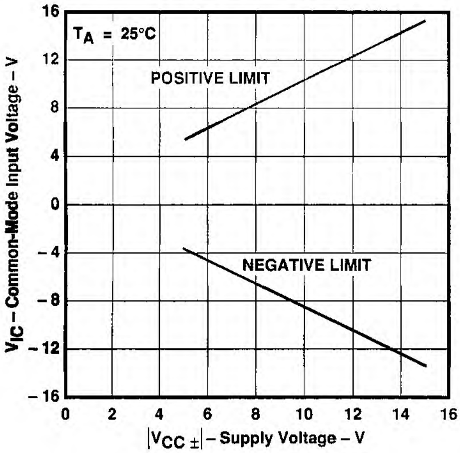

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

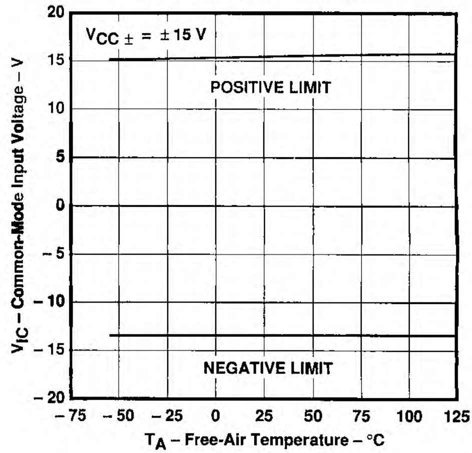

FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

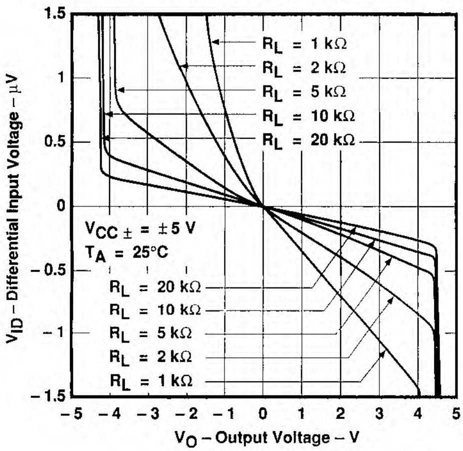

FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

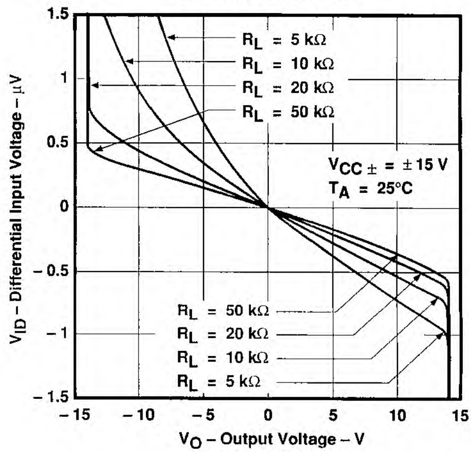

FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

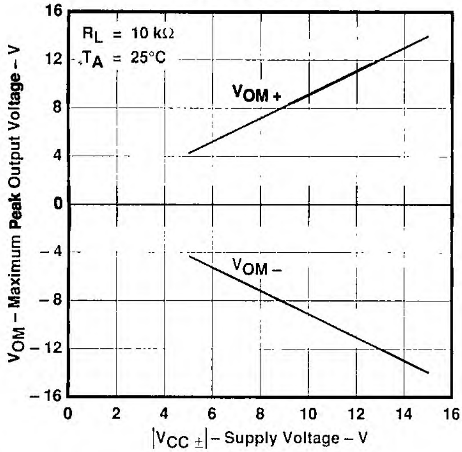

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

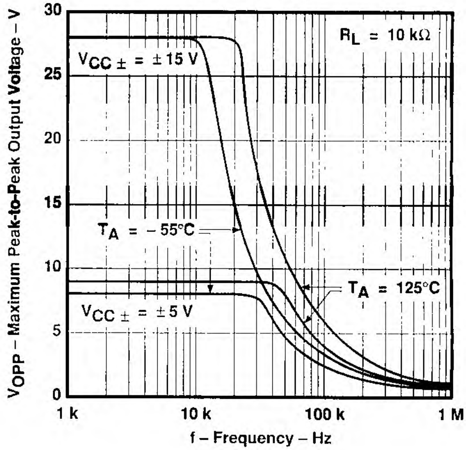

FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

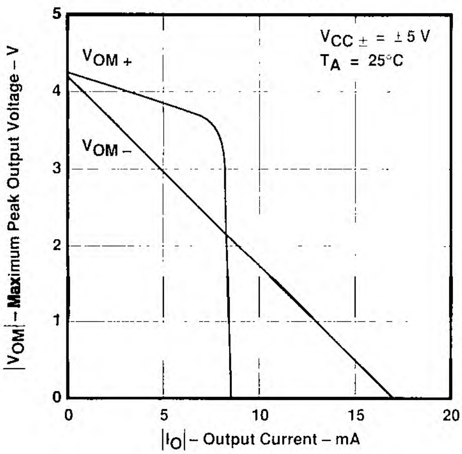

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

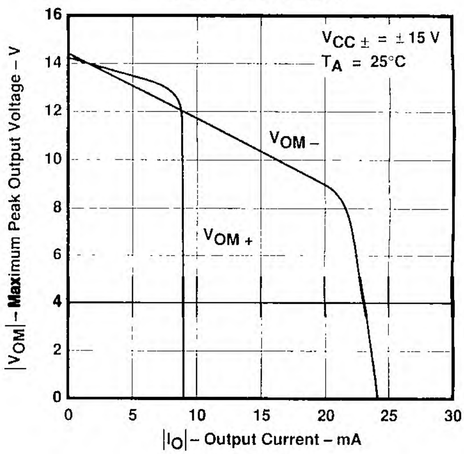

FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

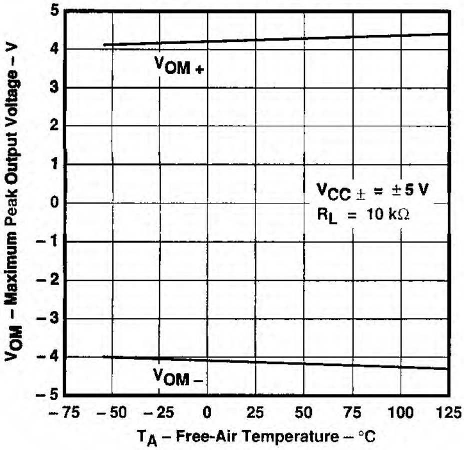

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

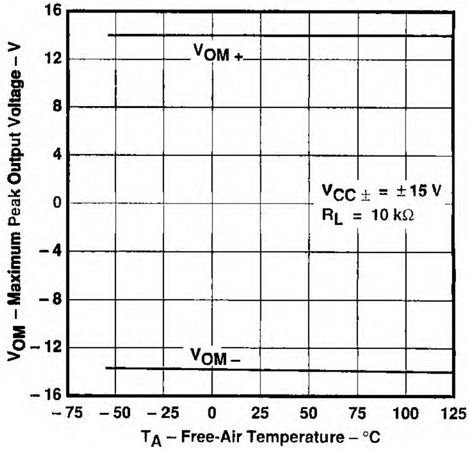

FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

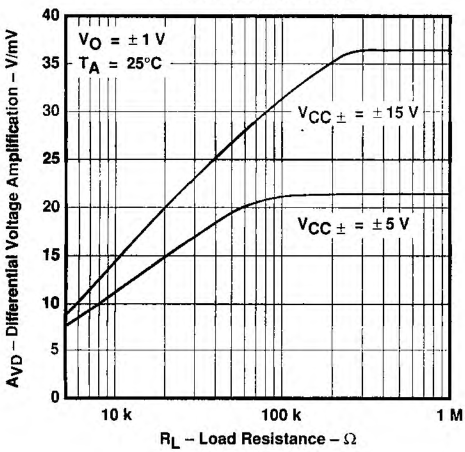

FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

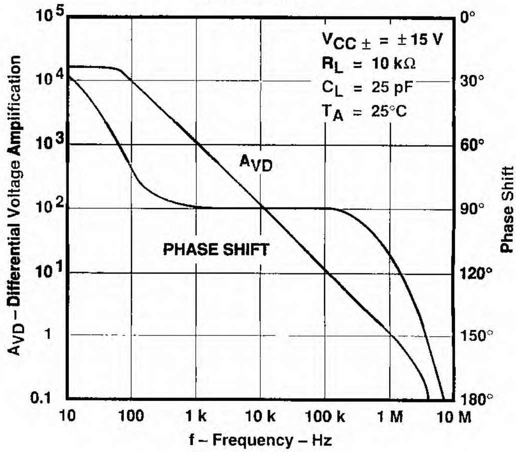

FIGURE 21

Operational Amplifiers

2

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

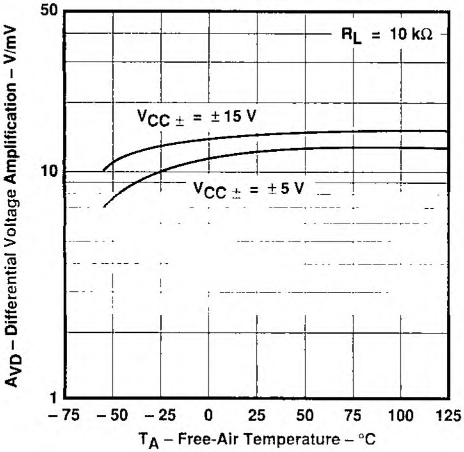

FIGURE 22

OUTPUT IMPEDANCE vs FREQUENCY

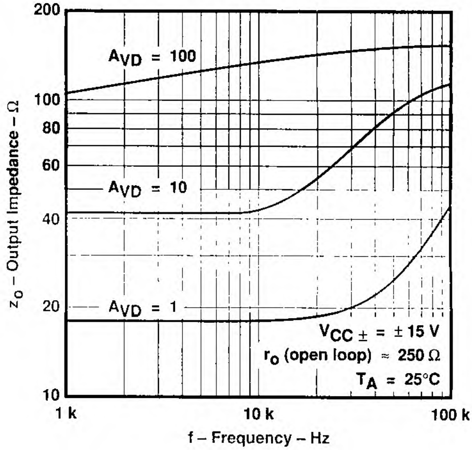

FIGURE 23

COMMON-MODE REJECTION RATIO vs FREQUENCY

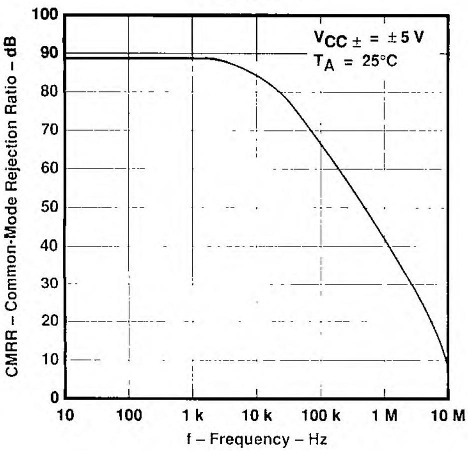

FIGURE 24

COMMON-MODE REJECTION RATIO vs FREQUENCY

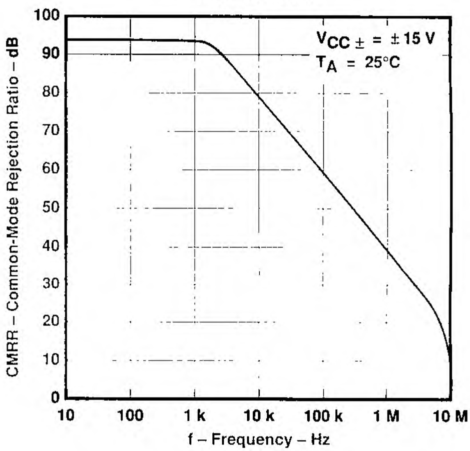

FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

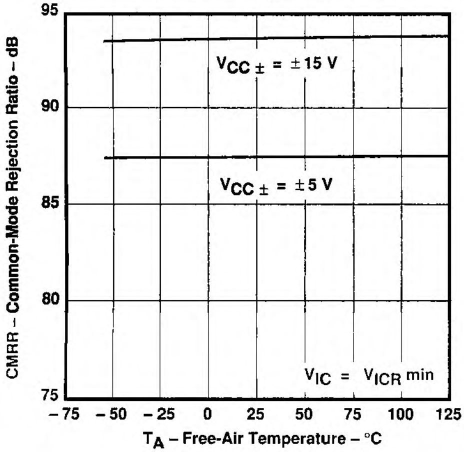

FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

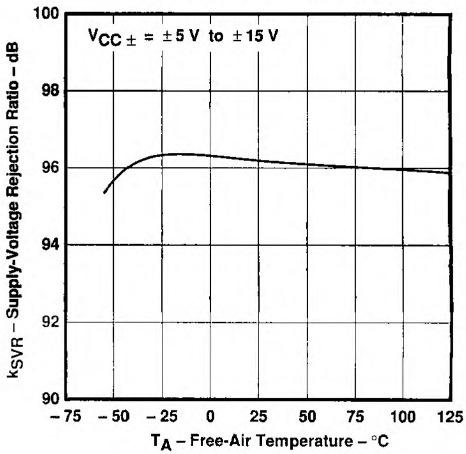

FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

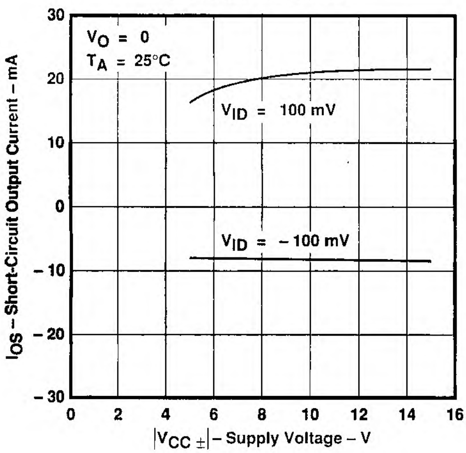

FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

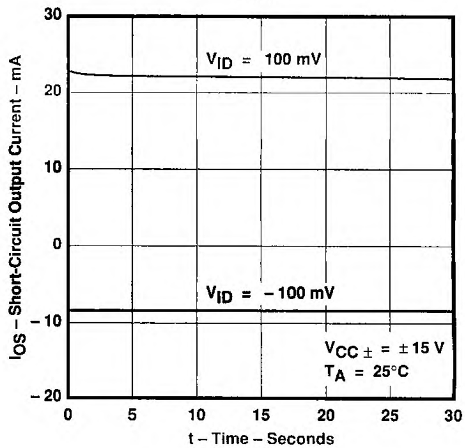

FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

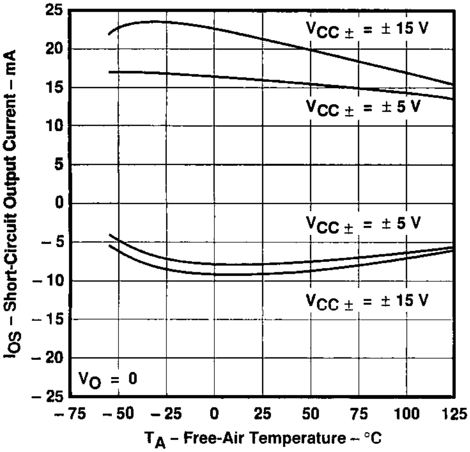

FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

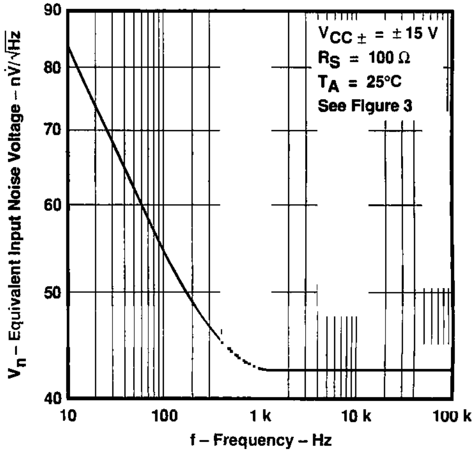

FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

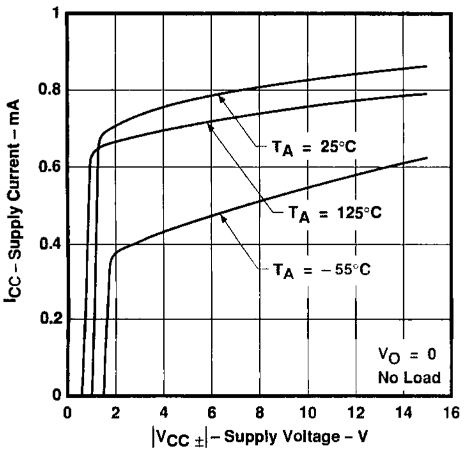

FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

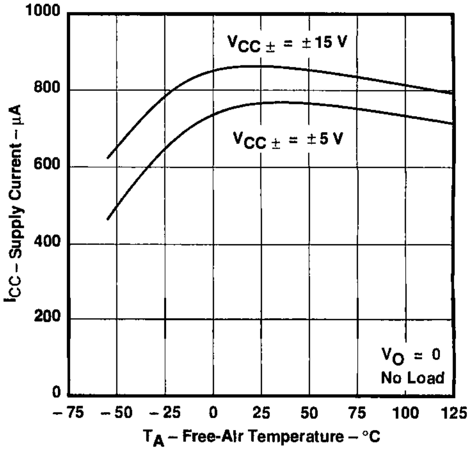

FIGURE 33

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

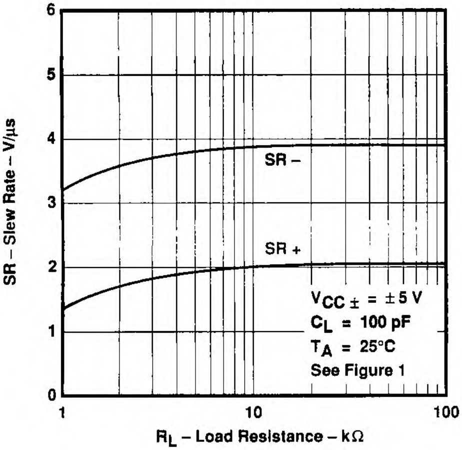


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

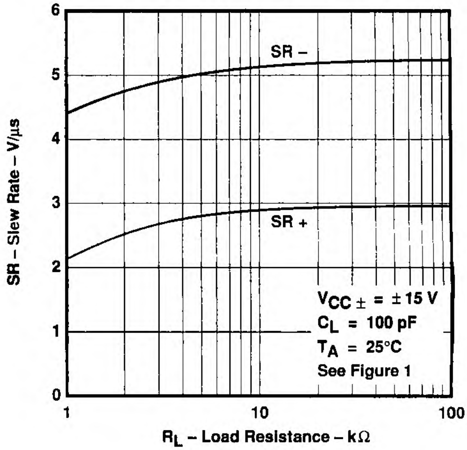


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

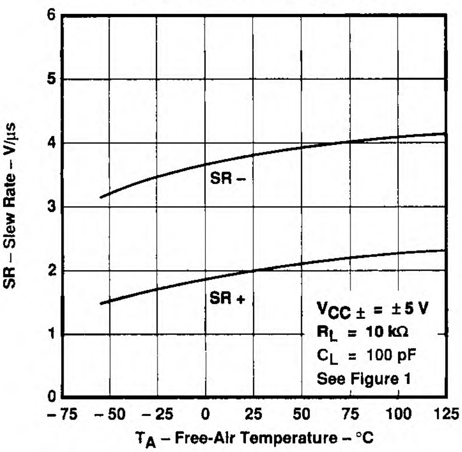


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

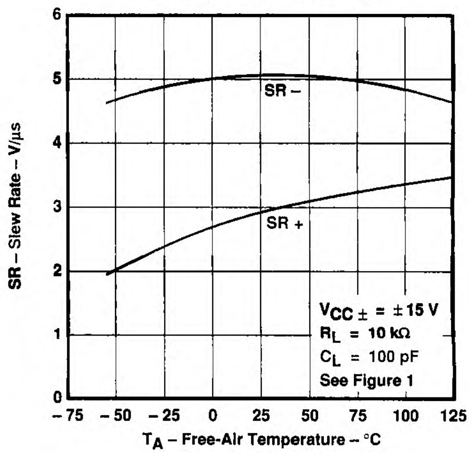


FIGURE 37

2
Operational Amplifiers

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

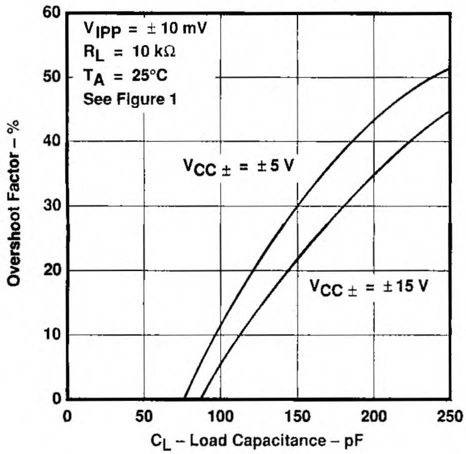


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

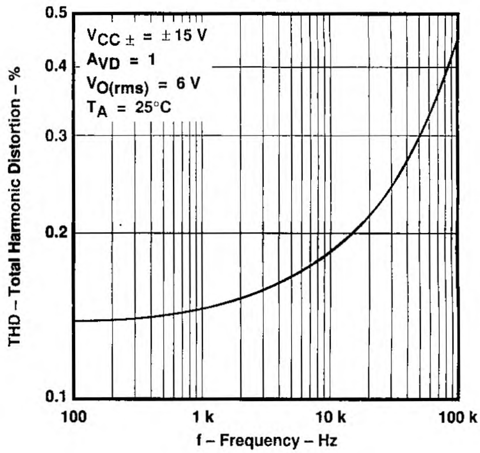


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

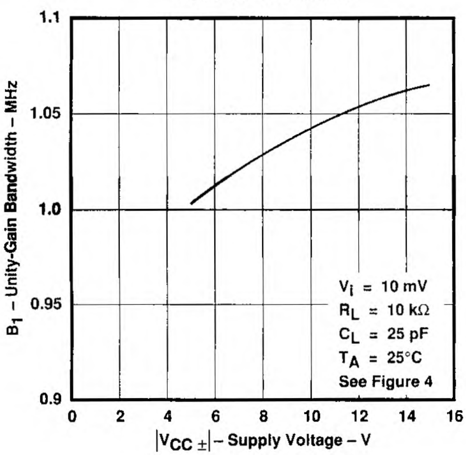


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

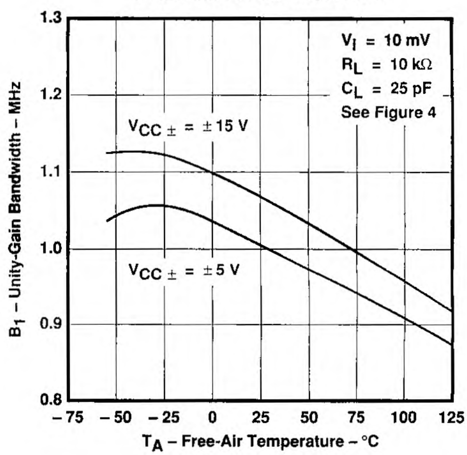


FIGURE 41

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

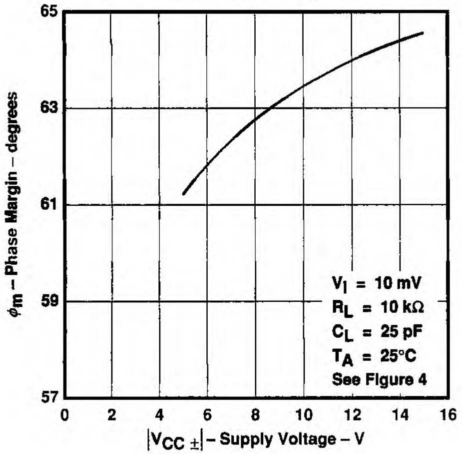


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

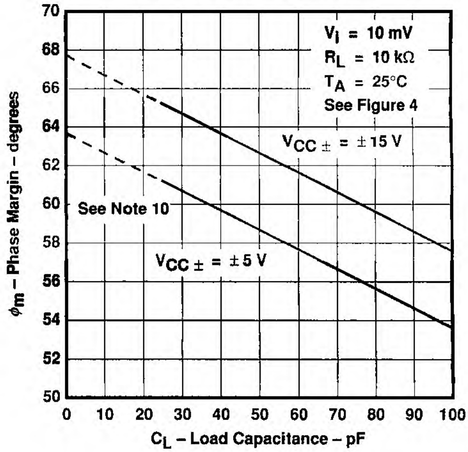


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

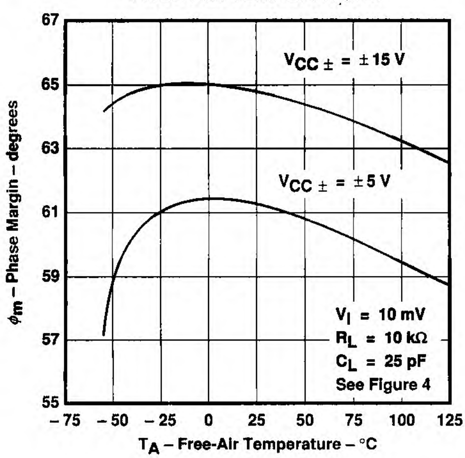


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

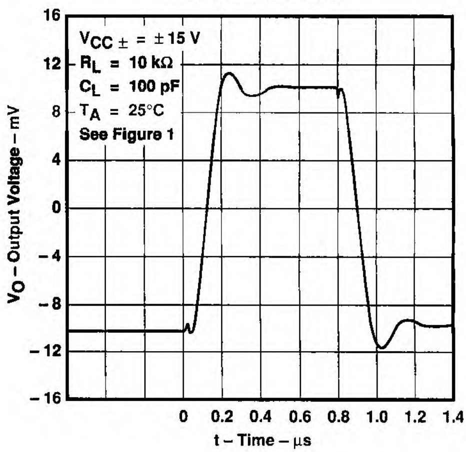


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

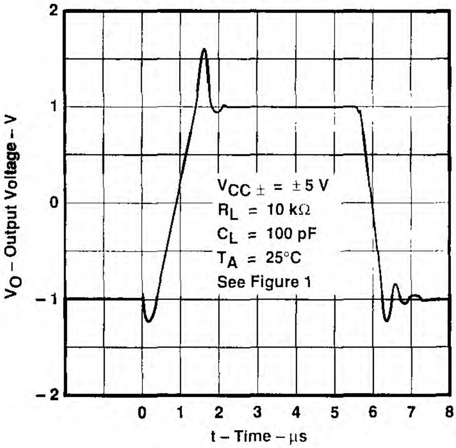


FIGURE 46

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

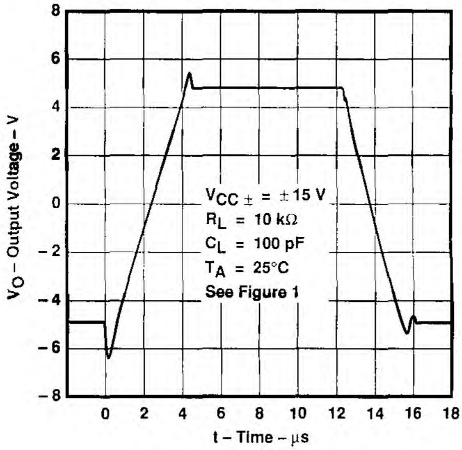


FIGURE 47

TYPICAL APPLICATION DATA

input characteristics

The TL034 and TL034A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL034 and TL034A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

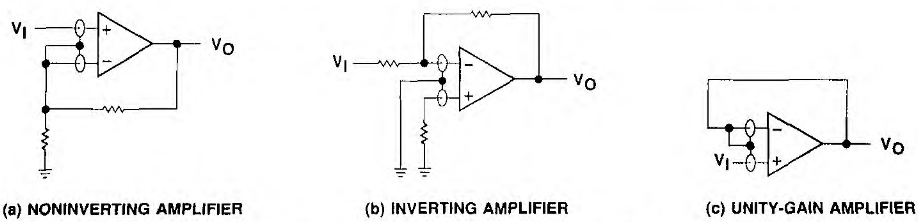
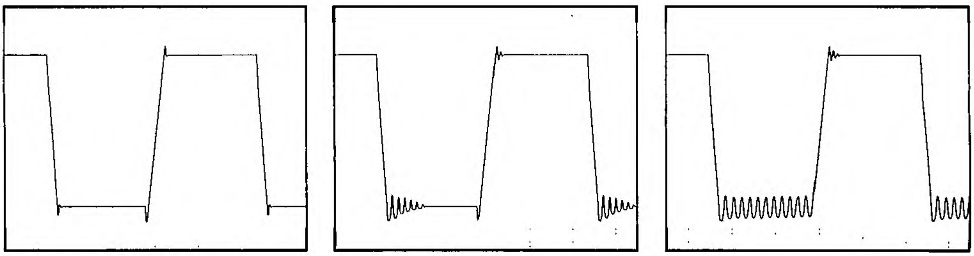


FIGURE 48. USE OF GUARD RINGS

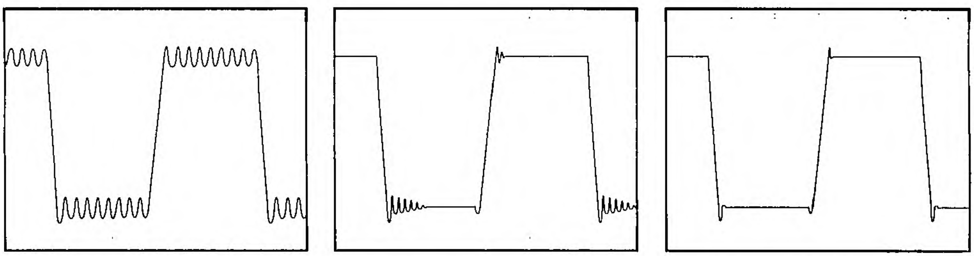
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL034 and TL034A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

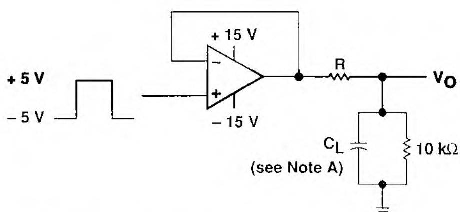


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



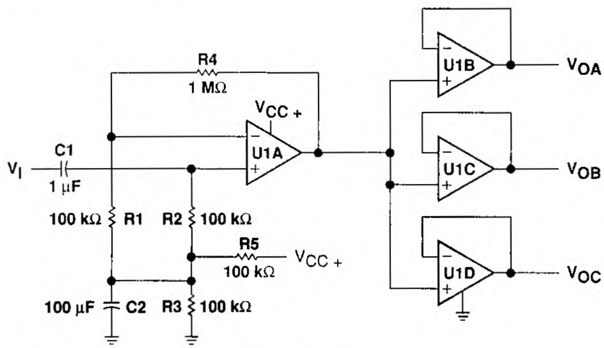
NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

audio distribution amplifier

This audio distribution amplifier feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10 while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL034 allows quick response to the input signal while maintaining low power consumption.



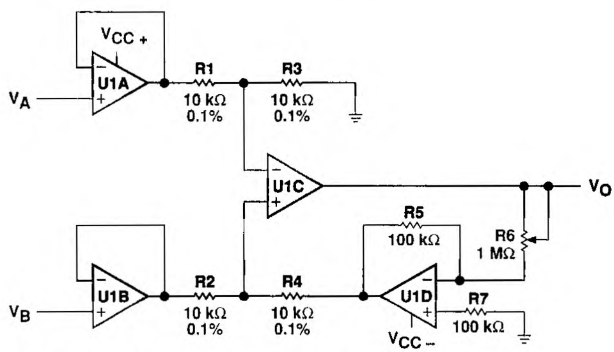
NOTE : U1A through U1D = TL034; V_{CC+} = 5 V.

instrumentation amplifier with linear gain adjust

The TL034 low-offset voltage and low-power consumption provides an accurate but inexpensive instrumentation amplifier. This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 should always be greater or equal to the value of R5 in order to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1% tolerance resistors.



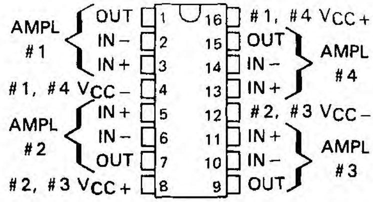
NOTE : U1A through U1D = TL034; $V_{CC\pm}$ = ± 15 V.

D1662, SEPTEMBER 1973—REVISED JUNE 1988

- Very Low Power Consumption
- Typical Power Dissipation with ±2-V Supplies . . . 340 μW
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Input Offset Voltage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Power Applied in Pairs

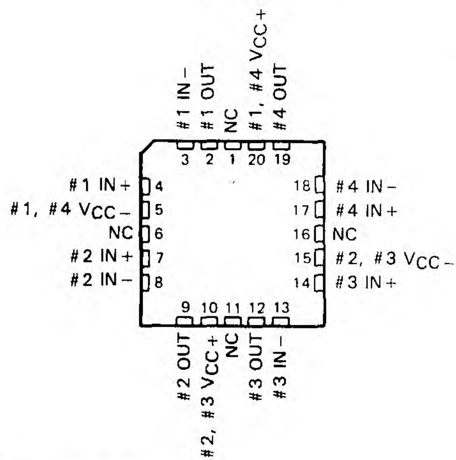
TL044M IS NOT RECOMMENDED FOR NEW DESIGNS.

TL044M . . . J OR W DUAL-IN-LINE PACKAGE
TL044C . . . J OR N PACKAGE
(TOP VIEW)



Pins 4 and 12 are internally connected together in the N package only.

TL044M . . . FK PACKAGE
(TOP VIEW)



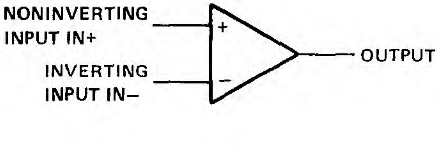
NC—No internal connection

description

The TL044 is a quad low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use. Power may be applied separately to Section A (amplifiers 1 and 4) or Section B (amplifiers 2 and 3) while the other pair remains unpowered.

The TL044M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL044C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)
0°C to 70°C	5 mV	–	TL044CJ	TL044CN	–
−55°C to 125°C	5 mV	TL044MFK	TL044MJ	–	TL044MW

2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL044M	TL044C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
[illegible] ly voltage V_{CC-} (see Note 1)		−22	−18	V
[illegible]rential input voltage (see Note 2)		±30	±30	V
[illegible] voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to [illegible]	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to [illegible]	°C
Case temperature for 60 seconds	FK package	[illegible]		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	[illegible]	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N package		[illegible]	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL044M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 85°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	680 mW	11.0 mW/°C	88°C	680 mW	[illegible] mW
J (TL044M)	680 mW	11.0 mW/°C	88°C	680 mW	275 mW
J (TL044C)	680 mW	8.2 mW/°C	67°C	656 mW	–
N	680 mW	N/A	N/A	680 mW	–
W	680 mW	8.0 mW/°C	65°C	640 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL044M MIN	TL044M TYP	TL044M MAX	TL044C MIN	TL044C TYP	TL044C MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	40		15	80	nA
			Full range			100			[illegible]	
I_{IB}	Input bias current	V_O = 0	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V	25°C	72	86		60	80		dB
			Full range	66			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	[illegible]		30	150		30	200	µV/V
			Full range			150			[illegible]	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0 V	25°C		250	400		[illegible]	500	µA
			Full range			400			500	
P_D	Total dissipation (four amplifiers)	No load, V_O = 0 V	25°C		7.5	12		7.5	15	mW
			Full range			12			15	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for TL044M is −55°C to 125°C and for TL044C is 0°C to 70°C.

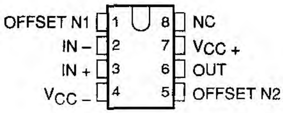
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL044M MIN	TL044M TYP	TL044M MAX	TL044C MIN	TL044C TYP	TL044C MAX	UNIT
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ,		0.3			0.3		µs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.5			0.5		V/µs

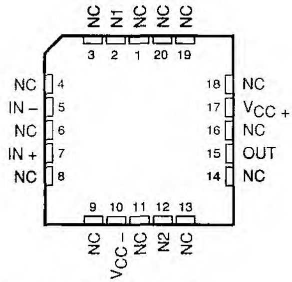
D3234, JUNE 1988 – REVISED FEBRUARY 1989

- **Maximum Offset Voltage . . . 800 μV (TL051A)**
- **High Slew Rate . . . 19.8 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 18 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE
(TOP VIEW)

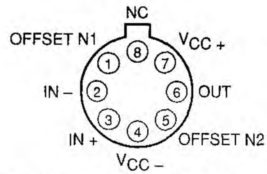


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 is in electrical contact with the case

description

The TL051 and TL051A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

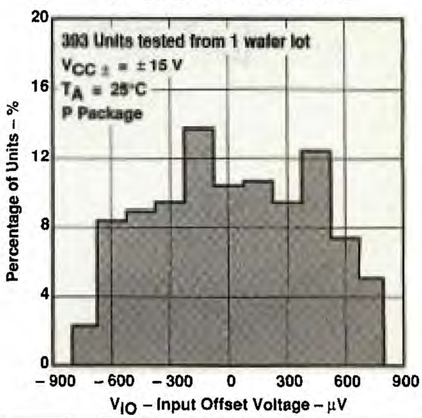
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL051 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL051 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 μV	TL051ACD	—	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	—	[illegible]	[illegible]	[illegible]
– 40°C to 85°C	[illegible]	[illegible]	—	[illegible]	[illegible]	[illegible]
	1500 μV	[illegible]	—	[illegible]	[illegible]	[illegible]
– 55°C to 125°C	800 μV	[illegible]	TL051AMFK	[illegible]	[illegible]	[illegible]
	1500 μV	[illegible]	TL051MFK	[illegible]	[illegible]	[illegible]

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL051CDR).

DISTRIBUTION OF TL051A
INPUT OFFSET VOLTAGE



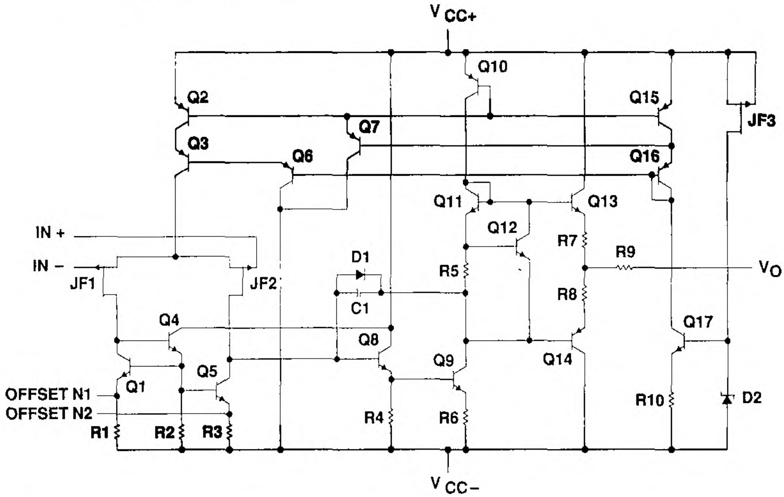
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL071 and TL081. Two offset voltage grades are available: TL051 (1.5 mV max) and TL051A (800 μV max).

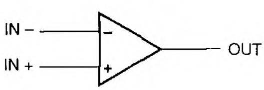
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) .... 18 V
Supply voltage, V_{CC-} (see Note 1) .... – 18 V
Differential input voltage (see Note 2) .... ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) .... ± 15 V
Input current, I_I (each input) .... ± 1 mA
Output current, I_O (each output) .... ± 80 mA
Total current into V_{CC+} terminal .... 160 mA
Total current out of V_{CC-} terminal .... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... – 55°C to 125°C
I-suffix .... – 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A < 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible] mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		[illegible]		± 15	[illegible]		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051M	25°C		0.75	3.5		0.59	1.5	mV
				Full range			6.5			4.5	
			TL051AM	25°C		0.55	2.8		0.35	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL051M	25°C to 125°C		8			8		µV/°C
			TL051AM	25°C to 125°C		8			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		[illegible]	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		[illegible]	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	[illegible]		15	49		
r_i	Input resistance			25°C		[illegible]			[illegible]		Ω
C_i	Input [illegible]			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				−55°C		2.3	3.2		2.4	3.2	
				125°C		2.4	3.2		2.5	3.2	

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/µs
				– 55°C		17.5			20		
				125°C		15			21.2		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				– 55°C		15.1			17		
				125°C		14.8			18.2		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				– 55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			[illegible]		
				– 55°C		25%			19%		
				[illegible]		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				– 55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				– 55°C		57°			61°		
				125°C		59°			62°		

† Full range is – 55°C to 125°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051I	25°C		0.75	3.5		0.59	1.5	mV
				Full range			5.3			3.3	
			TL051AI	25°C		0.55	2.8		0.35	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051I	25°C to 85°C		7			8		μV/°C
			TL051AI	25°C to 85°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		[illegible]	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			[illegible]		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				−40°C		2.4	3.2		2.6	3.2	
				85°C		2.5	3.2		2.6	3.2	

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1 and Note 7	25°C		18.2		15	23.7		V/µs
			– 40°C		20.1		13	23		
			85°C		16.1		13	21.9		
SR –	Negative slew rate at unity gain		25°C		16.5		15	19.8		
			– 40°C		16.6		13	19.4		
			85°C		15.7		13	19.1		
t_r	Rise time	$V_{IPP} = \pm 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2	25°C		55			56		ns
			– 40°C		52			53		
			85°C		64			65		
t_f	Fall time		25°C		55			57		
			– 40°C		51			53		
			85°C		64			65		
	Overshoot factor		25°C		24%			19%		
			– 40°C		24%			19%		
			85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	$R_S = 100$ Ω, See Figure 3; f = 10 Hz	25°C		75			75		nV/√Hz
		$R_S = 100$ Ω, See Figure 3; f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage	$R_S = 100$ Ω, See Figure 3; f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 8	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		3			3.1		MHz
			– 40°C		3.5			3.6		
			85°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		[illegible]			62°		
			– 40°C		58°			61°		
			85°C		59°			62°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, [illegible]) = 1 V; for $V_{CC\pm} = \pm 15$ V, $V_{o(rms)} = 6$ V.

10. This parameter is teste[illegible] sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051C	25°C		0.75	3.5		0.59	1.5	mV
				Full range			4.5			2.5	
			TL051AC	25°C		0.55	2.8		0.35	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051C	25°C to 70°C		8			8		µV/°C
			TL051AC	25°C to 70°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$			−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				0°C		2.7	3.2		2.8	3.2	
				70°C		2.6	3.2		2.7	3.2	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

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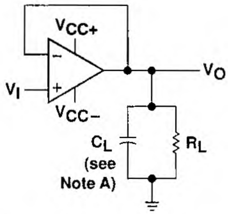
operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/μs
				0°C		19.5		13	24.1		
				70°C		16.4		13	22.6		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				0°C		16.8		13	19.9		
				70°C		16		13	19.3		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			[illegible]		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				0°C		3.2			3.3		
				70°C		2.7			2.8		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				0°C		58°			62°		
				70°C		59°			62°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
8. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

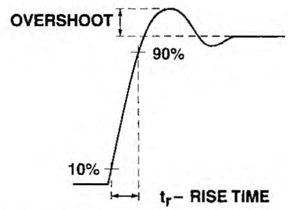


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

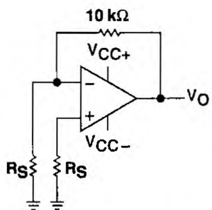
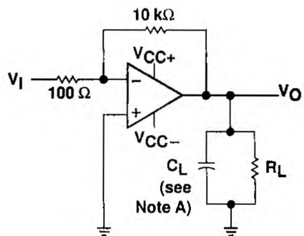


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

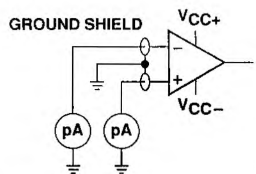


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp-bias-current level typical of the TL051 and TL051A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	[illegible]
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE

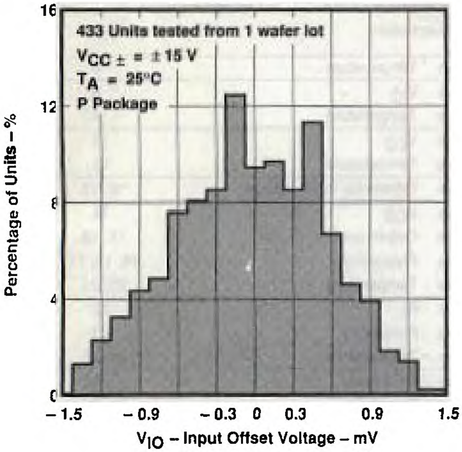

FIGURE 6

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

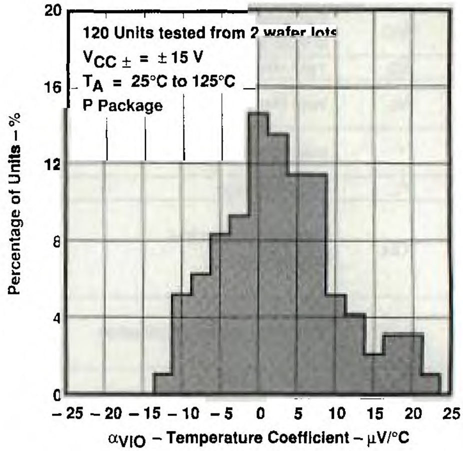

FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

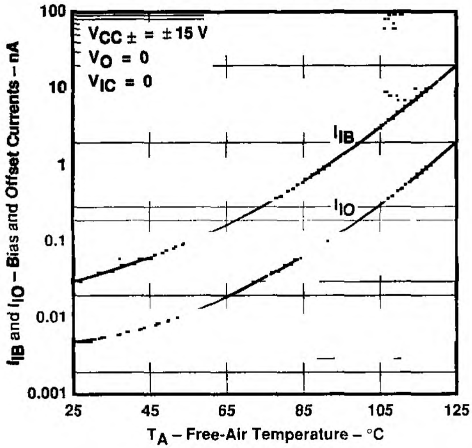

FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

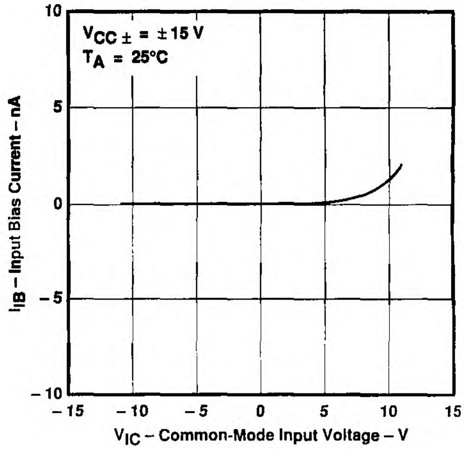

FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

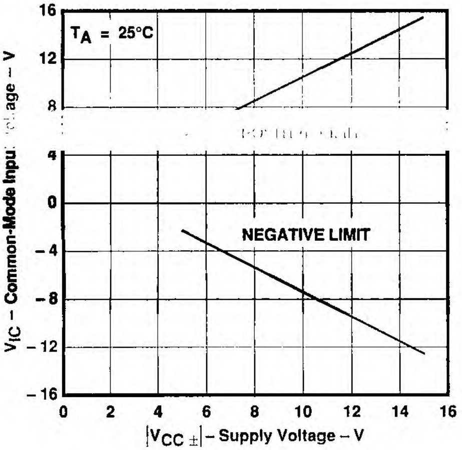

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

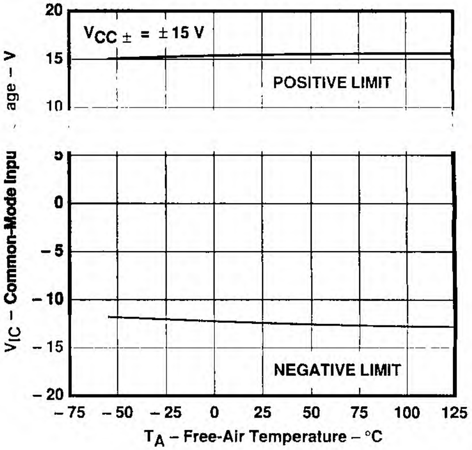

FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

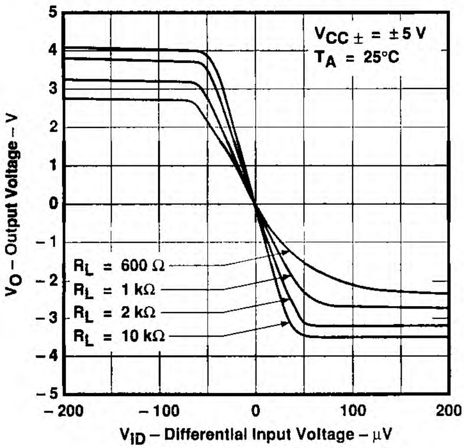

FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

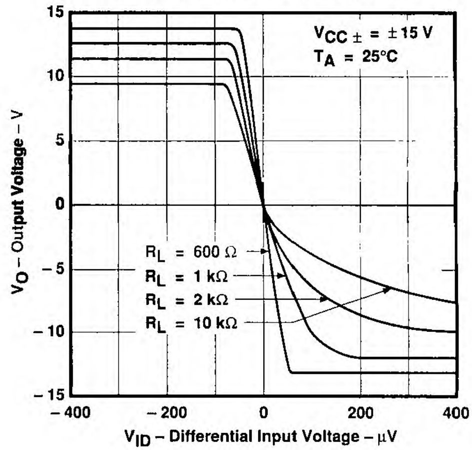

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

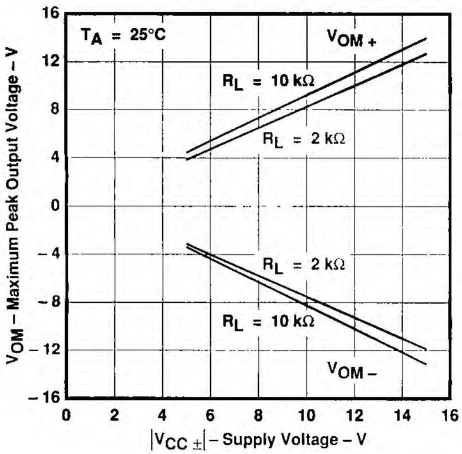

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

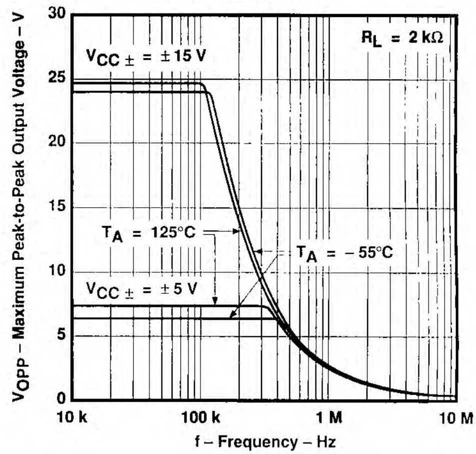

FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

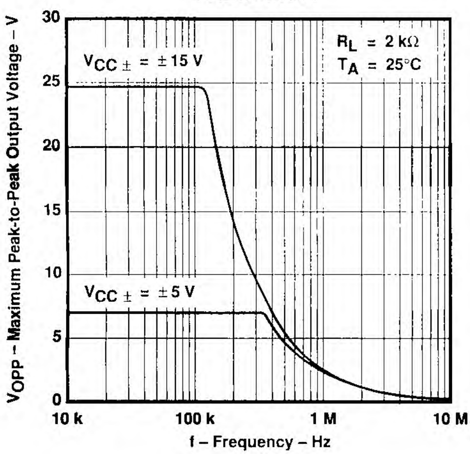

FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

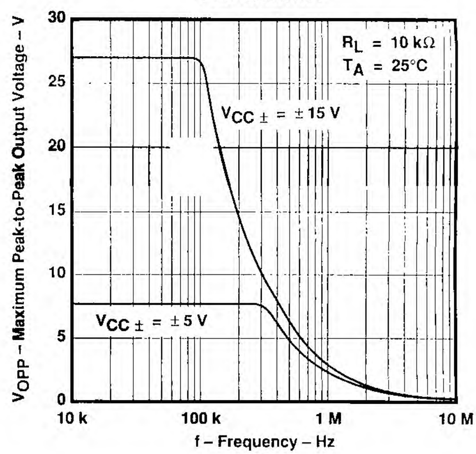

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

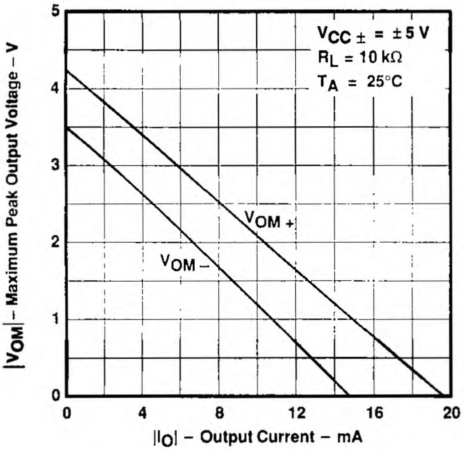

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

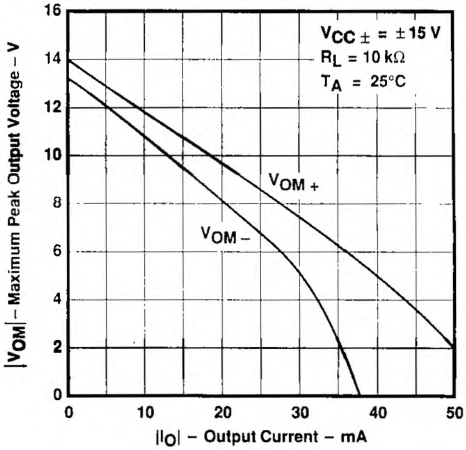

FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

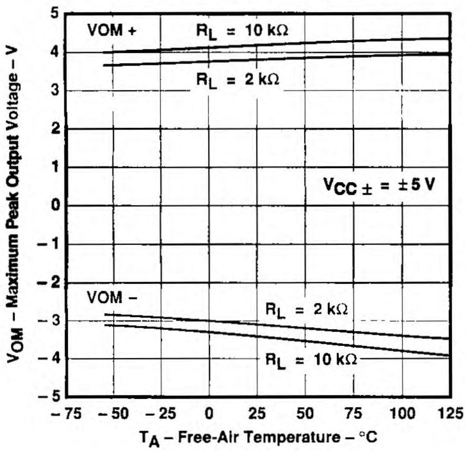

FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

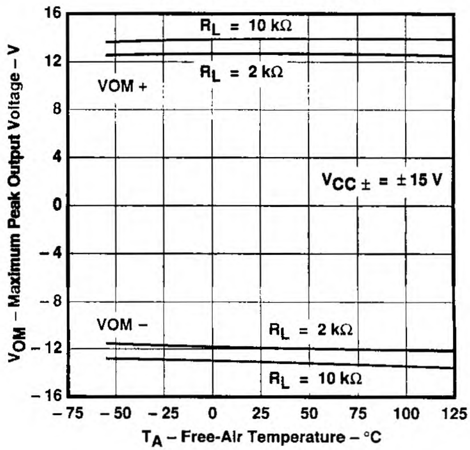

FIGURE 21

2 Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

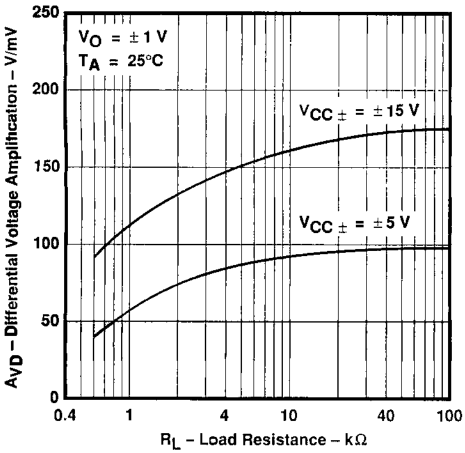

FIGURE 22

LARGE- ·:·.AL DIFFERENTIAL VOLTAGE
AMPI ·· · ATION AND PHASE SHIFT
vs
FREQUENCY

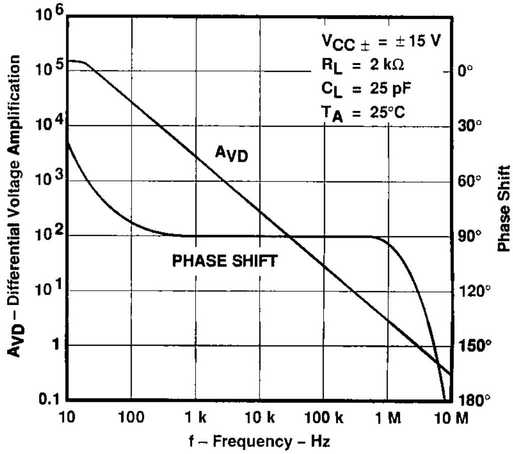

FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

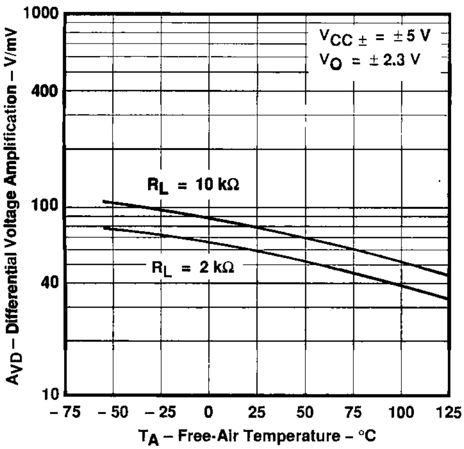

FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

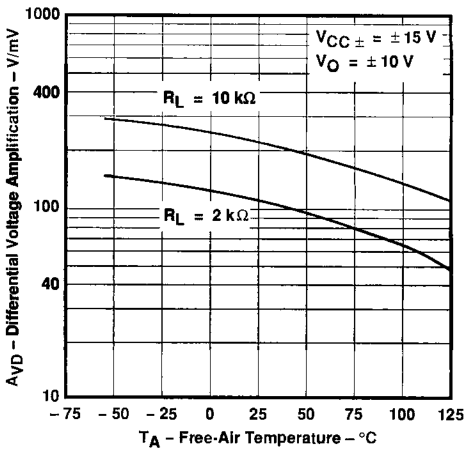

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

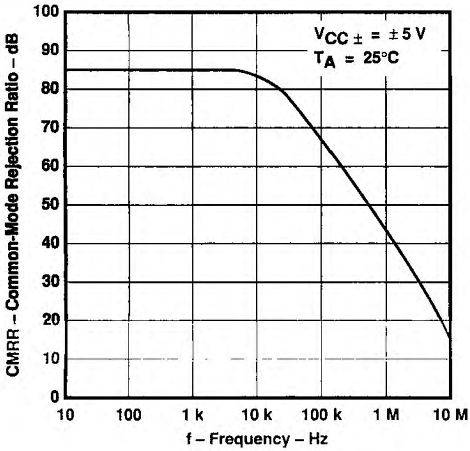

FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

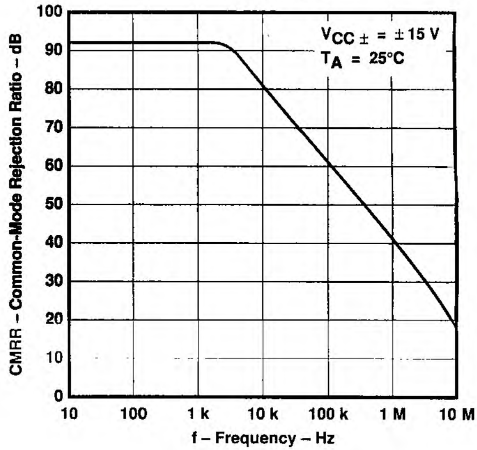

FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

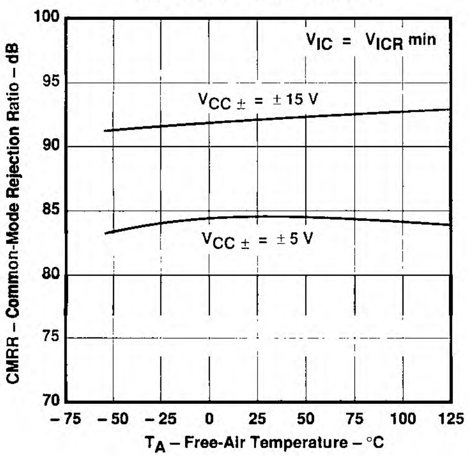

FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

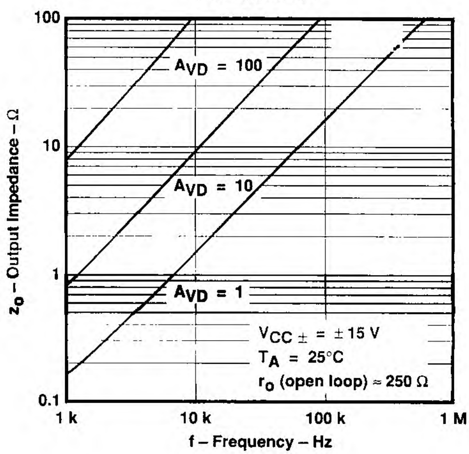

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

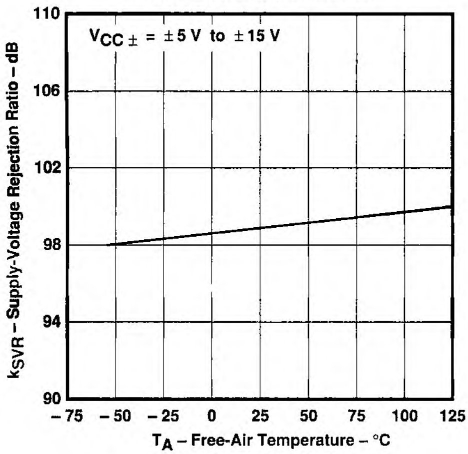

FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

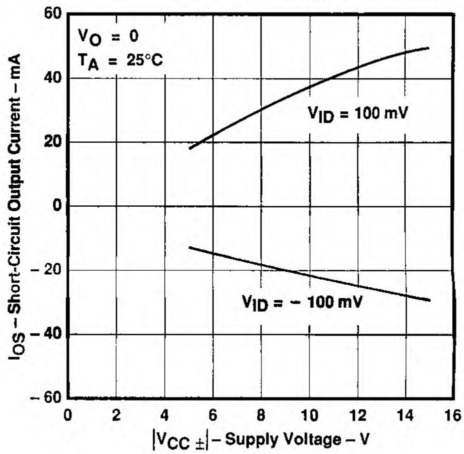

FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

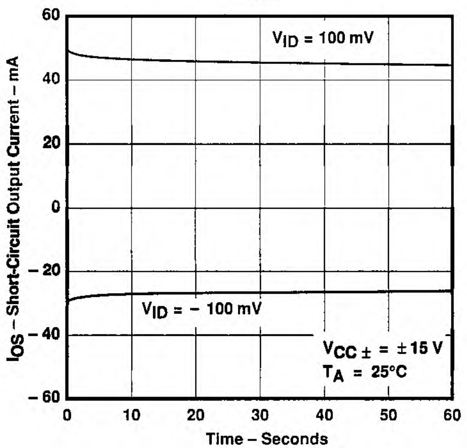

FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

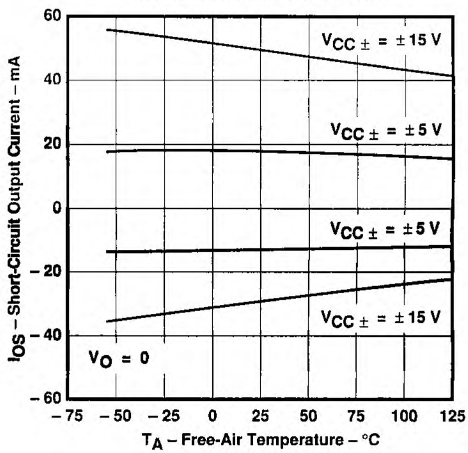

FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

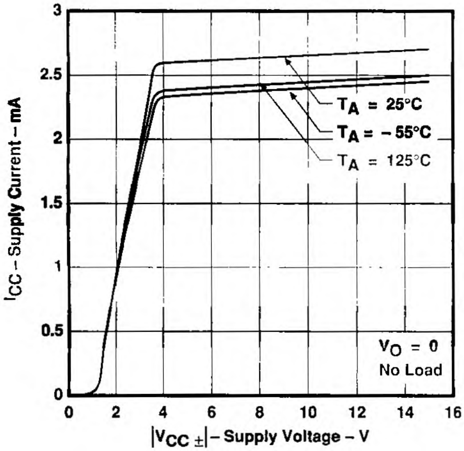

FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

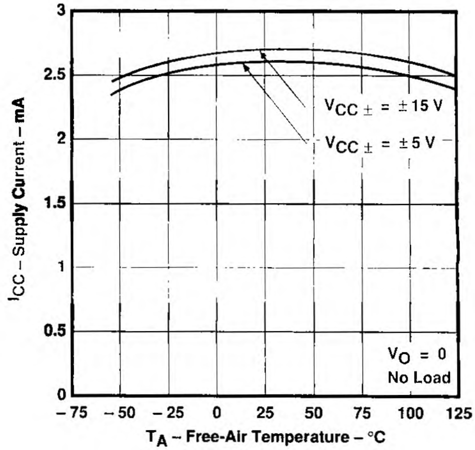

FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

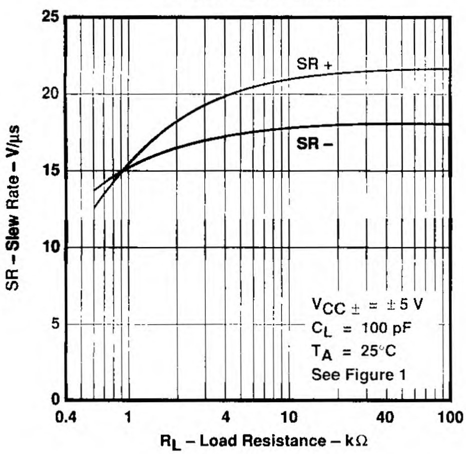

FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

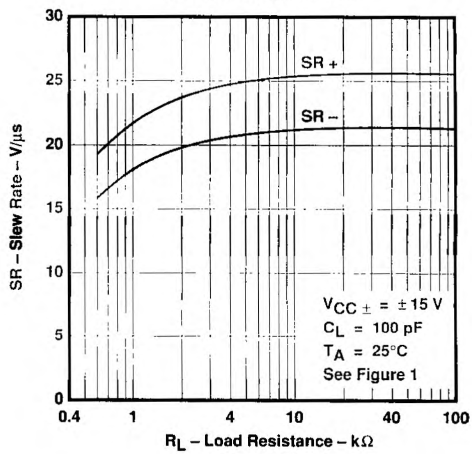

FIGURE 37

2

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

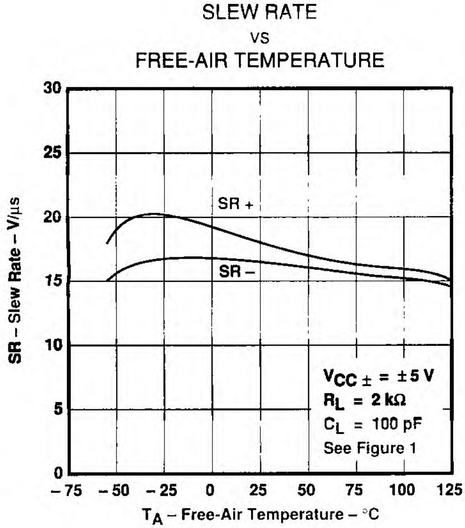

FIGURE 38

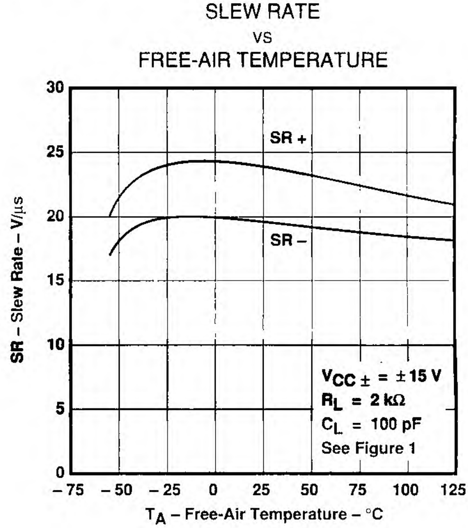

FIGURE 39

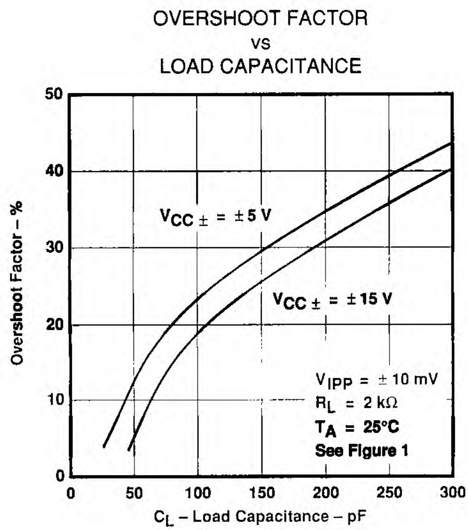

FIGURE 40

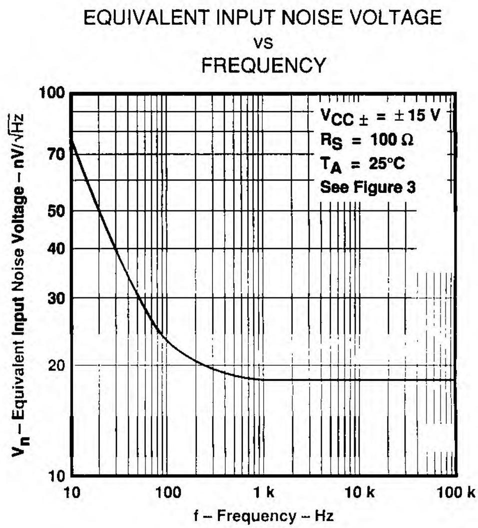

FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

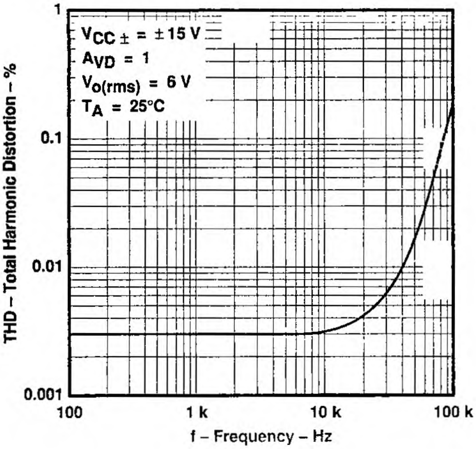


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

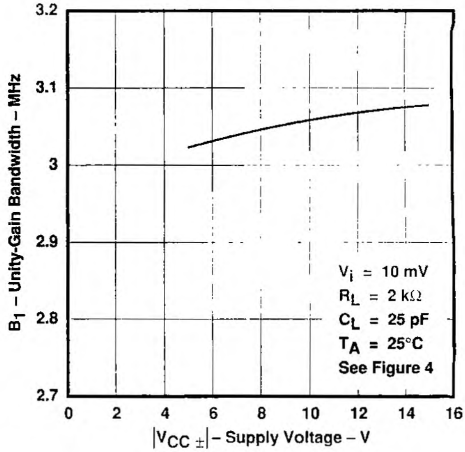


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

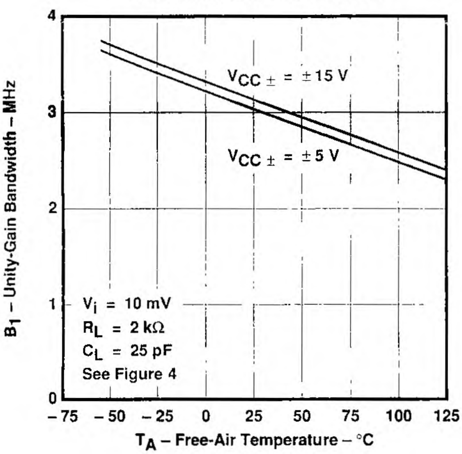


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

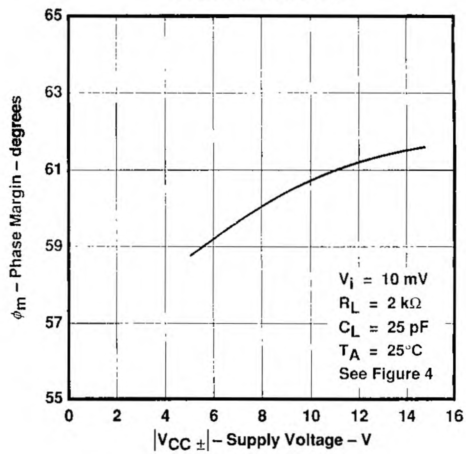


FIGURE 45

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

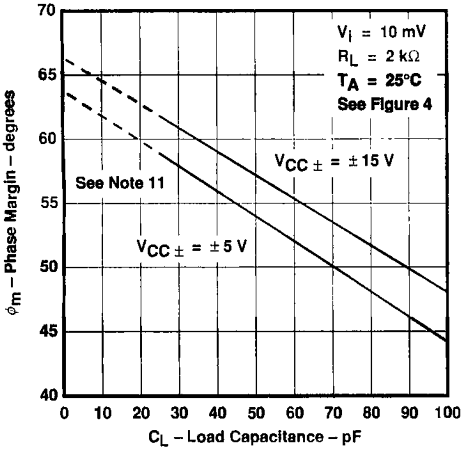


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

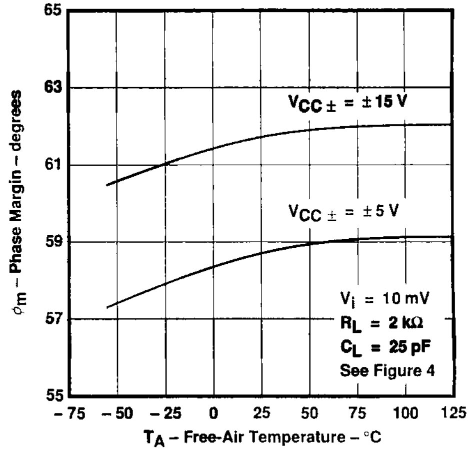


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

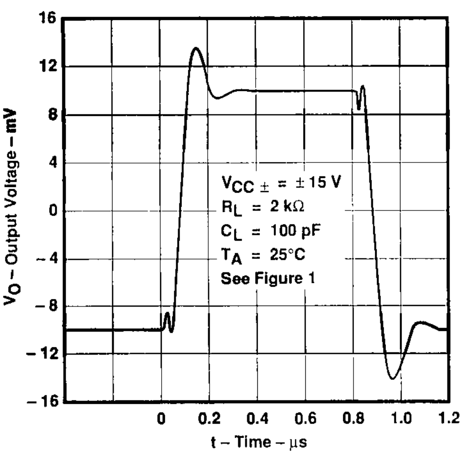


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

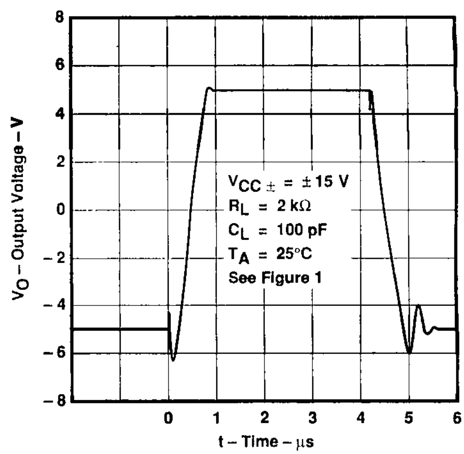


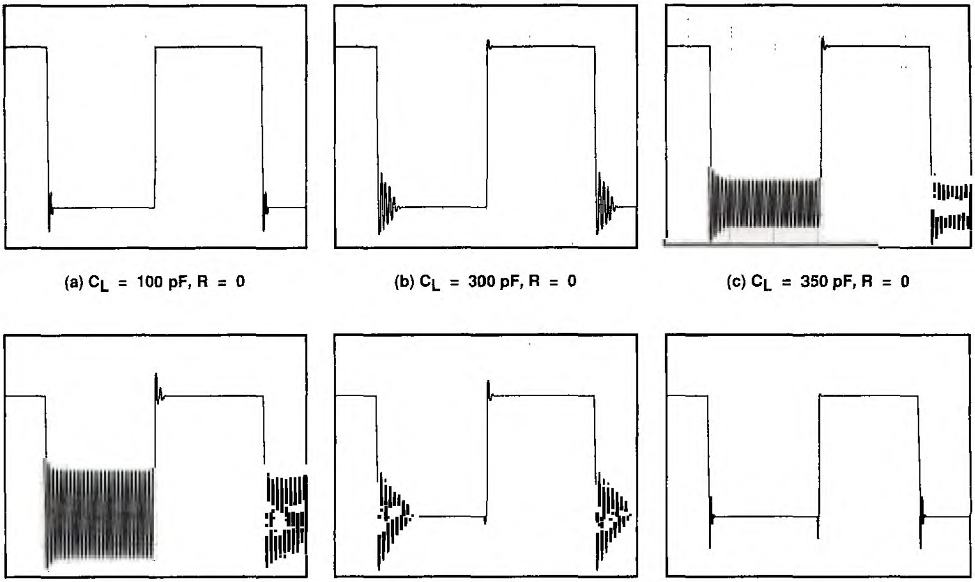
FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL APPLICATION DATA

output characteristics

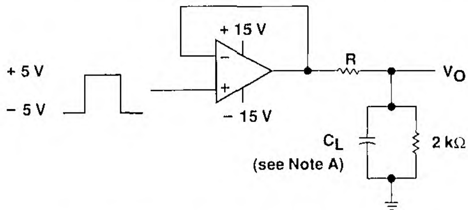
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL051 and TL051A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

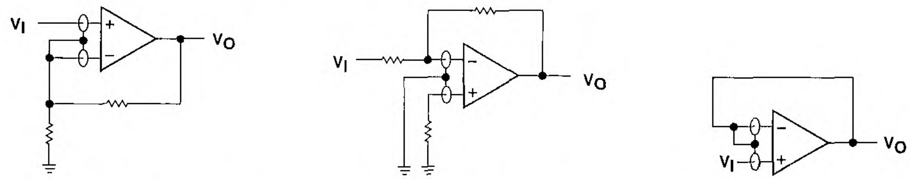
FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

The TL051 and TL051A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL051 and TL051A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL051 and TL051A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

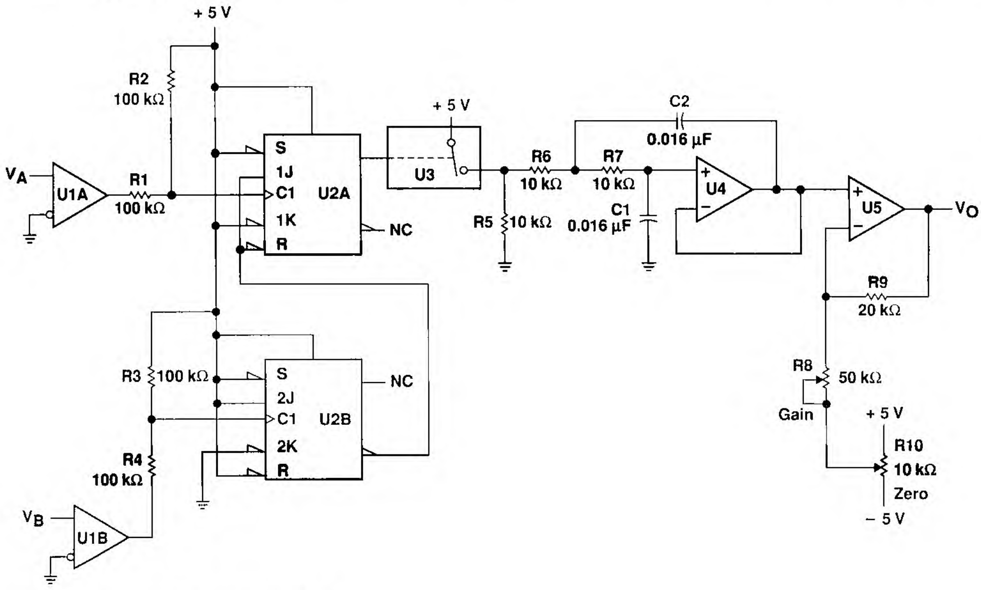
phase meter

The phase meter in Figure 53 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5-V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flop.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL051 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U2A approximates a square wave, and U4 has an output of almost 2.5 V. U5 acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4,U5 = TL051; $V_{CC\pm}$ = ±5 V.

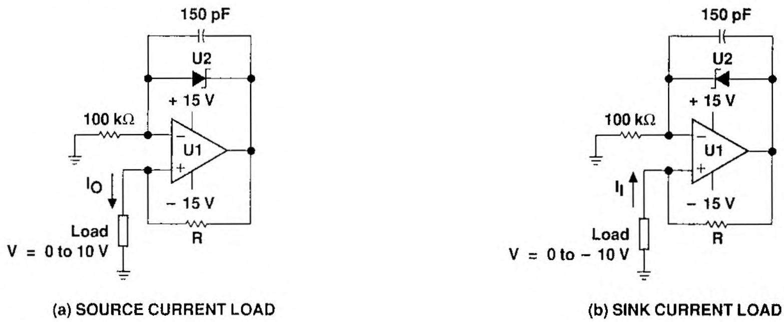
FIGURE 53. PHASE METER

TYPICAL APPLICATION DATA

precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL051. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



NOTES: U1 = TL051.
U2 = LM385, LT1004, or LT1009 voltage reference.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

FIGURE 54. PRECISION CONSTANT-CURRENT SOURCE

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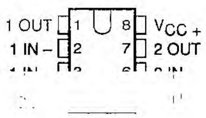
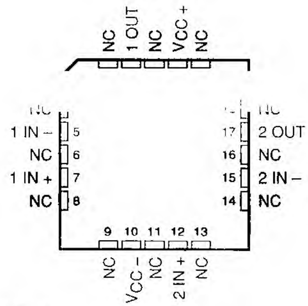
D3235, JUNE 1988 – REVISED FEBRUARY 1989

- **Maximum Offset Voltage . . . 800 μV (TL052A)**
- **High Slew Rate . . . 17.8 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE (TOP VIEW)

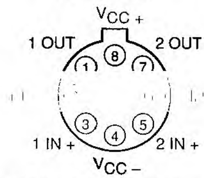


FK PACKAGE (TOP VIEW)



NC – No internal connection

L PACKAGE (TOP VIEW)



Pin 4 is in electrical contact with the case

description

The TL052 and TL052A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

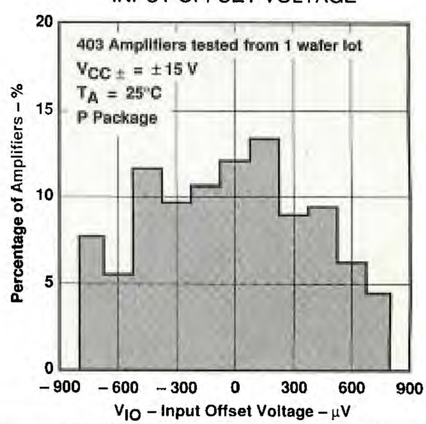
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL052 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL052 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 μV	T[illegible]	—	TL052ACJG	TL052ACL	TL052ACP
	1500 μV	T[illegible]	—	[illegible]	T[illegible]	T[illegible]
– 40°C to [illegible]	800 μV	T[illegible]	—	TL052AIJG	T[illegible]	T[illegible]
	1500 μV	T[illegible]	—	TL052IJG	T[illegible]	T[illegible]
[illegible] to 125°C	800 μV	T[illegible]MD	T[illegible]	TL052AMJG	T[illegible]	TL052AMP
	[illegible] μV	TL052MD	TL[illegible]	TL052MJG	TL052ML	TL052MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL052CDR).

DISTRIBUTION OF TL052A INPUT OFFSET VOLTAGE



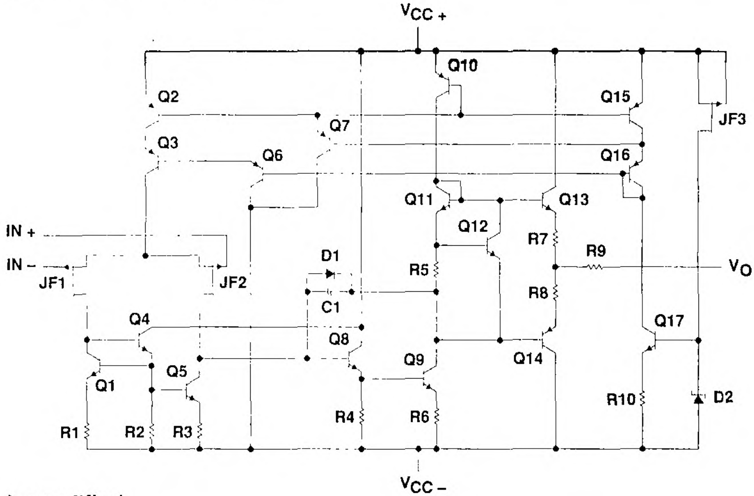
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL072 and TL082. Two offset voltage grades are available: TL052 (1.5 mV max) and TL052A (800 µV max).

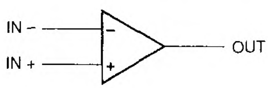
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	− 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	− 55°C to 125°C
I-suffix	− 40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	− 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1		4	− 1		4	− 1		4	V
	$V_{CC\pm} = \pm 15$ V	− 11		11	− 11		11	− 11		11	
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052M	25°C		0.73	3.5		0.65	1.5	mV
				Full range			6.5			4.5	
			TL052AM	25°C		0.51	2.8		0.4	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10			9		µV/°C
			TL052AM	25°C to 125°C		9			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5 6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				F[illegible]e	3			13			
		$R_L = 2\ k\Omega$			2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				−55°C		4.4	6.4		4.5	6.4	
				125°C		4.2	6.4		4.4	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7	25°C		17.8		[illegible]	20.7		V/μs
			– 55°C		18.8			20.3		
			125°C		14.5			20.2		
SR –	Negative slew rate at unity gain		25°C		15.4		13	17.8		
			– 55°C		15.7			17.6		
			125°C		13.8			16.5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		55			56		ns
			– 55°C		51			52		
			125°C		68			68		
t_f	Fall time		25°C		55			57		
			– 55°C		51			52		
			125°C		68			69		
	Overshoot factor		25°C		24%			19%		
			– 55°C		25%			19%		
			125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3; f = 10 Hz	25°C		71			71		nV/√Hz
		R_S = 100 Ω, See Figure 3; f = 1 kHz	25°C		19			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage	R_S = 100 Ω, See Figure 3; f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4	25°C		3			3		MHz
			– 55°C		3.6			3.7		
			125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4	25°C		60°			63°		
			– 55°C		57°			61°		
			125°C		60°			63°		

† Full range is – 55°C to 125°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
8. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

2 Operational Amplifiers

electrical characteristics

	PARAMETER	TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052I	25°C		0.73	3.5		0.65	1.5	mV
			TL052I	Full range			5.3			3.3	mV
			TL052AI	25°C		0.51	2.8		0.4	0.8	mV
			TL052AI	Full range			4.6			2.6	mV
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052I	25°C to 85°C		7			6		μV/°C
			TL052AI	25°C to 85°C		6			6	25	μV/°C
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	[illegible]		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			V
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		V
				Full range	2.5			11.5			V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			V
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		V
				Full range	−2.3			−11			V
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		V/mV
				85°C	20	43		30	76		V/mV
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		dB
				85°C	65	84		75	93		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		dB
				85°C	75	99		75	99		dB
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				−40°C		4.5	6.4		4.7	6.4	mA
				85°C		4.4	6.4		4.6	6.4	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

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operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/µs
				– 40°C		18.8		11	20.6		
				85°C		16		11	20.7		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 40°C		16		11	17.8		
				85°C		14.5		11	17.2		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			[illegible]		
				– 40°C		24%			[illegible]		
				85°C		24%			[illegible]		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				– 40°C		3.5			3.6		
				85°C		2.5			2.6		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				– 40°C		58°			61°		
				85°C		60°			63°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
8. For $V_{CC\pm} = \pm5$ V, $V_{o(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{o(rms)} = 6$ V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052C	25°C		0.73	3.5		0.65	1.5	mV
				Full range			4.5			2.5	
			TL052AC	25°C		0.51	2.8		0.4	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052C	25°C to 70°C		8			8		µV/°C
			TL052AC	25°C to 70°C		8			6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20			30		pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	[illegible]ce			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				0°C		4.7	6.4		4.8	6.4	
				70°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

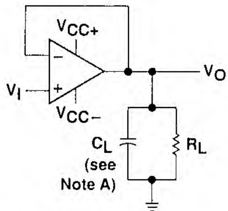
operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/µs
				0°C		18.5		11	20.9		
				70°C		16.5		11	20.8		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				0°C		15.7		11	18.5		
				70°C		14.7		11	16.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			[illegible]		
				0°C		24%			[illegible]		
				70°C		24%			[illegible]		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			[illegible]		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				0°C		3.2			3.2		
				70°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				0°C		59°			63°		
				70°C		60°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
8. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

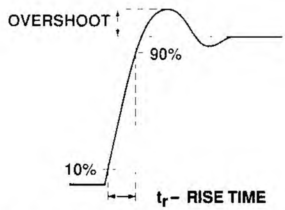


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

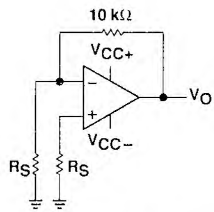
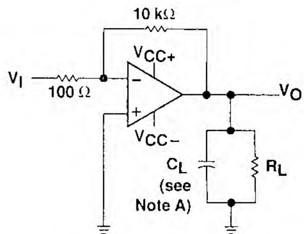


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

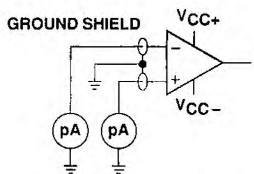


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

At the picoamp-bias-current level typical of the TL052 and TL052A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE

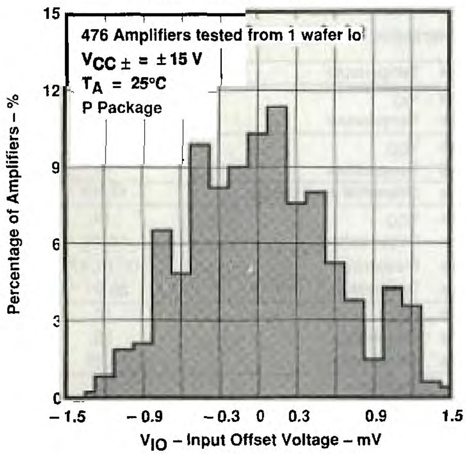


FIGURE 6

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

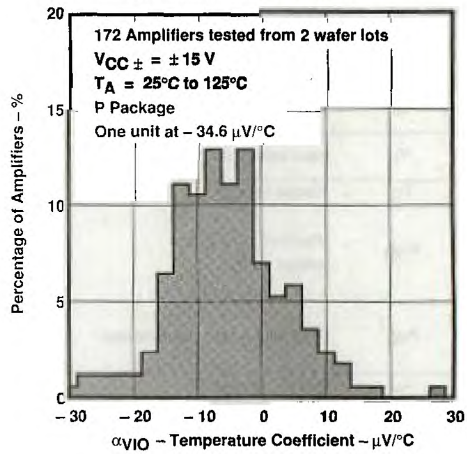


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

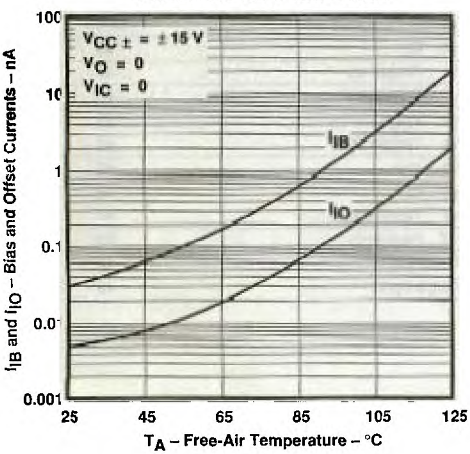


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

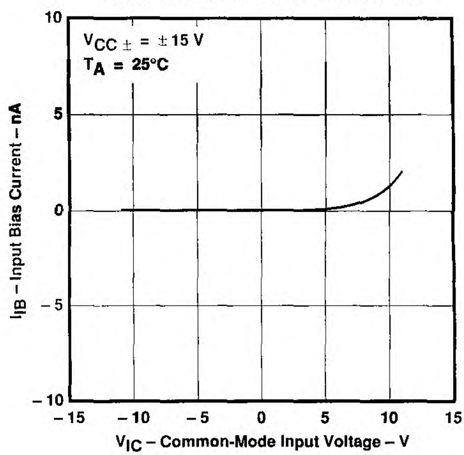


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

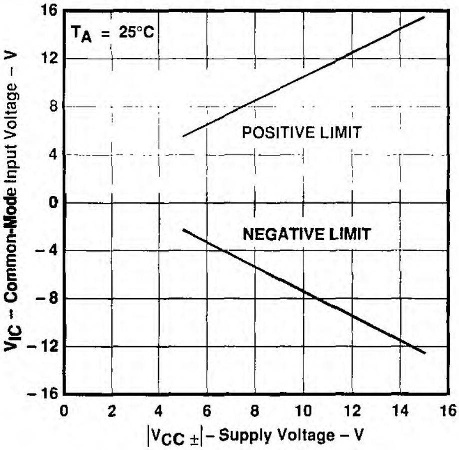


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

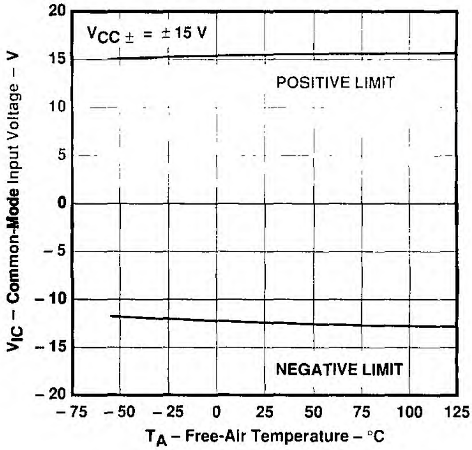


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

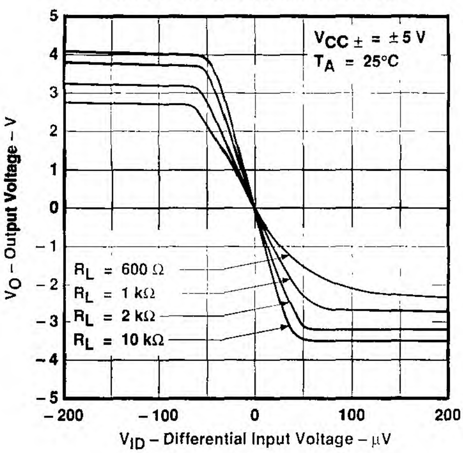


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

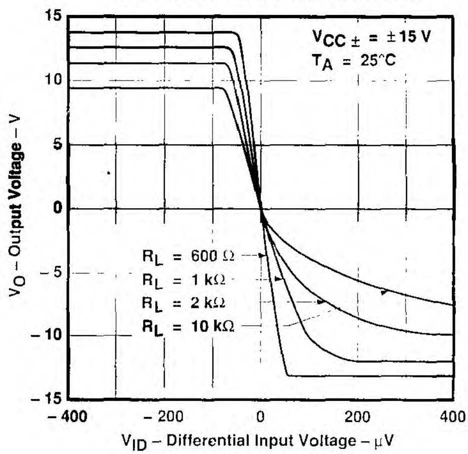


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

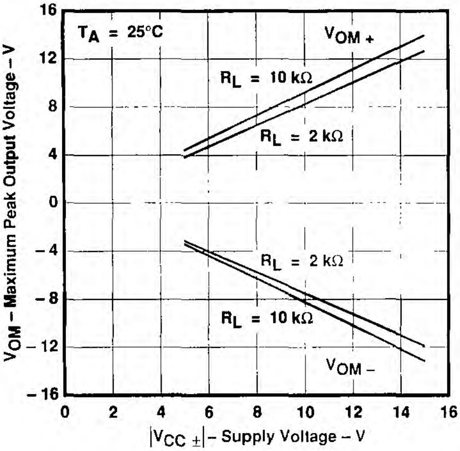


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

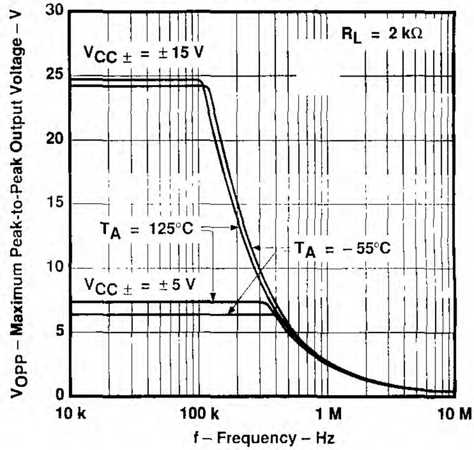


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

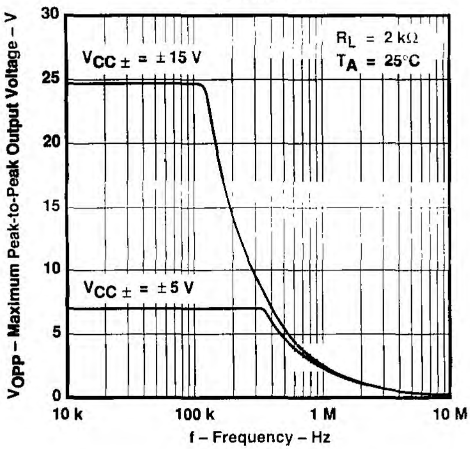


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

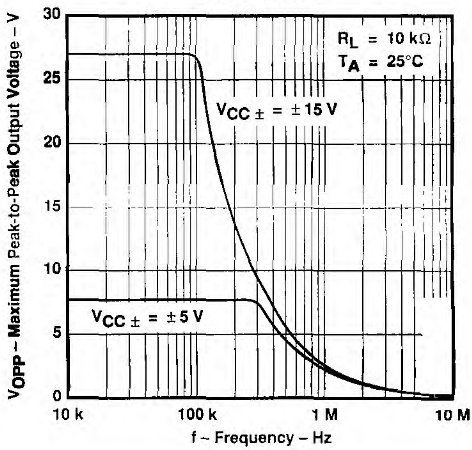


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

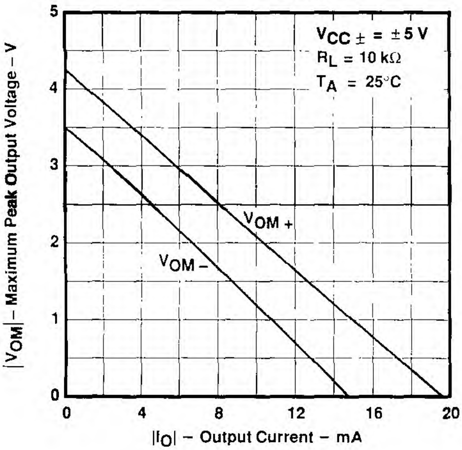

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

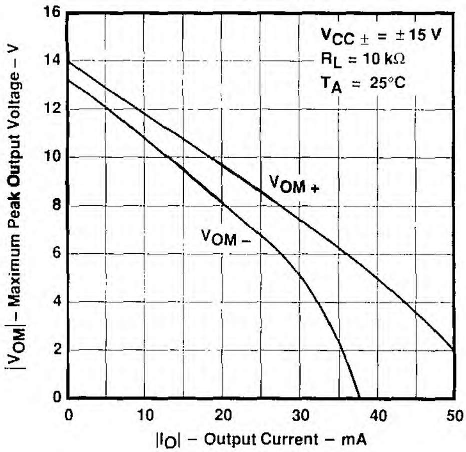

FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

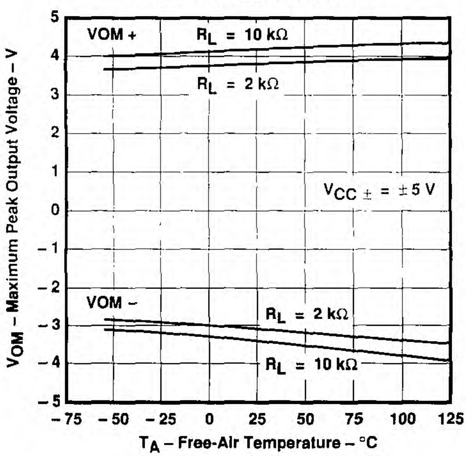

FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

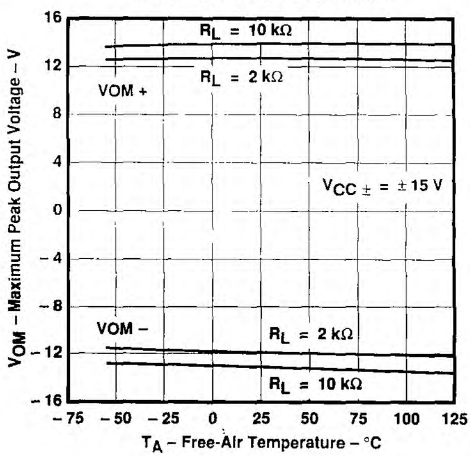

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

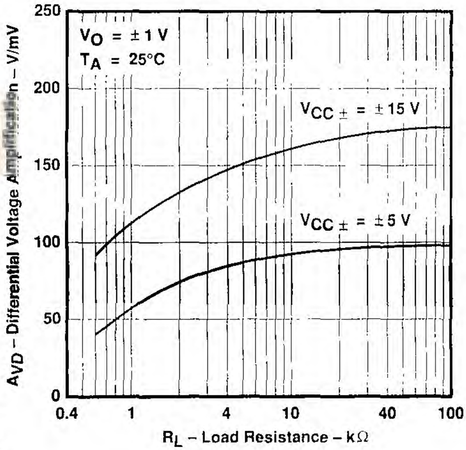

FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

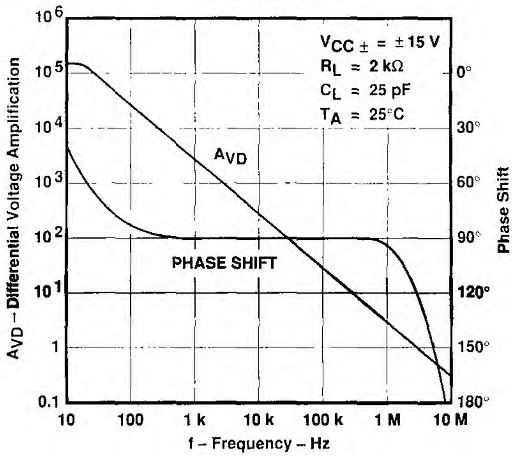

FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

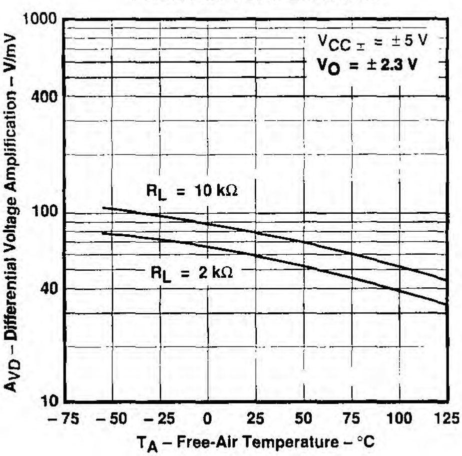

FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

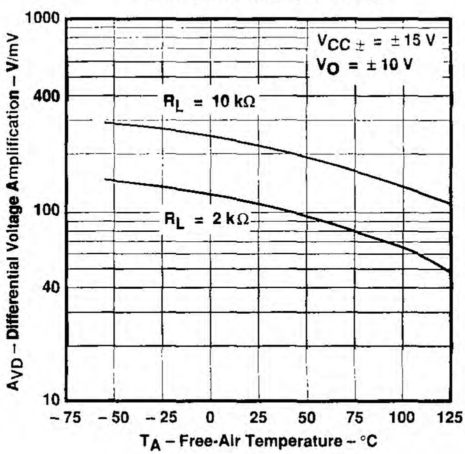

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

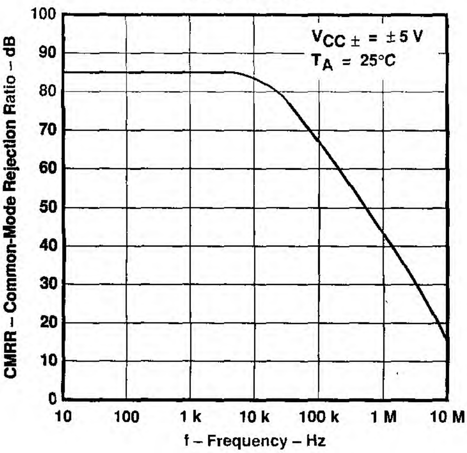

FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

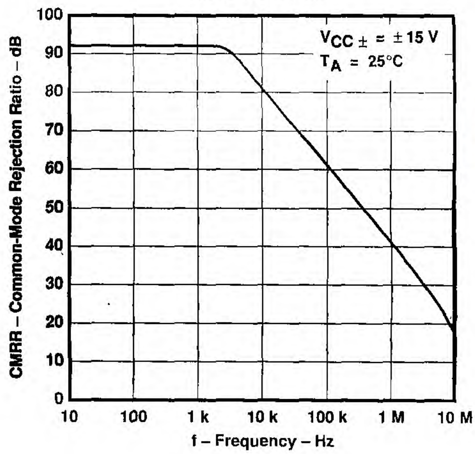

FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

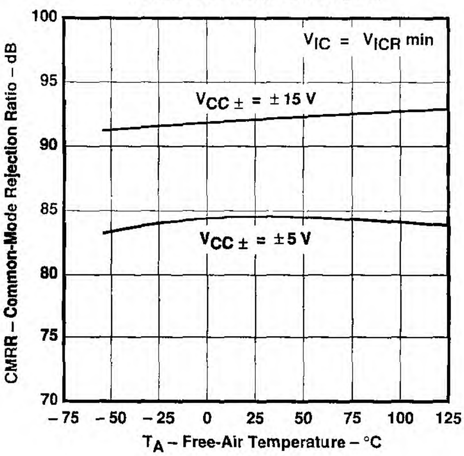

FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

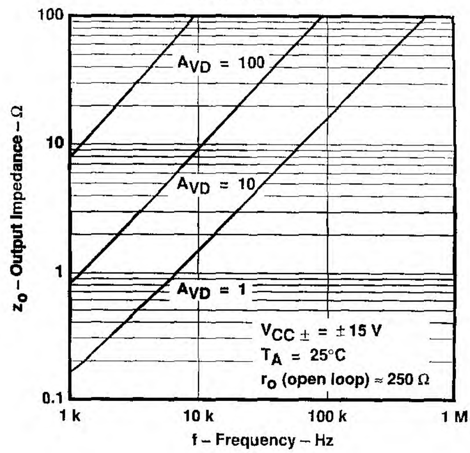

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

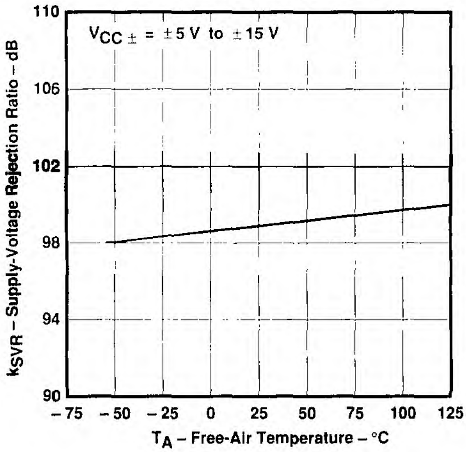

FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

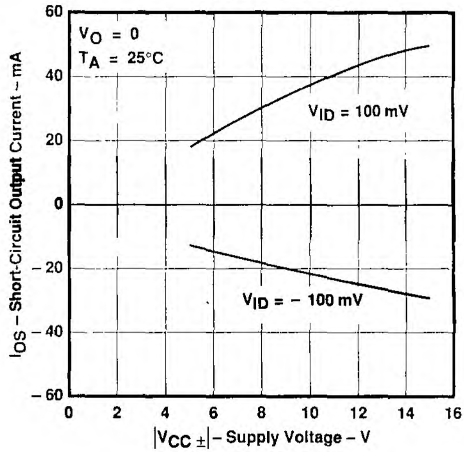

FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

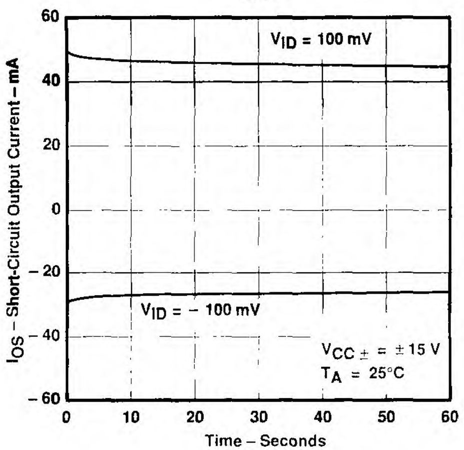

FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

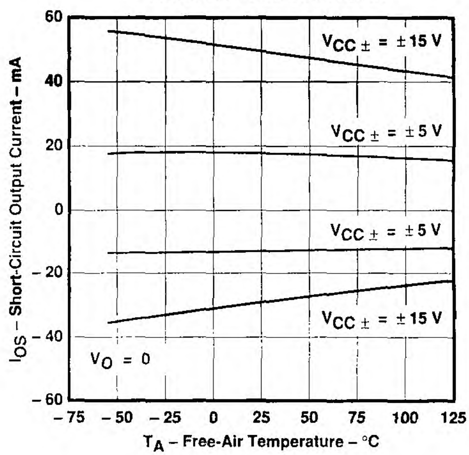

FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

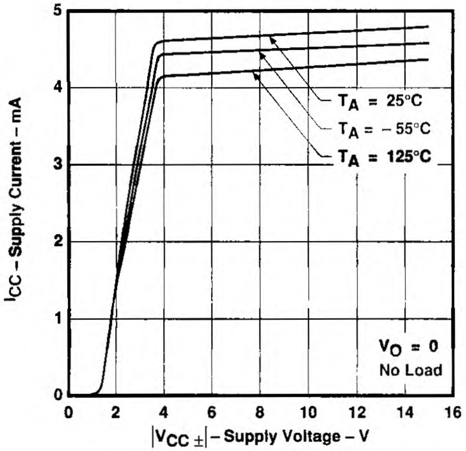

FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

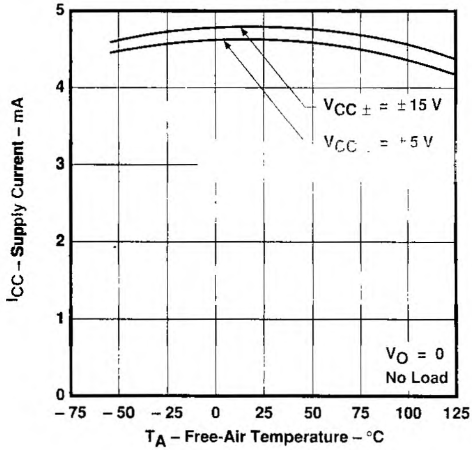

FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

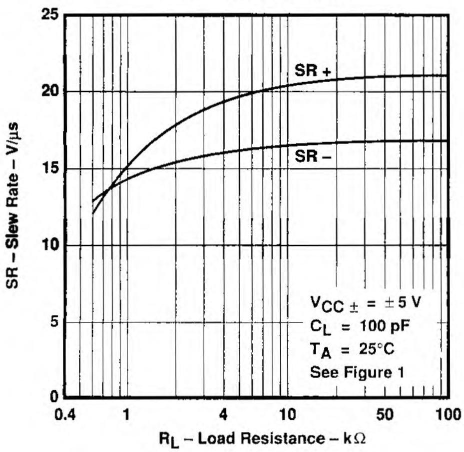

FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

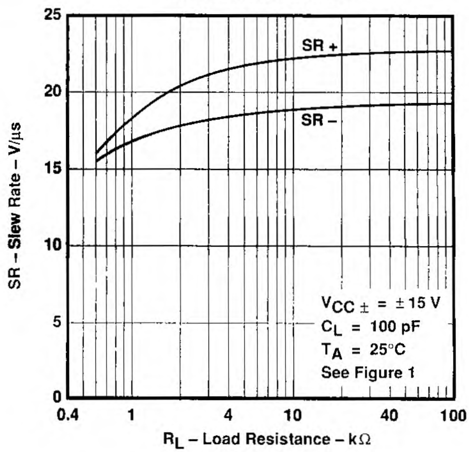

FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

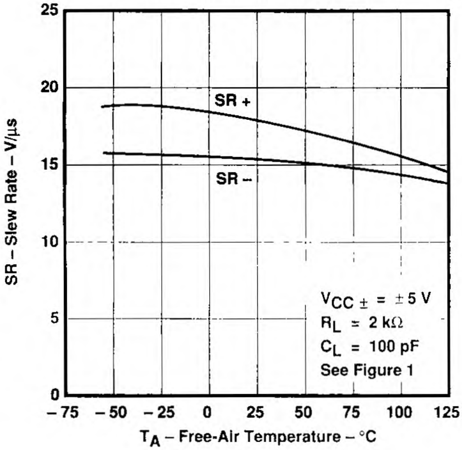

FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

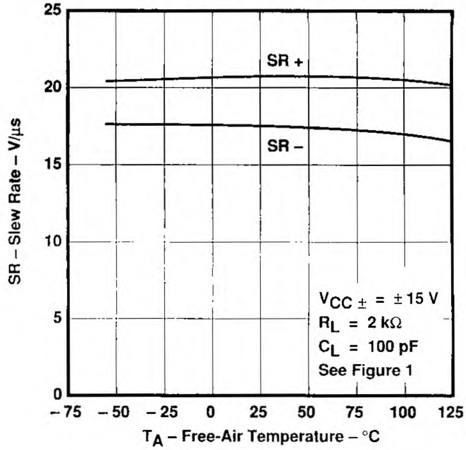

FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

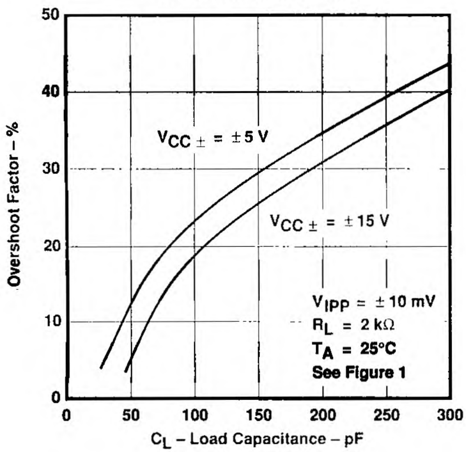

FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

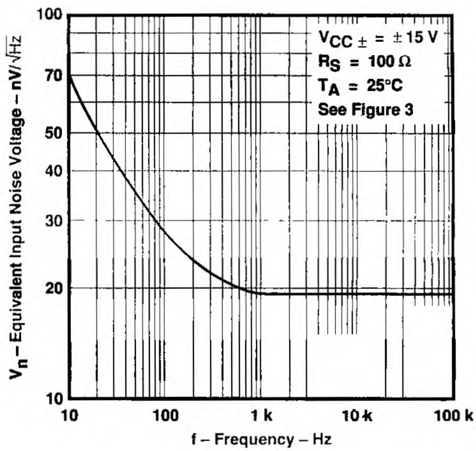

FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

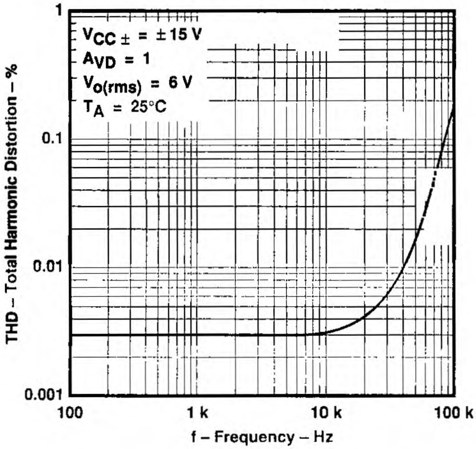

FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

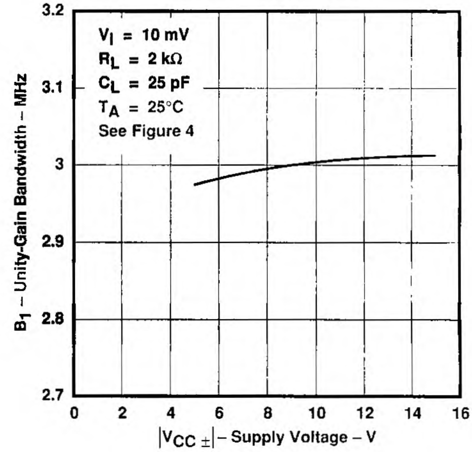

FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

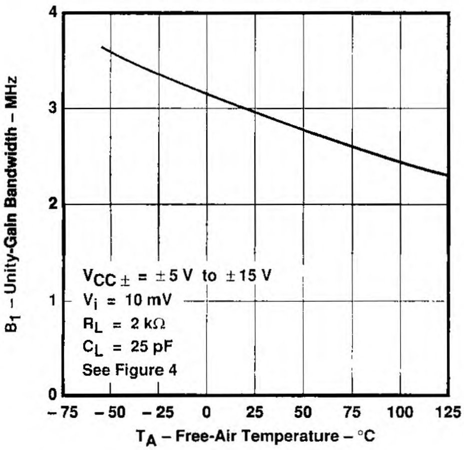

FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

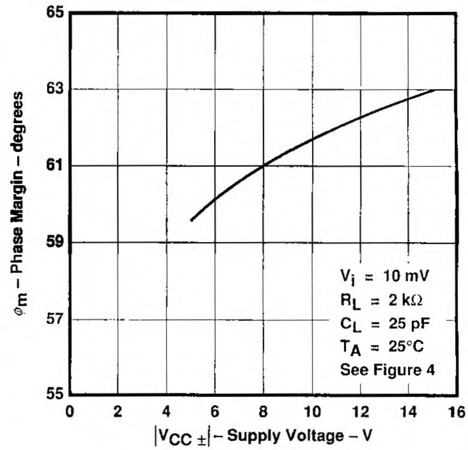

FIGURE 45

2 Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

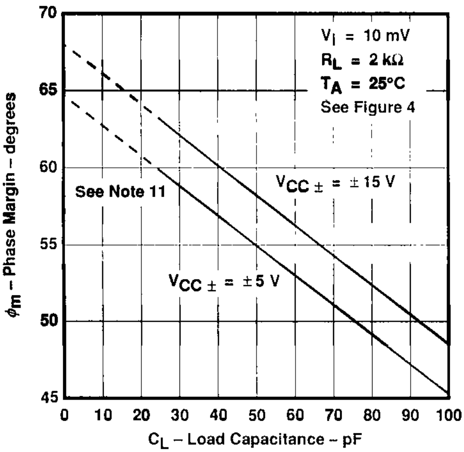

FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

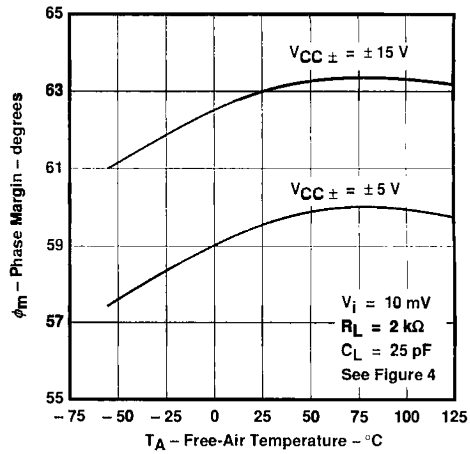

FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

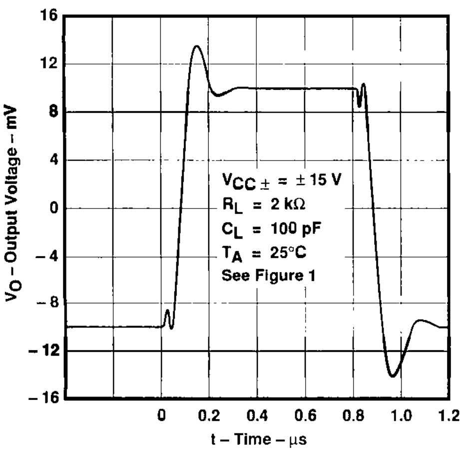

FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

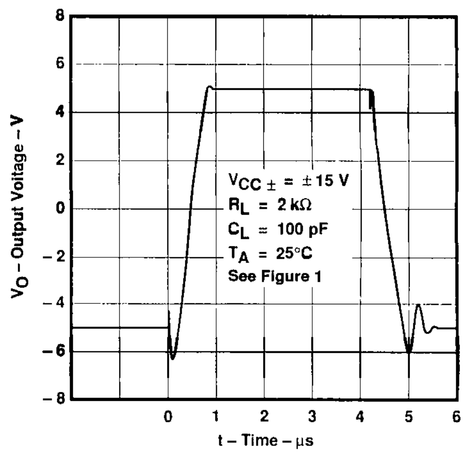

FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

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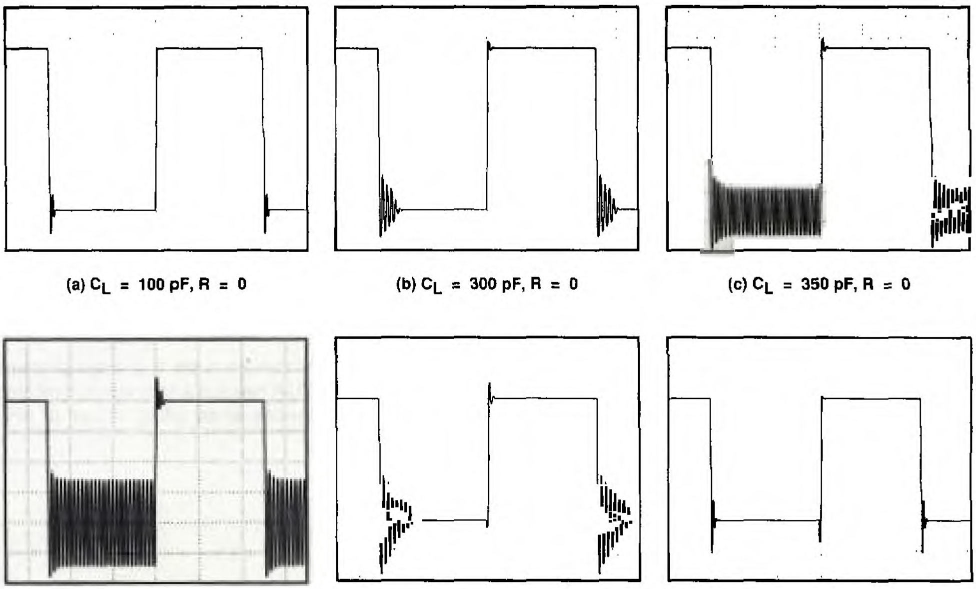
TYPICAL APPLICATION DATA

output characteristics

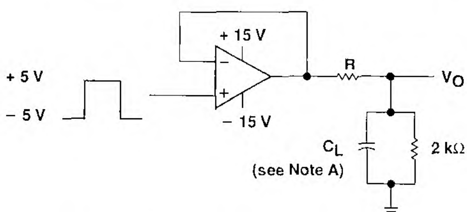
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL052 and TL052A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

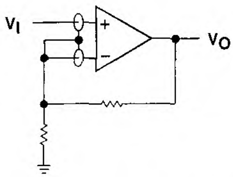
TYPICAL APPLICATION DATA

input characteristics

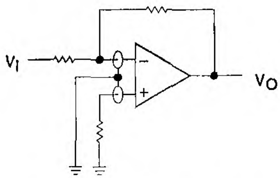
The TL052 and TL052A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL052 and TL052A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

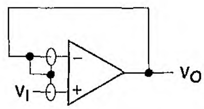
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER



(b) INVERTING AMPLIFIER



(c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL052 and TL052A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL052A. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

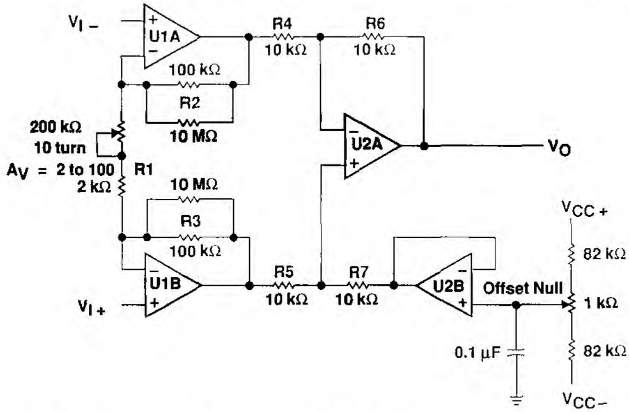
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL052A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE. U1A through U2B = TL052A, $V_{CC\pm} = \pm 15$ V.

FIGURE 53. INSTRUMENTATION AMPLIFIER

2

Operational Amplifiers

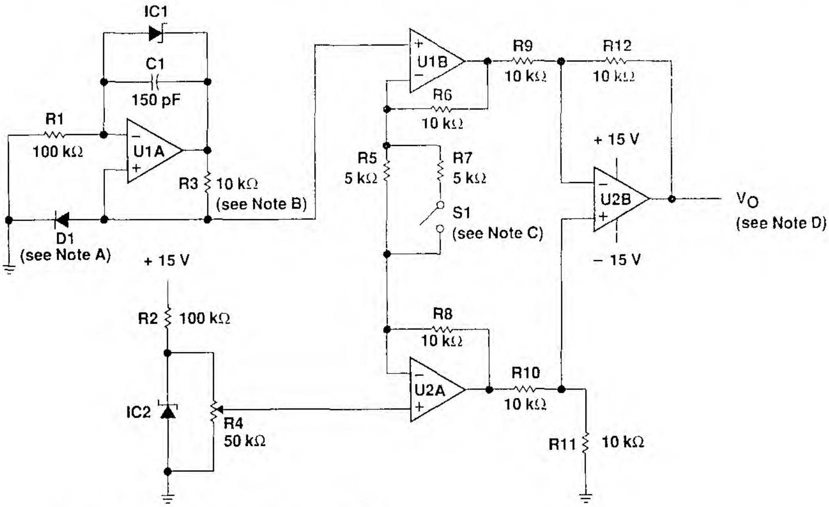
TYPICAL APPLICATION DATA

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 54). Amplifier U1A and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL052 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature sensing diode ≈ (– 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A through U2B = TL052. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 54. ANALOG THERMOMETER

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

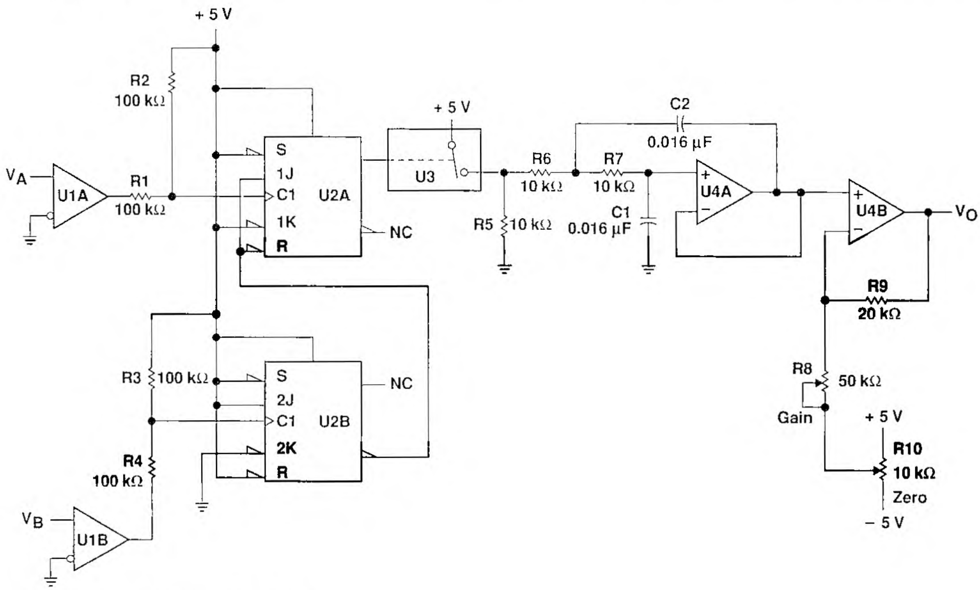
phase meter

The phase meter in Figure 55 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5 V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL052 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave, and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0-to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4 = TL052, $V_{CC\pm}$ = ±5 V.

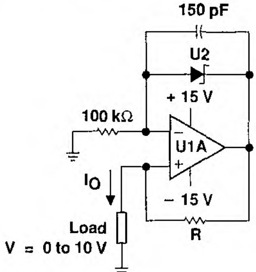
FIGURE 55. PHASE METER

TYPICAL APPLICATION DATA

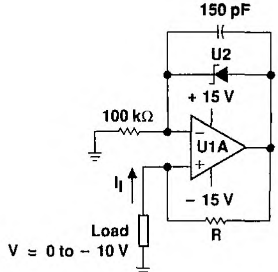
precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL052. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) SOURCE CURRENT LOAD



(b) SINK CURRENT LOAD

NOTES: IC1 = LM385, LT1004, or LT1009 voltage reference.
U1A = TL052.
$I \approx \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

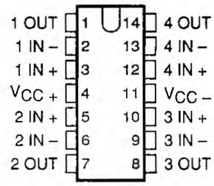
FIGURE 56. PRECISION CONSTANT-CURRENT SOURCE

TL054, TL054A ENHANCED JFET PRECISION QUAD OPERATIONAL AMPLIFIERS

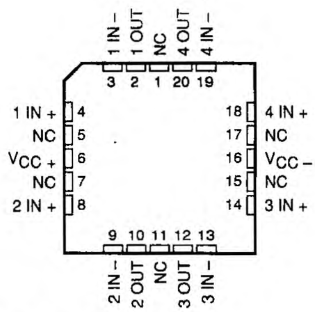
D3236, JUNE 1988 – REVISED JANUARY 1989

- **Maximum Offset Voltage . . . 1.5 mV (TL054A)**
- **High Slew Rate . . . 15.9 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 21 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**
- **Monolithic Construction**

D, J, or N PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)



NC – No internal connection

description

The TL054 and TL054A quad operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL054 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL054 has been designed to be functionally compatible, as well as pin compatible, with the TL074 and TL084.

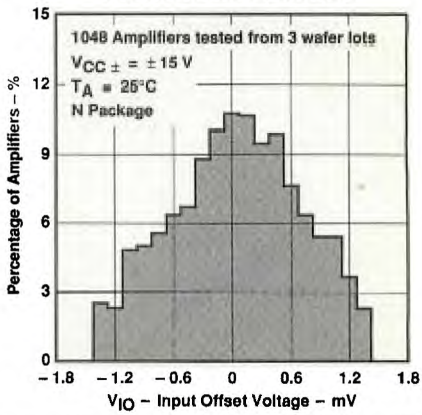
Two offset voltage grades are available: TL054 (4 mV max) and TL054A (1.5 mV max).

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	[illegible]	—	TL054ACJ	[illegible]
	4 mV	[illegible]	—	TL054CJ	[illegible]
– 40°C to 85°C	1.5 mV	[illegible]	—	TL054AIJ	TL054AIN
	4 mV	[illegible]	—	[illegible]	[illegible]
– 55°C to 125°C	1.5 mV	[illegible]	[illegible]	[illegible]	[illegible]
	4 mV	[illegible]	[illegible]	[illegible]	[illegible]

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL054CDR).

DISTRIBUTION OF TL054A INPUT OFFSET VOLTAGE

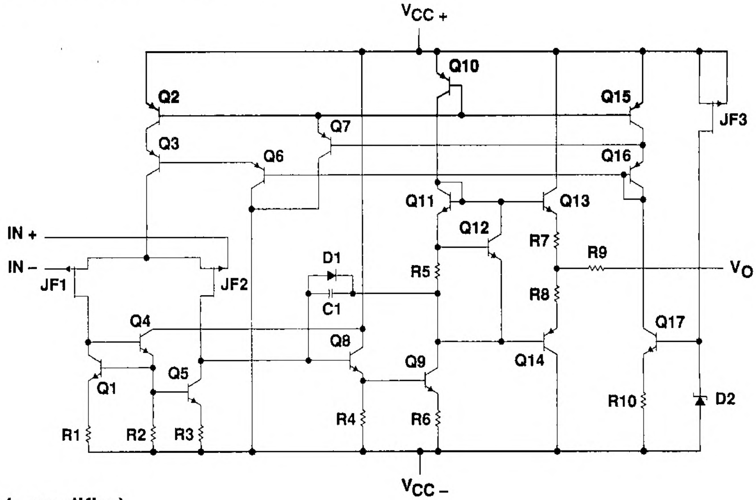


description (continued)

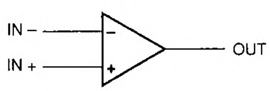
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) .... 18 V
Supply voltage, V_{CC-} (see Note 1) .... − 18 V
Differential input voltage (see Note 2) .... ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) .... ± 15 V
Input current, I_I (each input) .... ± 1 mA
Output current, I_O (each output) .... ± 80 mA
Total current into V_{CC+} terminal .... 160 mA
Total current out of V_{CC-} terminal .... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... − 55°C to 125°C
I-suffix .... − 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... − 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE TA = 25°C	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	230 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1		4	− 1		4	− 1		4	V
	$V_{CC\pm} = \pm 15$ V	− 11		11	− 11		11	− 11		11	
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054M	25°C		0.64	5.5		0.56	4	mV
				Full range			10.5			9	
			TL054AM	25°C		0.57	3.5		0.5	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL054M	25°C to 125°C		21			20		µV/°C
			TL054AM	25°C to 125°C		21			20		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	[illegible]		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				−55°C	30	99		60	209		
				125°C	10	35		15	[illegible]		
r_i	Input resistance			25°C		10^{12}			[illegible]		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−55°C		7.8	12.8		8.1	12.8	
				125°C		7.1	11.2		7.5	11.2	
V_{O1}/V_{O2}	C[illegible]	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				– 55°C		16.7			18.3		
				125°C		12.9			16.7		
SR –	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				– 55°C		14.7			16.3		
				125°C		12.2			14.5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				– 55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				– 55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				– 55°C		3.4			3.4		
				125°C		2.1			2.1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				– 55°C		58°			62°		
				125°C		60°			64°		

† Full range is – 55°C to 125°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, $V_{o(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{o(rms)} = 6$ V.

electrical characteristics

	PARAMETER	TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054I	25°C		0.64	[illegible]		0.56	4	mV
				Full range			8.8			7.3	
			TL054AI	25°C		0.57	3.5		0.5	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL054I	25°C to 85°C		25			24		µV/°C
			TL054AI	25°C to 85°C		25			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				−40°C	30	101		60	212		
				85°C	20	50		30	70		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−40°C	65	83		75	92		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	99		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−40°C		7.9	12.8		8.2	12.8	
				85°C		7.6	11.2		7.9	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				– 40°C		16.4		8	18		
				85°C		14		8	17.3		
SR –	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				– 40°C		14.7		8	16.1		
				85°C		13		8	[illegible]		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		[illegible]			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		[illegible]			[illegible]		
				– 40°C		[illegible]			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				– 40°C		3.3			3.3		
				85°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				– 40°C		59°			62°		
				85°C		61°			64°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

	PARAMETER	TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054C	25°C		0.64	5.5		0.56	4	mV
				Full range			7.7			6.2	
			TL054AC	25°C		0.57	3.5		0.5	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage		TL054C	25°C to 70°C		25			23		µV/°C
			TL054AC	25°C to 70°C		24			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				0°C	30	88		60	173		
				70°C	20	57		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	99		75	99		
				70°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				0°C		8.2	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

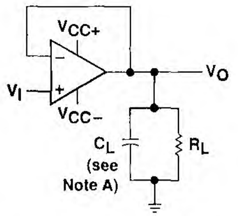
PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/µs
				0°C		15.7		8	17.9		
				70°C		14.4		8	17.5		
SR –	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				0°C		14.3		8	16.1		
				70°C		13.3		8	[illegible]		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			[illegible]		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise vc[illegible] (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	P[illegible] peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				0°C		3			3		
				70°C		2.4			2.4		
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				0°C		60°			64°		
				70°C		61°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
8. For $V_{CC\pm} = \pm 5$ V, [illegible] = 1 V; for $V_{CC\pm} = \pm 15$ V, [illegible] = 6 V.
9. This parameter is test[illegible] sample basis. For other test re[illegible]ts, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

2 Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

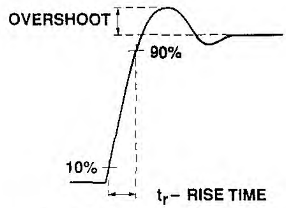


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

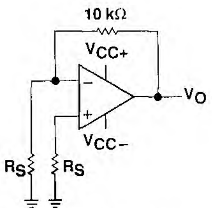
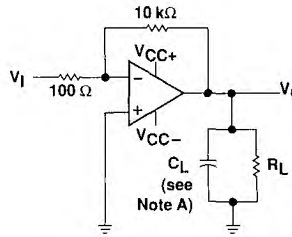


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

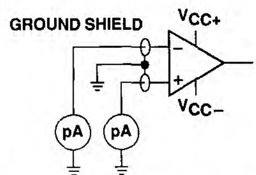


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

At the picoamp-bias-current level typical of the TL054 and TL054A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE

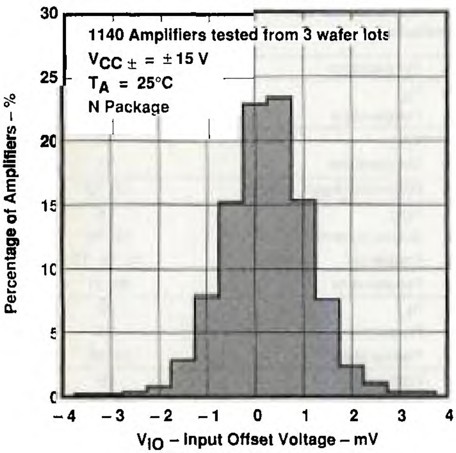


FIGURE 6

DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

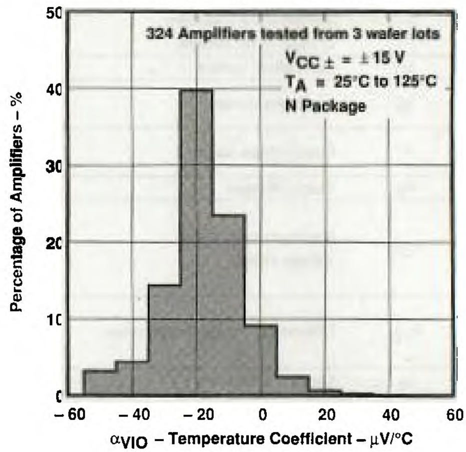


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

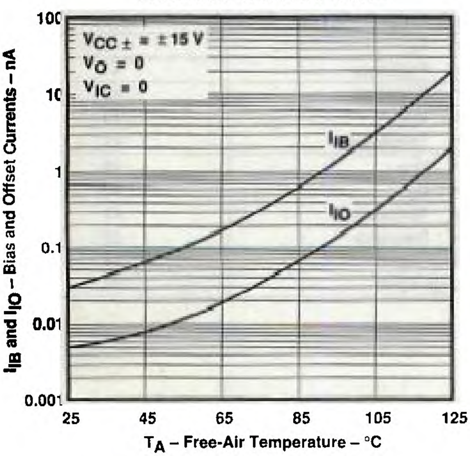


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

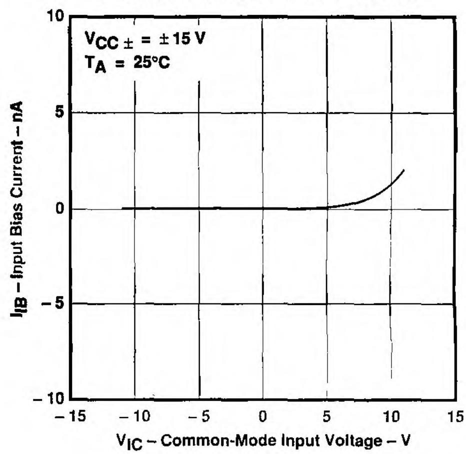


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

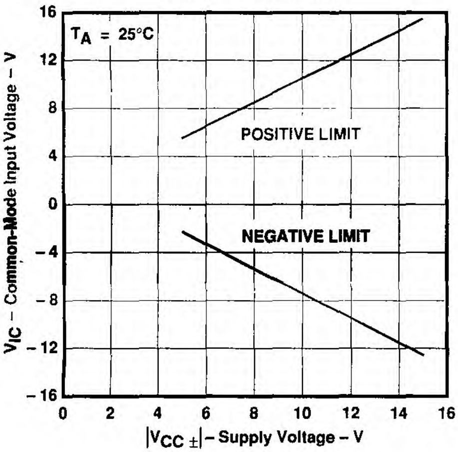


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

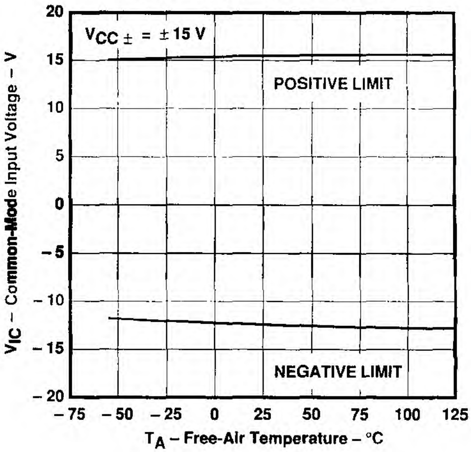


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

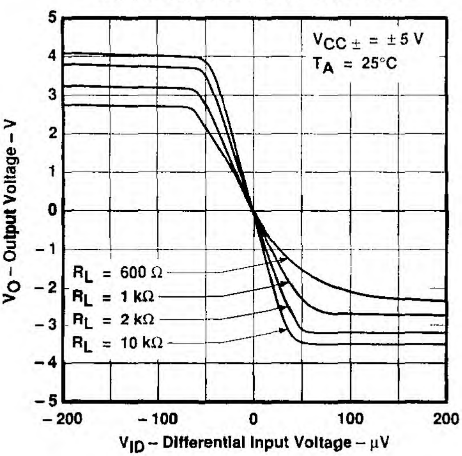


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

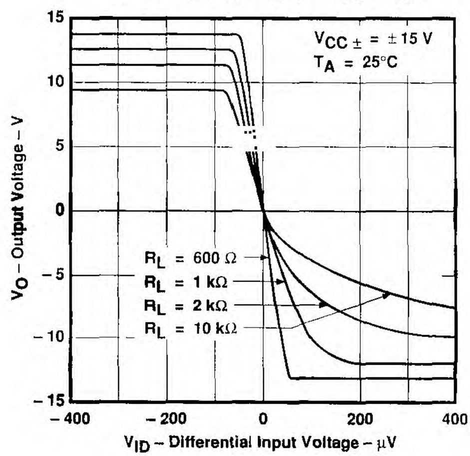


FIGURE 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

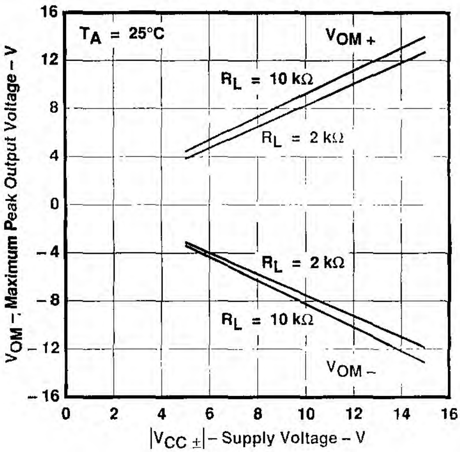


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

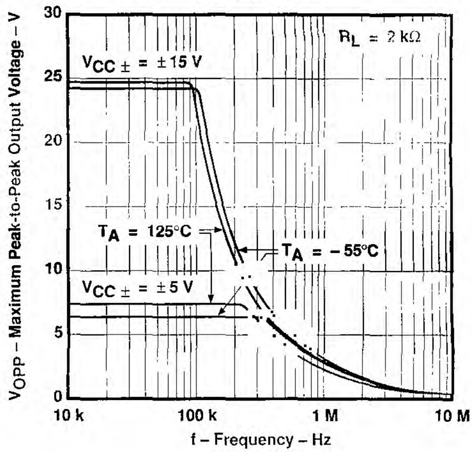


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

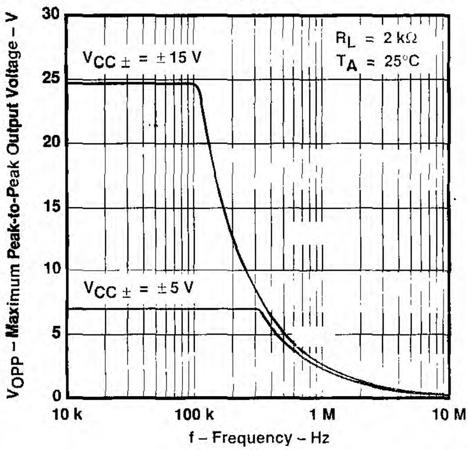


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

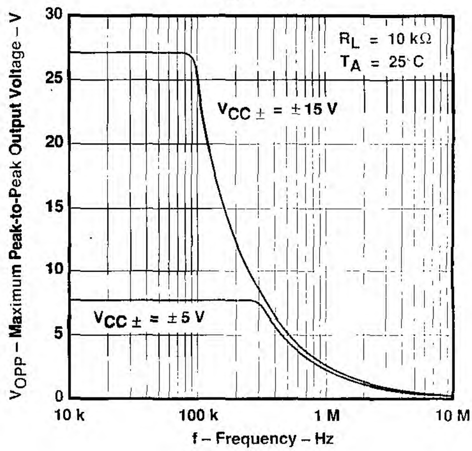


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

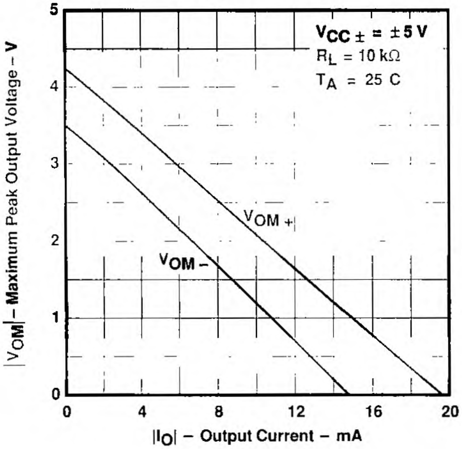

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

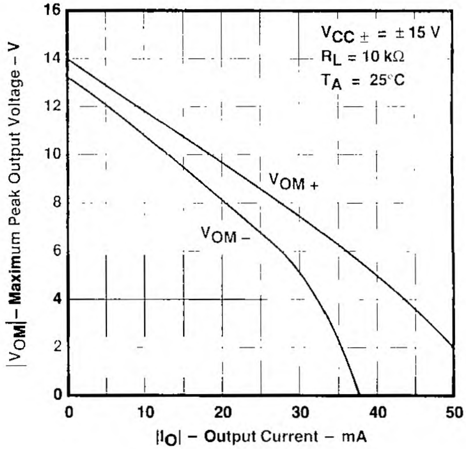

FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

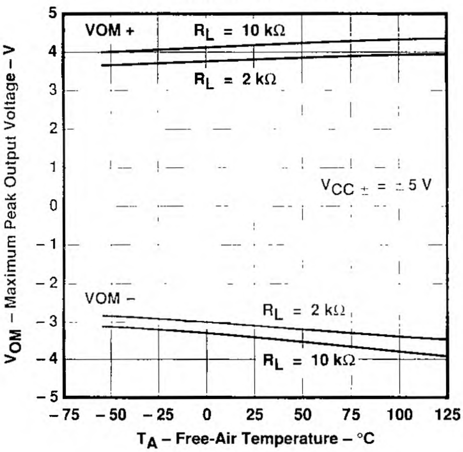

FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

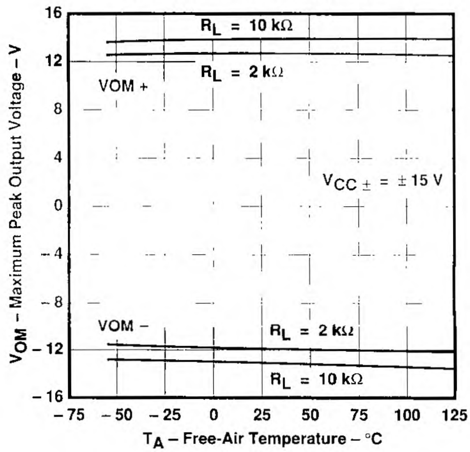

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

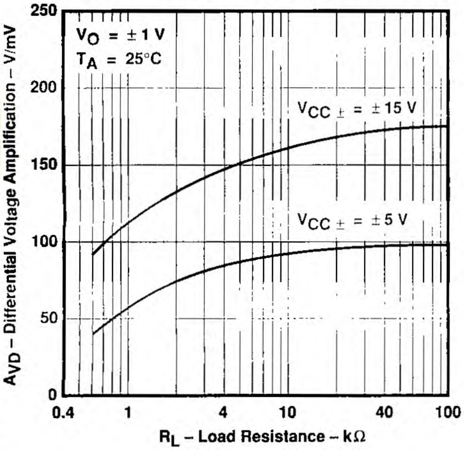

FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

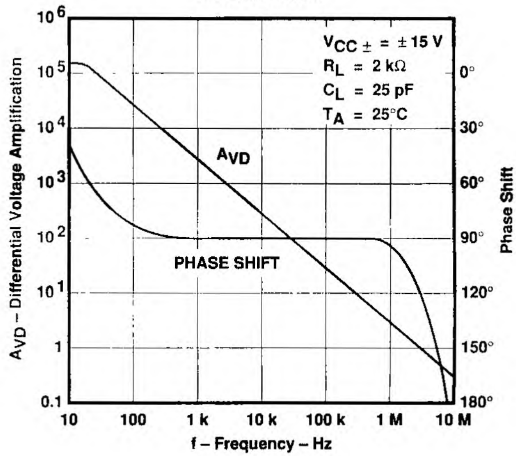

FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

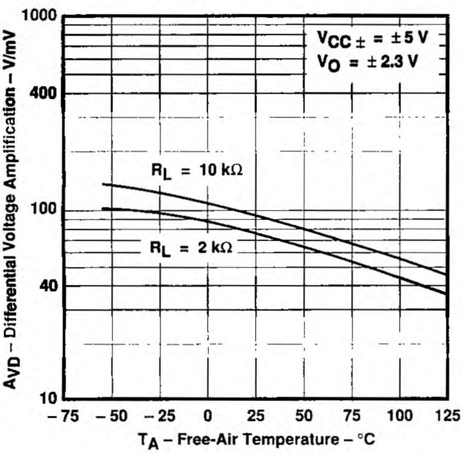

FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

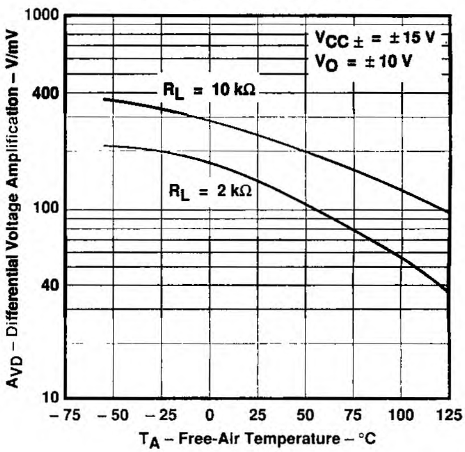

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

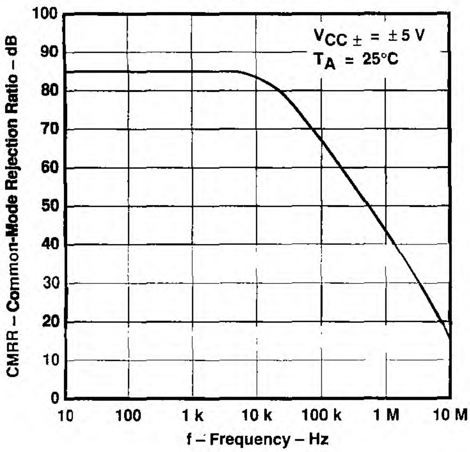


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

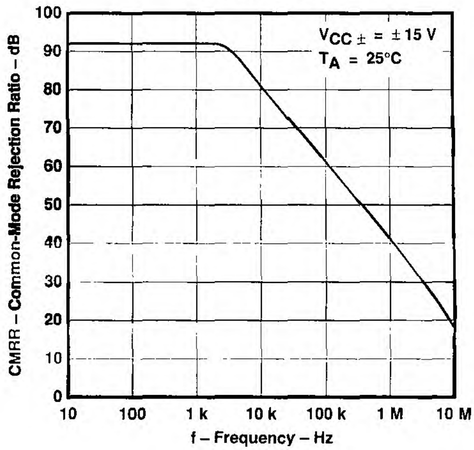


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

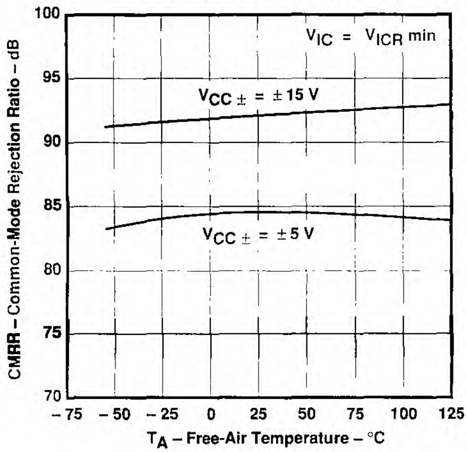


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

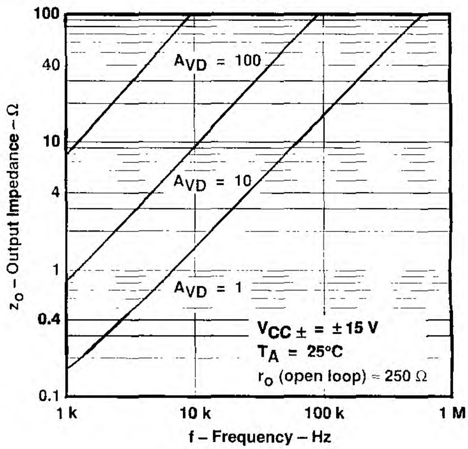


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

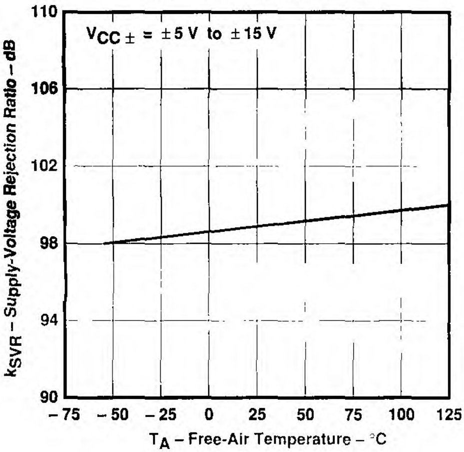


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

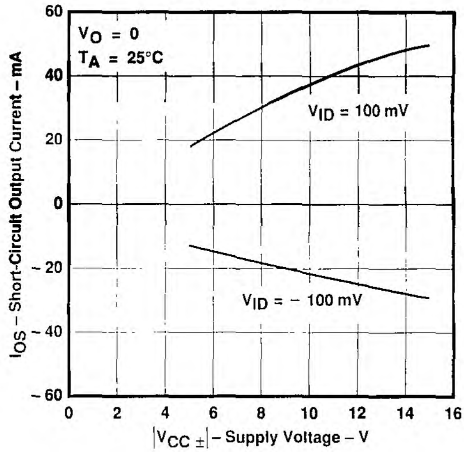


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

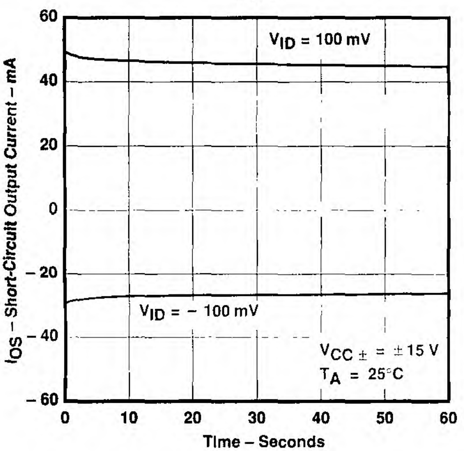


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

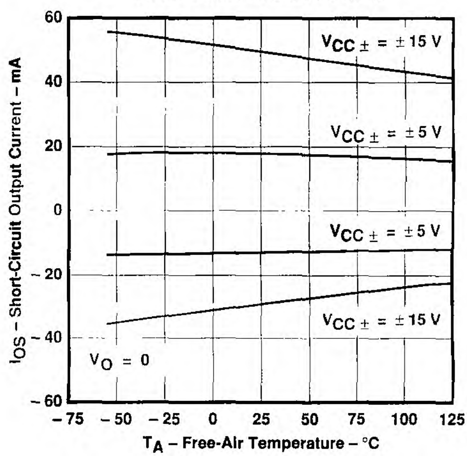


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

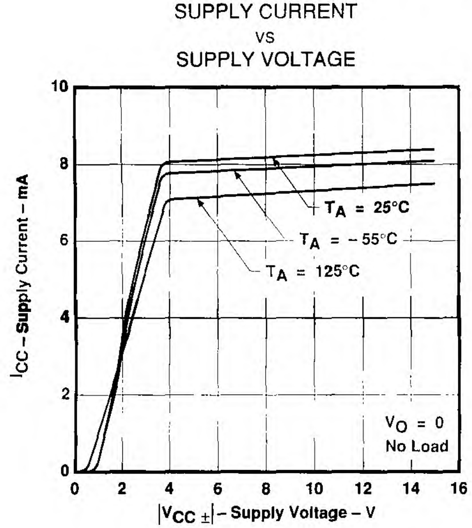


FIGURE 34

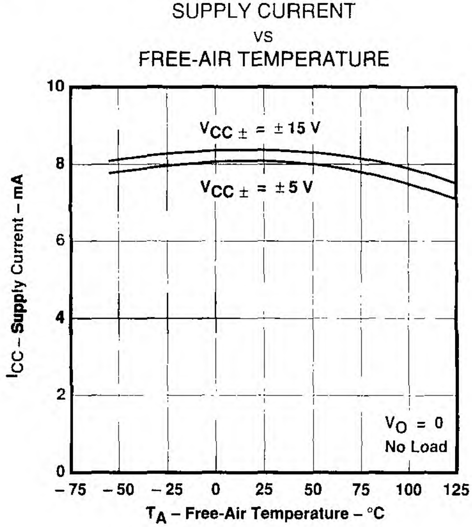


FIGURE 35

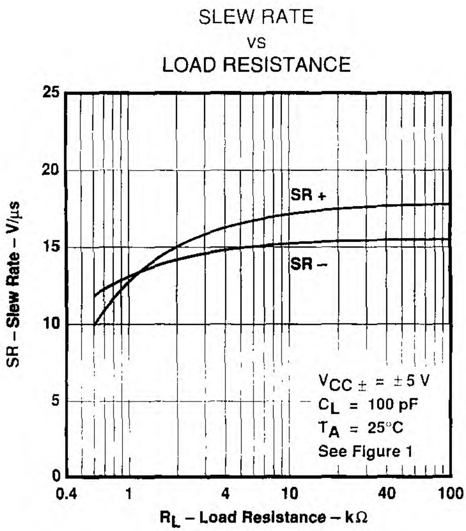


FIGURE 36

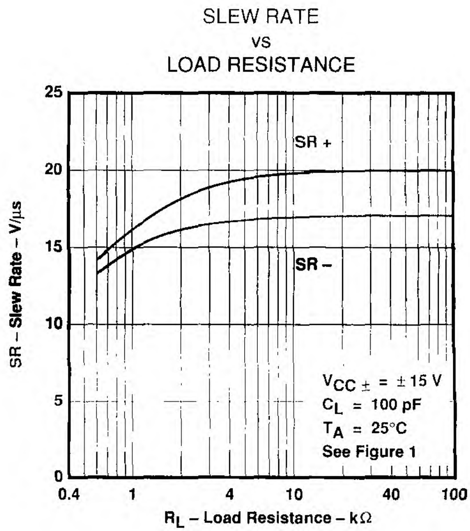


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

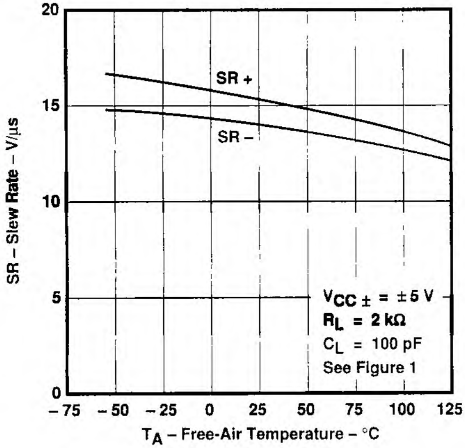


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

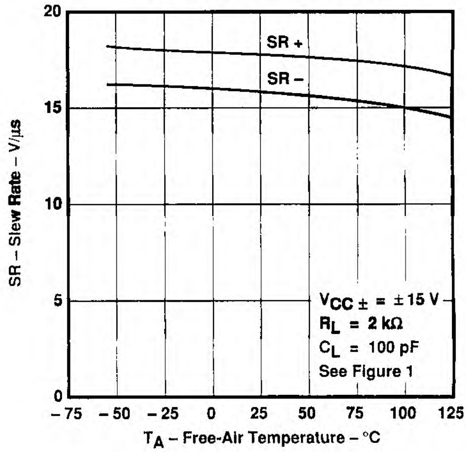


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

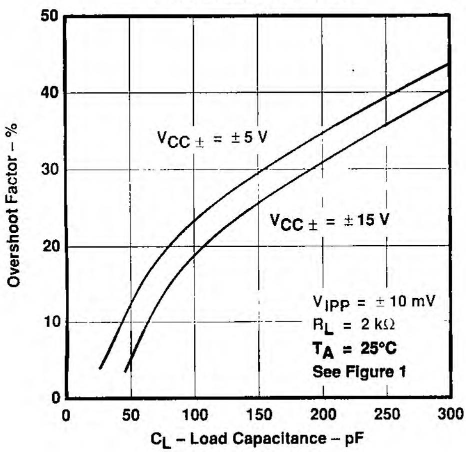


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

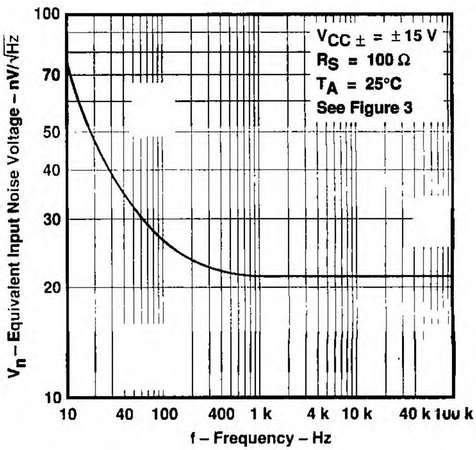


FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

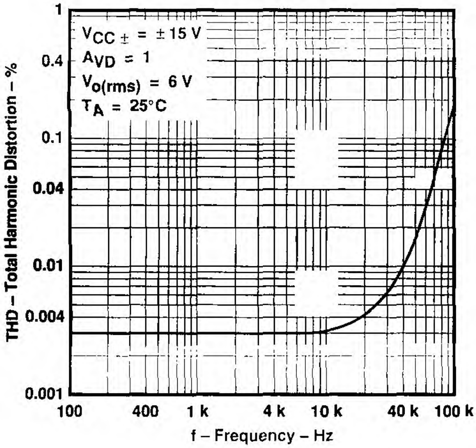


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

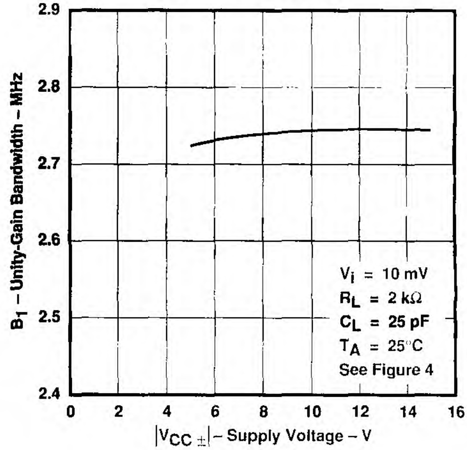


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

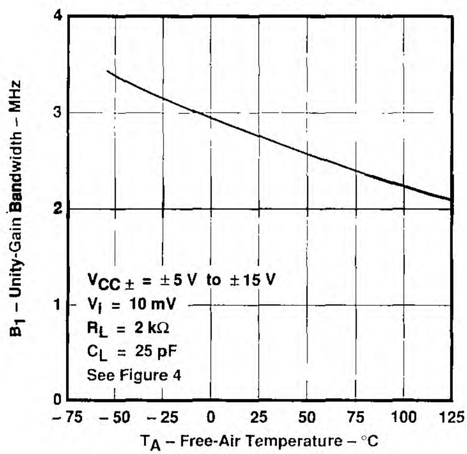


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

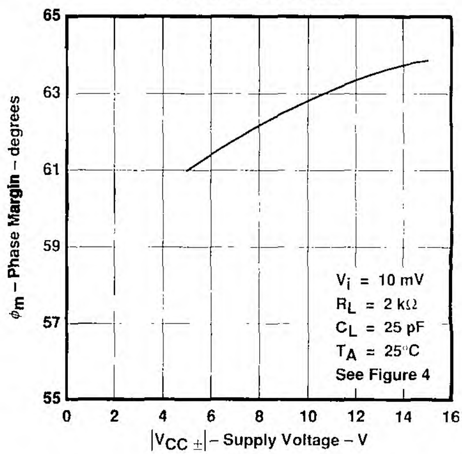


FIGURE 45

2
Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

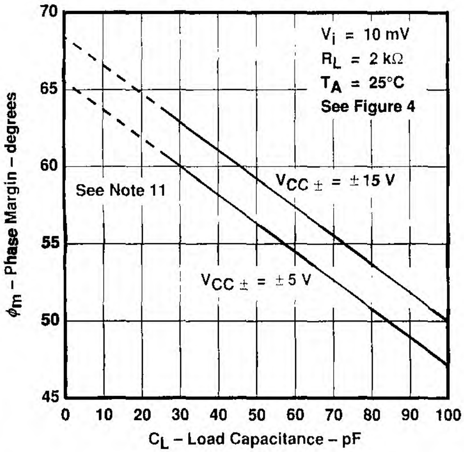


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

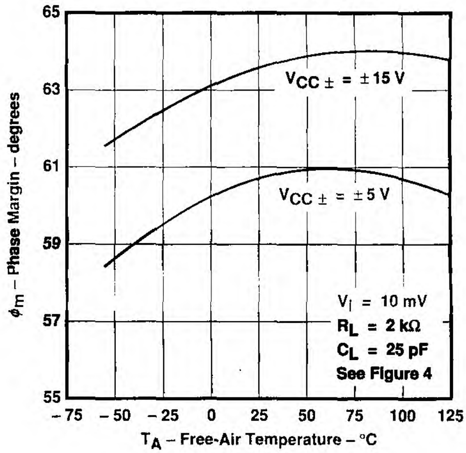


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

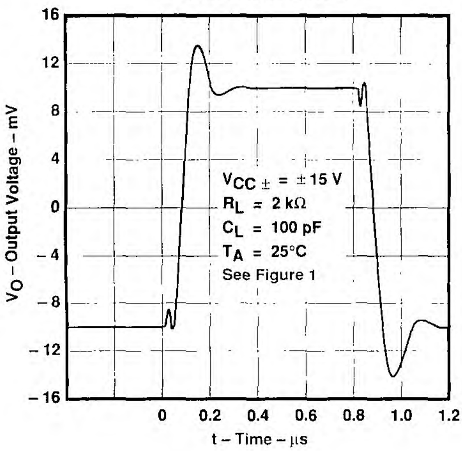


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

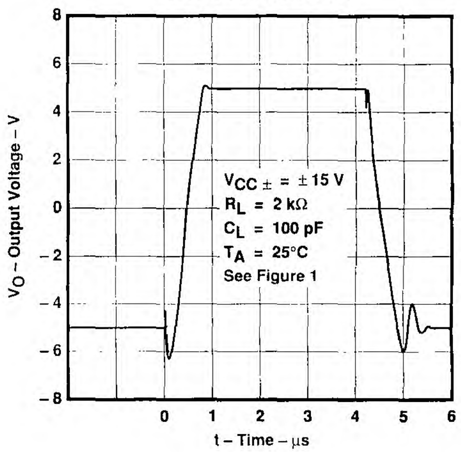


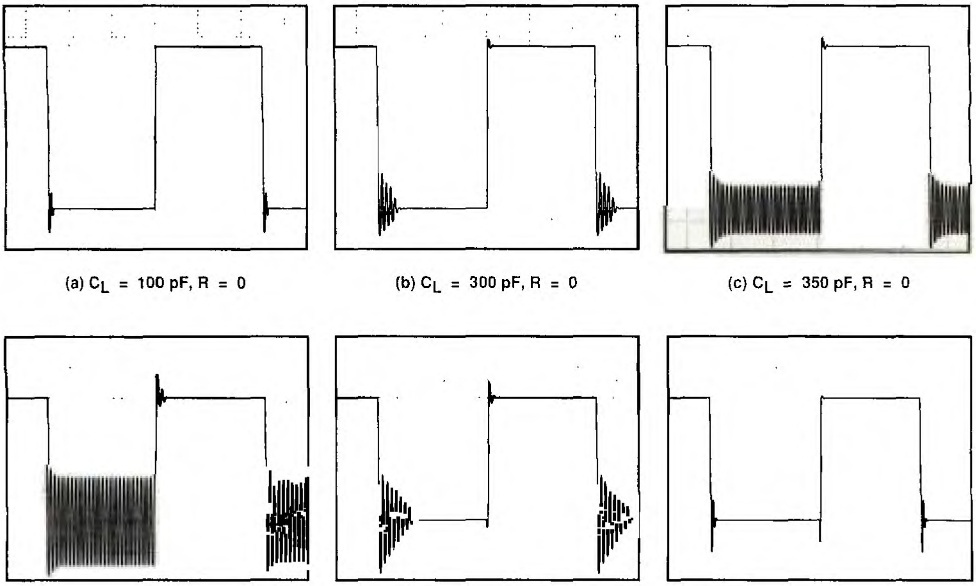
FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL APPLICATION DATA

output characteristics

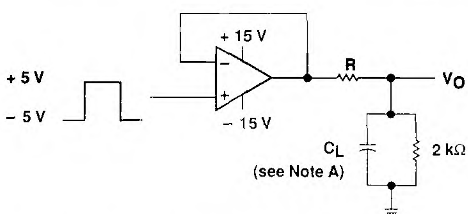
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL054 and TL054A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

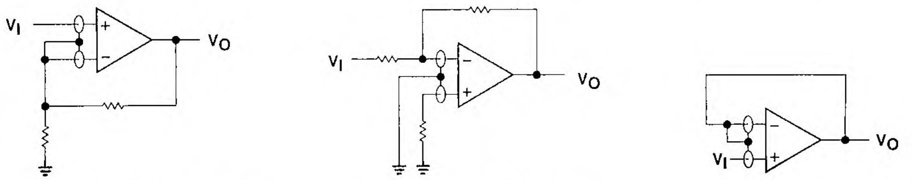
TYPICAL APPLICATION DATA

input characteristics

The TL054 and TL054A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL054 and TL054A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL054 and TL054A result in very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL054A. Amplifiers U1A, U1B, and U1C form the actual instrumentation amplifier, while U1D provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

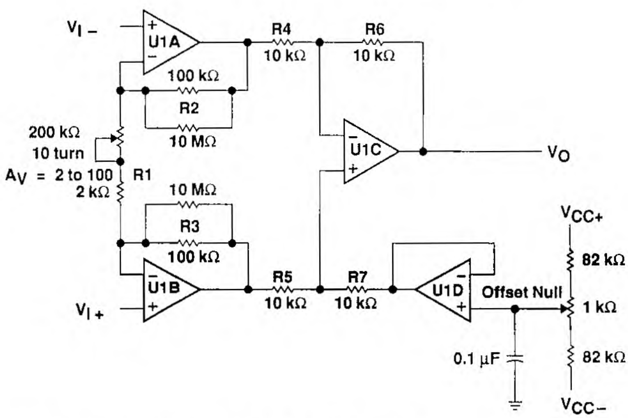
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U1D is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL054A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE A: U1A through U1D = TL054A; $V_{CC\pm}$ = ± 15 V.

FIGURE 53. INSTRUMENTATION AMPLIFIER

TYPICAL APPLICATION DATA

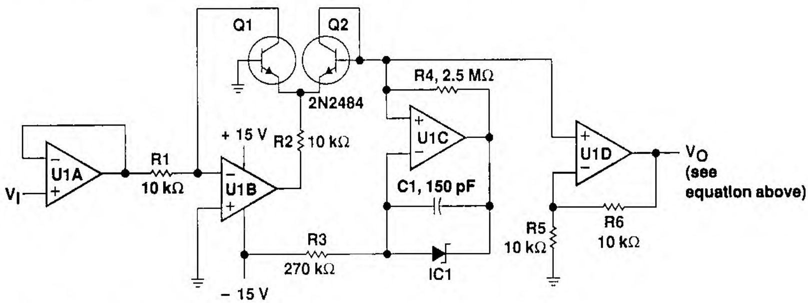
high input impedance log amplifier

The low input offset voltage and high input impedance of the TL054A create a precision log amplifier (see figure 54). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1 μA temperature-stable current source that sets the base-emitter voltage of Q2. Amplifier U1D then amplifies the difference between the base-emitter voltage of Q1 and Q2. The output voltage is given by the following equation:

$$V_O = -\left[1 + \frac{R6}{R5}\right]\frac{kT}{q}\left[\ln \frac{V_I}{(R1 \times 1 \times 10^{-6})}\right]$$

where k = 1.38×10^{-23}, q = 1.602×10^{-19}, and T is in kelvins.



NOTES: U1A thru U1D = TL054A.
IC1 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 54. LOG AMPLIFIER

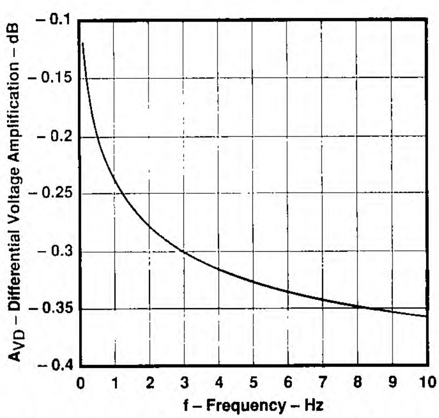


FIGURE 55. OUTPUT VOLTAGE vs INPUT VOLTAGE FOR LOG AMPLIFIER

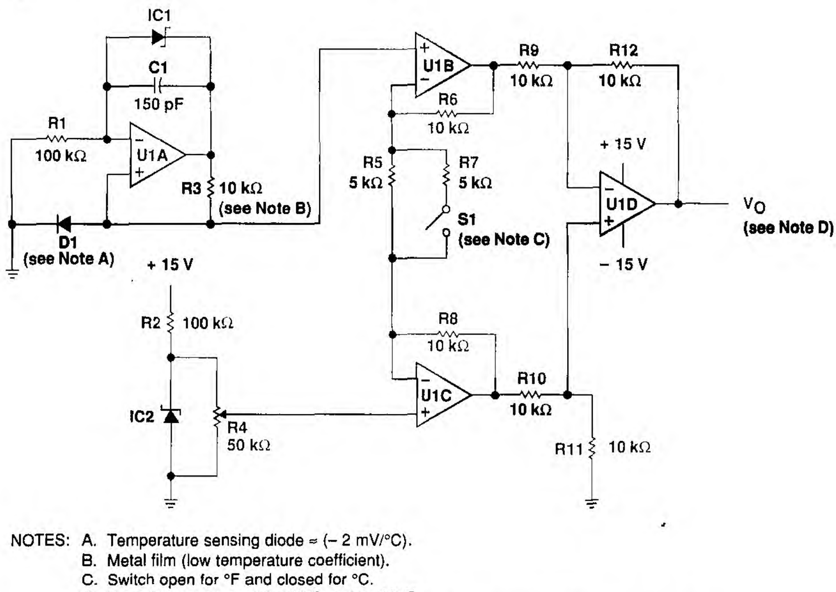
TYPICAL APPLICATION DATA

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 56). Amplifier U1A and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL054 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U1C, and U1D form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature sensing diode ≈ (− 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A thru U1D = TL054. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 56. ANALOG THERMOMETER

TYPICAL APPLICATION DATA

voltage-ratio-to-dB converter

The application in Figure 57 measures the amplitude ratio of two signals and then converts the ratio to decibels. The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoidal ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL054A devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL054A forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched NPN transistors.

The input signal first passes through a high impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2 so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-kΩ potentiometer on the input of U3C calibrates the zero dB reference level. The following equations are used to derive the relationship between the input voltage ratio expressed in decibels and the output voltage.

$$X\,dB = 20\log\left[\frac{V_A}{V_B}\right] = 20\left[\frac{\ln(V_A) - \ln(V_B)}{\ln(10)}\right]$$

$$X\,dB = 8.686\left[\ln(V_A) - \ln(V_B)\right]$$

$$V_{BE(Q1)} = \frac{kT}{q}\ln\left[\frac{V_A}{R \times I_S}\right] \qquad V_{BE(Q2)} = \frac{kT}{q}\ln\left[\frac{V_B}{R \times I_S}\right]$$

$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\left[\ln(V_A) - \ln(V_B)\right]$$

$$X\,dB = \frac{8.686}{kT/q}\left[V_{BE(Q1)} - V_{BE(Q2)}\right] = 336\left[V_{BE(Q1)} - V_{BE(Q2)}\right] \text{ at } 25°C.$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in kelvins.

This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

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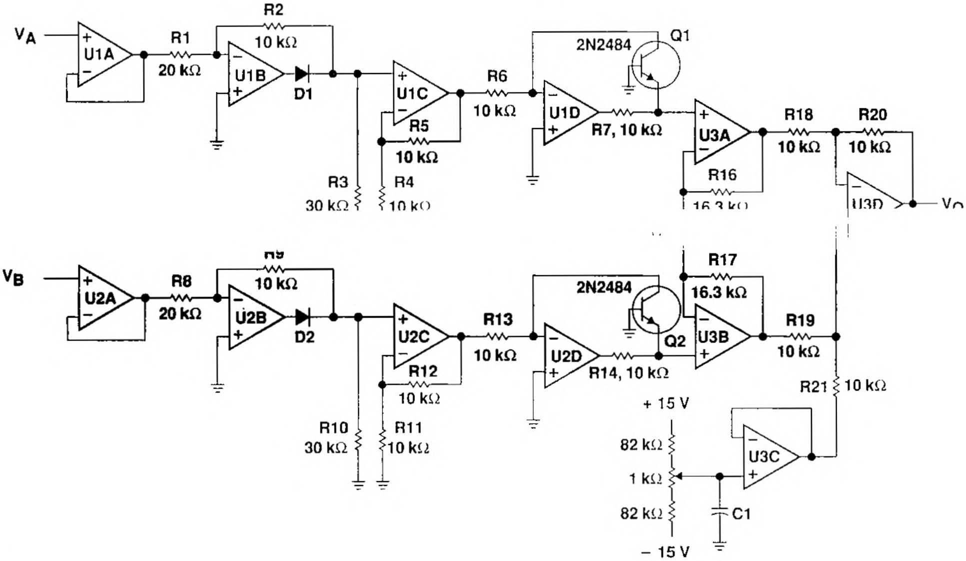
TYPICAL APPLICATION DATA



NOTES: U1A through U3D = TL054A, $V_{CC\pm}$ = ± 15 V.
D1 and D2 = 1N914.

FIGURE 57. VOLTAGE-RATIO-TO-dB CONVERTER

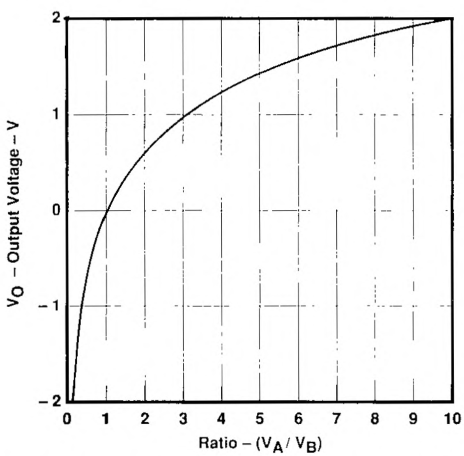


FIGURE 58. OUTPUT VOLTAGE vs THE RATIO OF THE INPUT VOLTAGES FOR VOLTAGE-TO-dB CONVERTER

20 DEVICES COVER MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

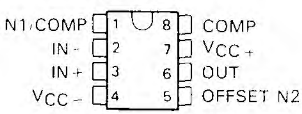
- Very Low Power Consumption
- Typical Supply Current . . . 200 μA (per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes V_{CC+}
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL060)
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/μs Typ

description

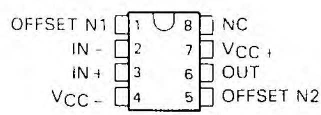
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

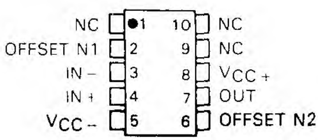
TL060, TL060A, TL060B
D, JG, OR P PACKAGE
(TOP VIEW)



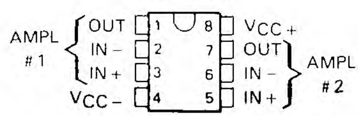
TL061, TL061A, TI061B
D, JG, OR P PACKAGE
(TOP VIEW)



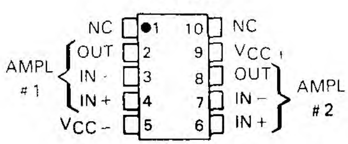
TL061 . . . U PACKAGE
(TOP VIEW)



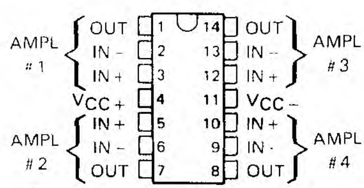
TL062, TL062A, TL062B
D, JG, OR P PACKAGE
(TOP VIEW)



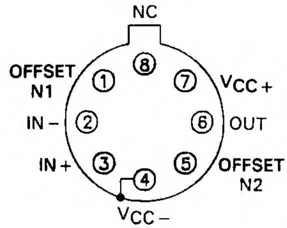
TL062 . . . U PACKAGE
(TOP VIEW)



TL064 . . . D, J, N, OR W PACKAGE
TL064A, TL064B . . . D, J, OR N PACKAGE
(TOP VIEW)

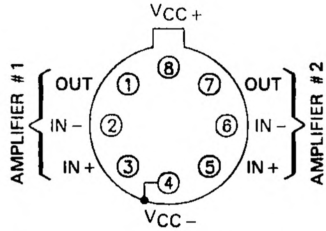


TL061 . . . L PACKAGE
(TOP VIEW)



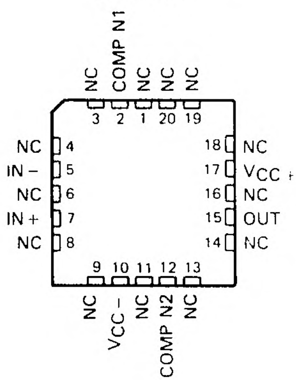
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL062 . . . L PACKAGE
(TOP VIEW)

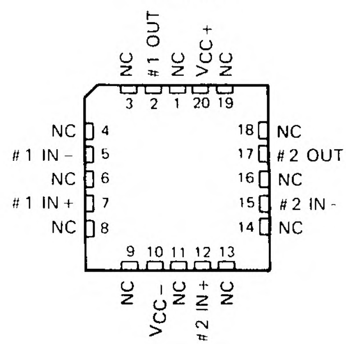


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

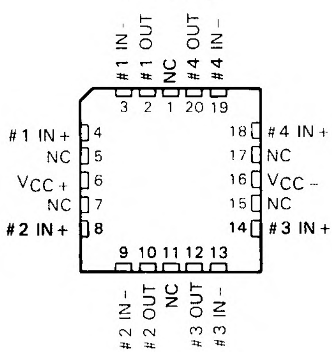
TL061 . . . FK PACKAGE
(TOP VIEW)



TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

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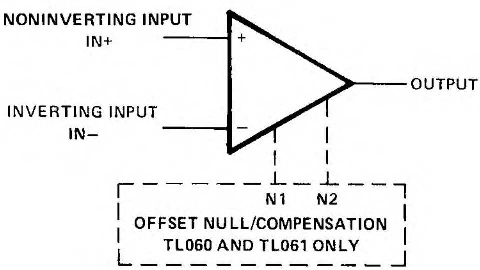
AVAILABLE OPTIONS

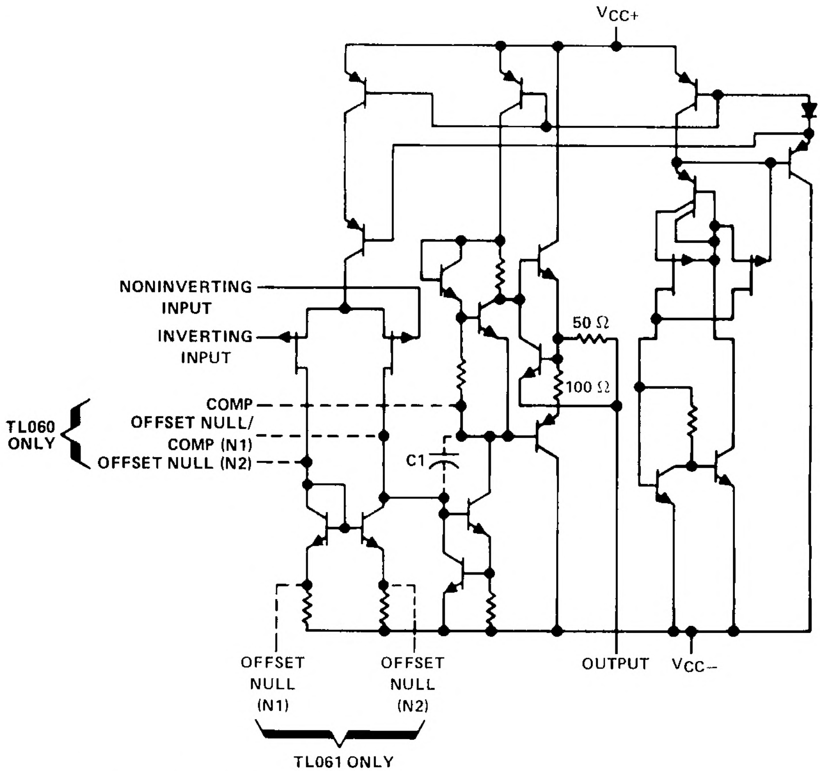
T_A	V_{IO} MAX at 25°C	PACKAGE SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLUG-IN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	15 mV	TL060CD			TL060CJG			TL060CP		
	6 mV	TL060ACD			TL060ACJG			TL060ACP		
	3 mV	[illegible]			[illegible]			TL060BCP		
	15 mV	[illegible]			[illegible]			TL061CP		
	6 mV	TL061ACD			TL061ACJG			TL061ACP		
	3 mV	[illegible]			TL061BCJG			[illegible]		
	15 mV	[illegible]			TL062CJG			[illegible]		
	6 mV	TL062ACD			TL062ACJG			TL062ACP		
	3 mV	TL062BCD			TL062BCJG			TL062BCP		
	15 mV	TL064CD		TL064CJ			TL064CN			
	6 mV	TL064ACD		TL064ACJ			TL064ACN			
	3 mV	TL064BCD		TL064BCJ			TL064BCN			
−40°C to 85°C	6 mV	TL060ID			TL060IJG			TL060IP		
	6 mV	TL061ID			TL061IJG			TL061IP		
	6 mV	TL062ID			TL062IJG			TL062IP		
	6 mV	TL064ID		TL064IJ			TL064IN			
−55°C to 125°C	6 mV		TL061MFK		TL061MJG	TL061ML			TL061MU	
	6 mV		TL062MFK		TL062MJG	TL062ML			TL062MU	
	9 mV		TL064MFK	TL064MJ						TL064MW

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL061CDR).

symbol (each amplifier)



schematic (each amplifier)



C1 = 10 pF ON TL061, TL062, AND TL064 ONLY
COMPONENT VALUES SHOWN ARE NOMINAL

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL06_M	TL06_I	TL06_C, TL06_AC, TL06_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to [illegible]	−40 to 85	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N or P package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300			°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	[illegible] mW	5.8 mW/°C	33°C	464 mW	[illegible] mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL06_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL06_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
L	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061M TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω,	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	mV
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			10			10		µV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		30	200		30	[illegible]	pA
			T_A = −55°C to 125°C			50			[illegible]	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = −55°C to 125°C	±10			±10			V
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V,	T_A = 25°C	4	6		4	6		V/mV
		R_L ≥ 10 kΩ	T_A = −55°C to 125°C	4			4			V/mV
B_1	Unity-gain bandwidth	R_L = 10 kΩ,	T_A = 25°C							MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, V_O = 0, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			200	250		200	250	µA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL060I TL061I TL062I TL064I			TL060C TL061C TL062C TL064C			TL060AC TL061AC TL062AC TL064AC			TL060BC TL061BC TL062BC TL064BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			10			10			10			10		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			5			3			3	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	400		30	200		30	200	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11.5	−12 to +15		±11	−12 to +15		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$, $T_A = 25°C$		±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		$R_L \geq 10\ k\Omega$, T_A = full range		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 10\ k\Omega$	$T_A = 25°C$	4	6		3	6		4	6		4	6		V/mV
			T_A = full range	4			3			4			4			
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$, $T_A = 25°C$			1			1			1			1		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC\pm}/\Delta V_{IO})$	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	95		70	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			200	250		200	250		200	250		200	250	µA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL06_I and 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC.

‡ Input bias currents of a FET input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 1[illegible]se techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ,		0.2		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

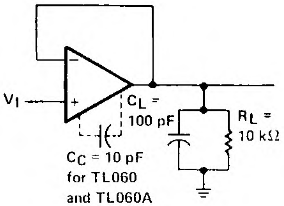


FIGURE 1. UNITY-GAIN AMPLIFIER

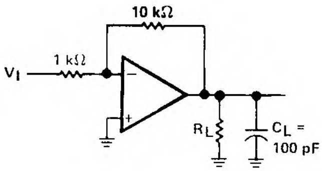


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

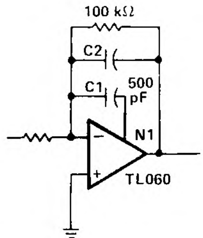
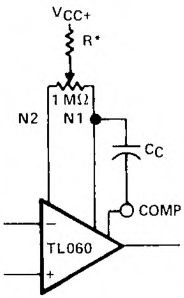


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS



*For best results use R = 20 MΩ for $V_{CC\pm} = \pm 15$ V to R = 5 MΩ for $V_{CC\pm} = \pm 3$ V.

FIGURE 4

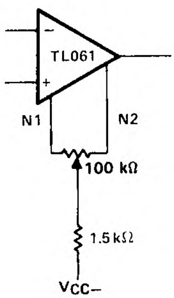


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

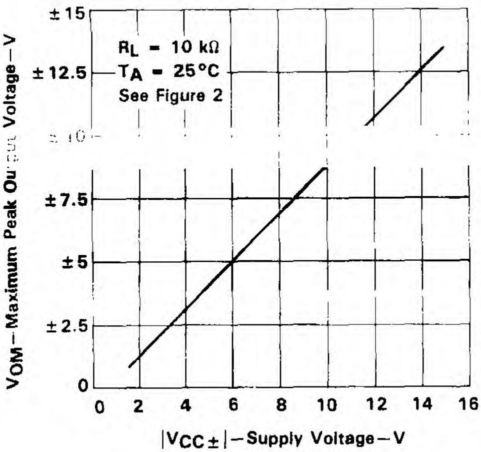


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

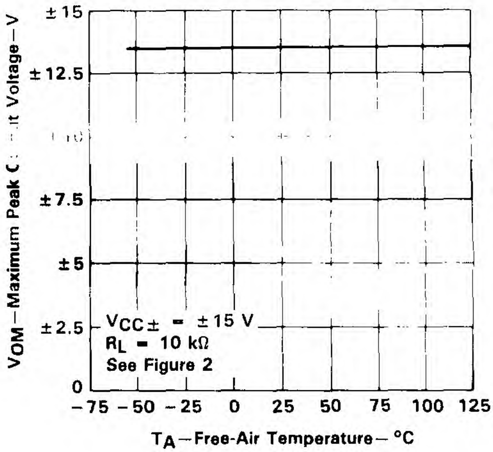


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

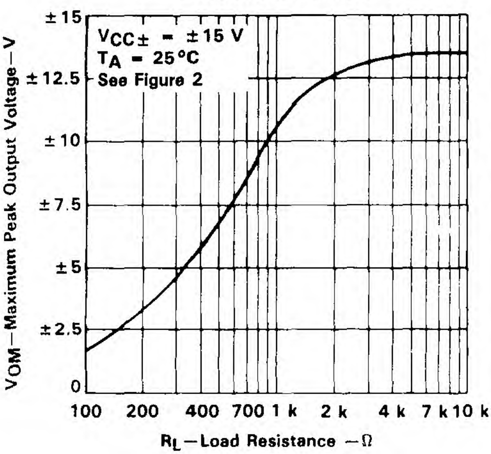


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

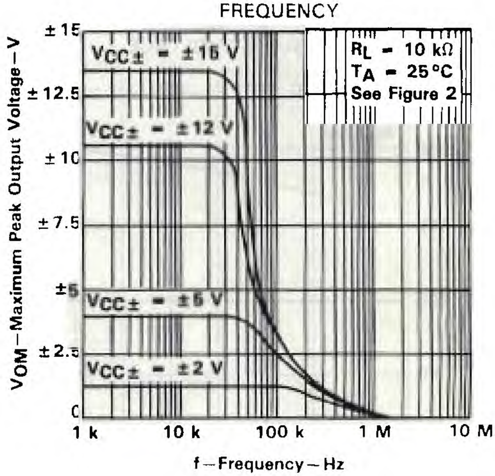


FIGURE 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

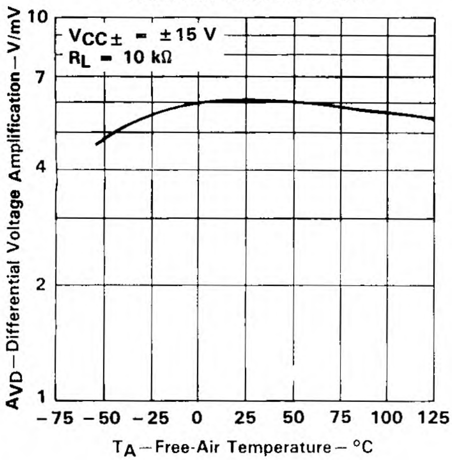


FIGURE 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

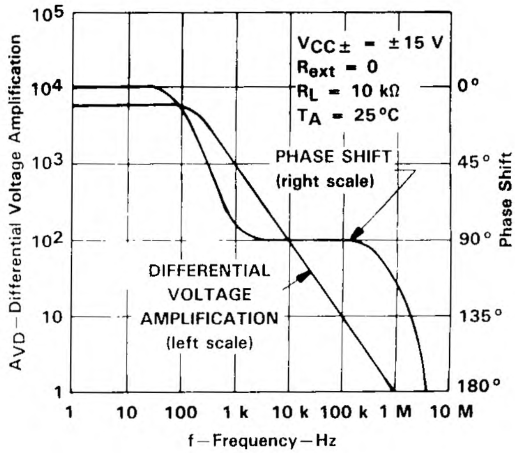


FIGURE 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

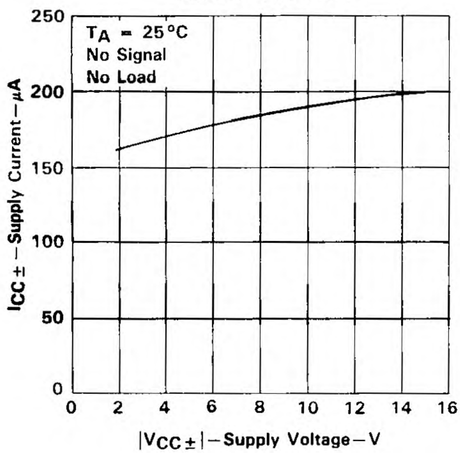


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

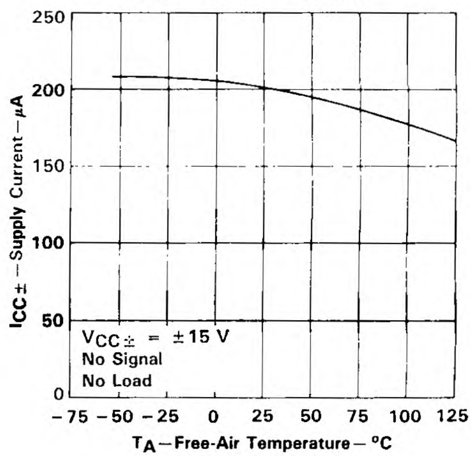


FIGURE 13

†A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

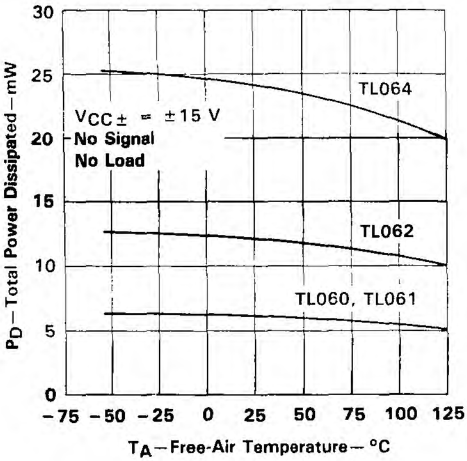


FIGURE 14

ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

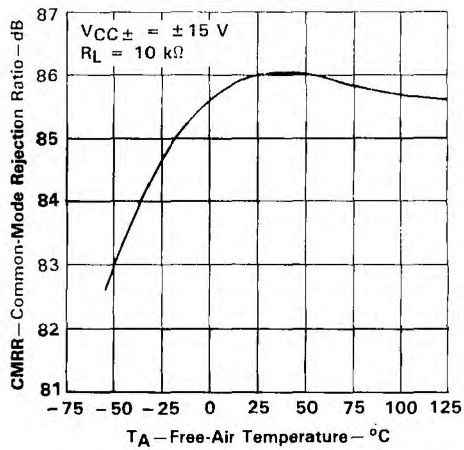


FIGURE 15

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

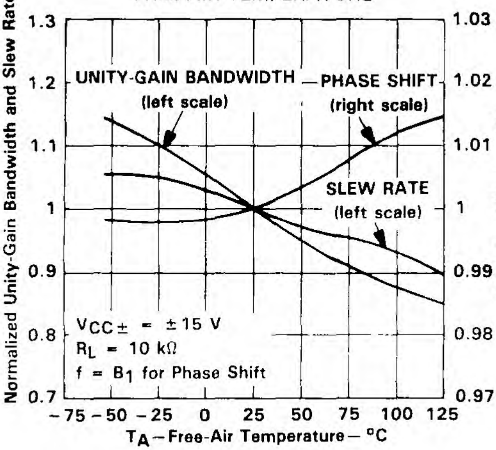


FIGURE 16

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

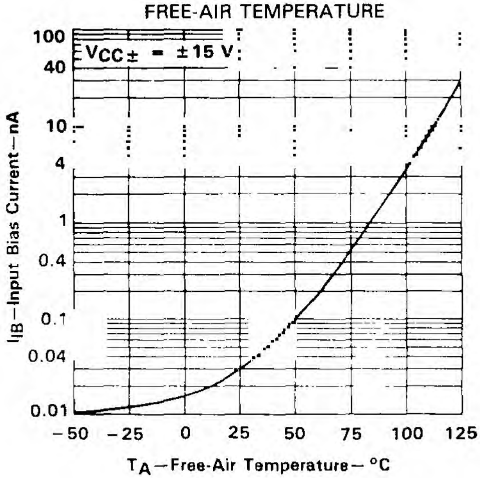


FIGURE 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

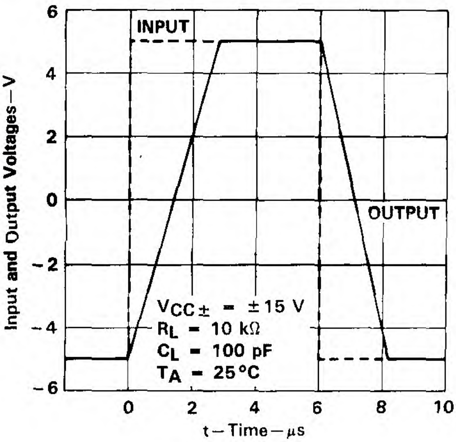


FIGURE 18

OUTPUT VOLTAGE
vs
ELAPSED TIME

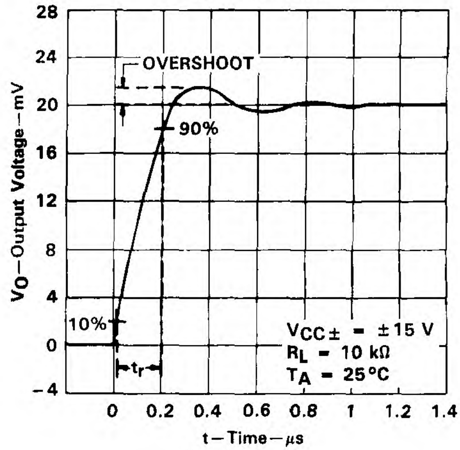


FIGURE 19

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

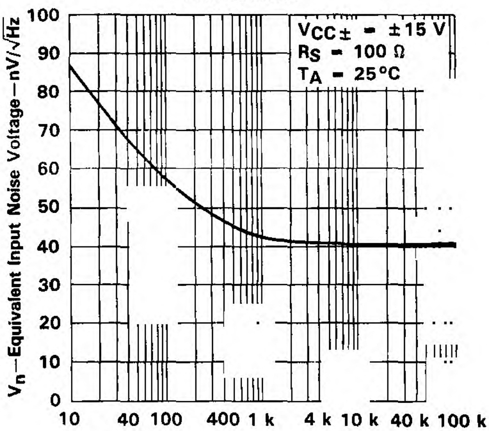


FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

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TYPICAL APPLICATION DATA

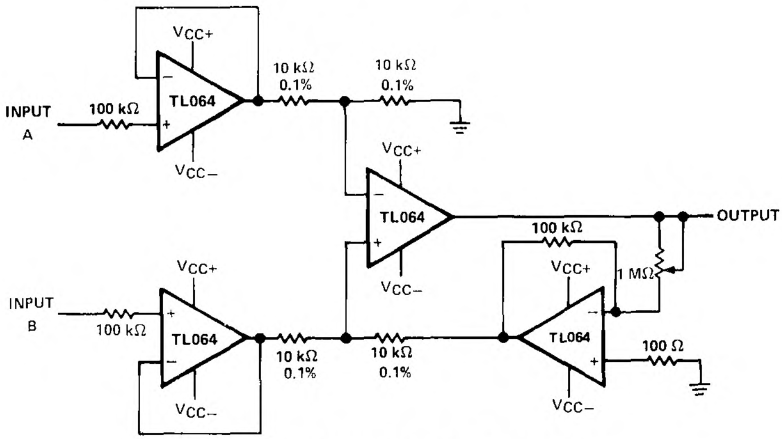
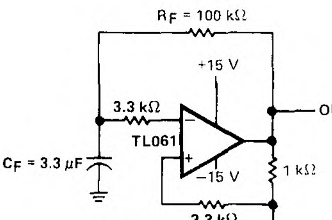
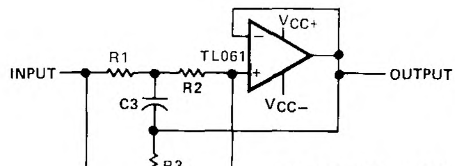


FIGURE 21. INSTRUMENTATION AMPLIFIER



$$f = \frac{1}{2\pi R_F C_F}$$

FIGURE 22. 0.5-Hz SQUARE-WAVE OSCILLATOR



R1 = R2 = 2R3 = 1.5 MΩ

$$C1 = C2 = \frac{C3}{2} = 110\ \text{pF}$$

$$f_o = \frac{1}{2\pi\, R1\, C1} = 1\ \text{kHz}$$

FIGURE 23. HIGH-Q NOTCH FILTER

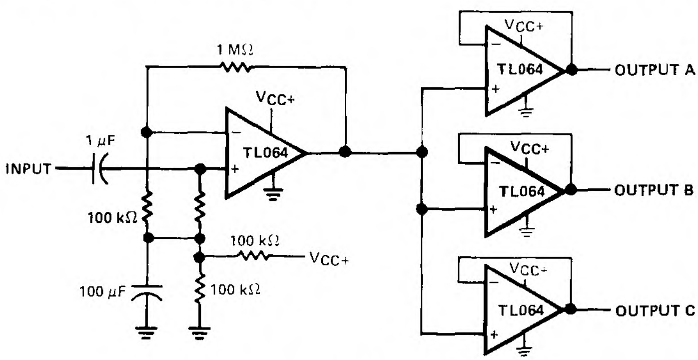


FIGURE 24. AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA

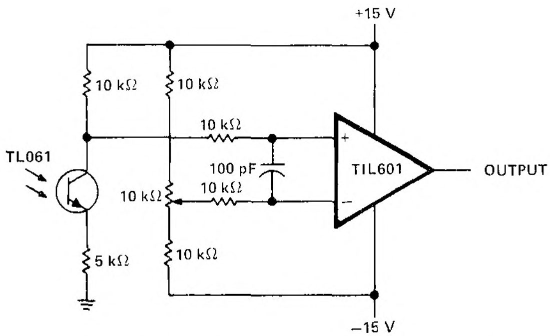


FIGURE 25. LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

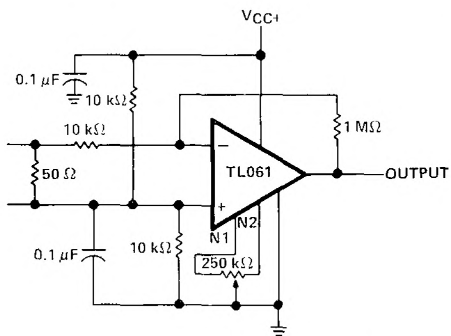


FIGURE 26. AC AMPLIFIER

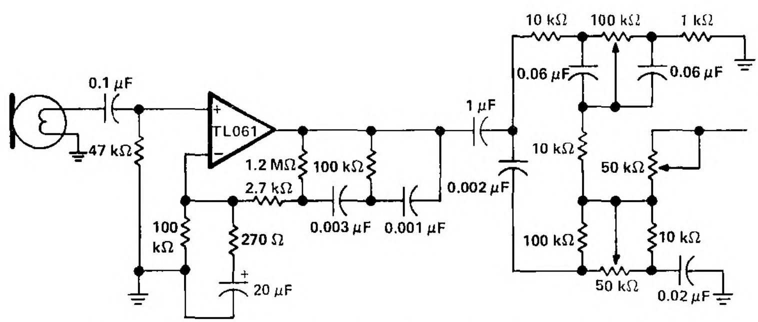


FIGURE 27. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

TYPICAL APPLICATION DATA

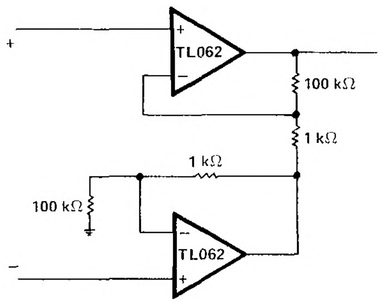


FIGURE 28. INSTRUMENTATION AMPLIFIER

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

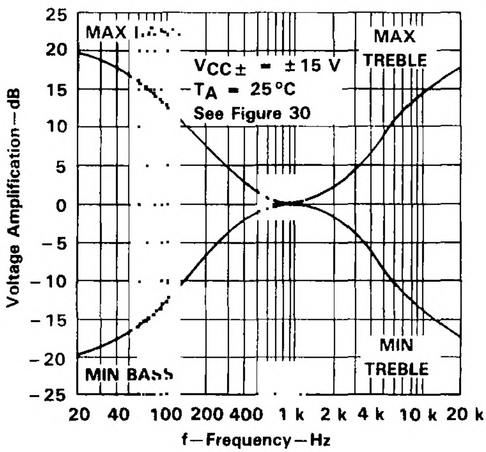


FIGURE 29

TYPICAL APPLICATION DATA

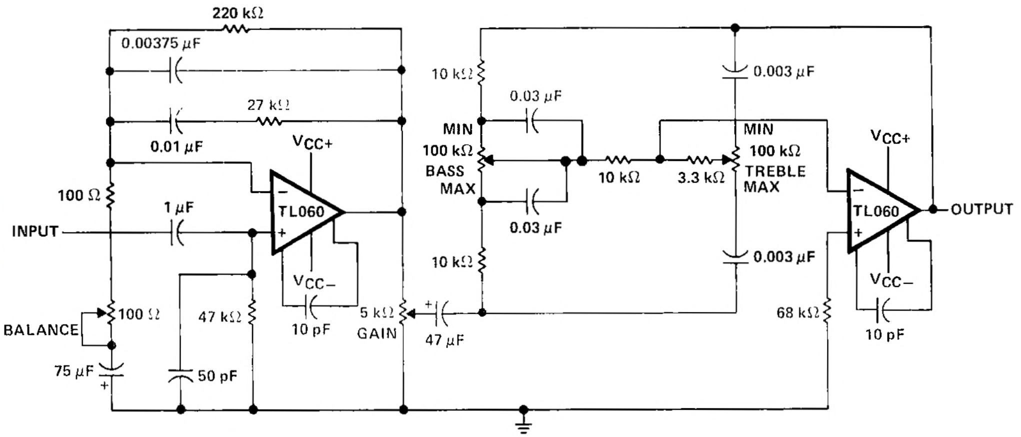


FIGURE 30. IC PREAMPLIFIER

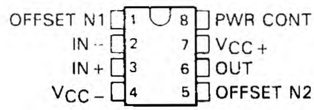
D2494, FEBRUARY 1979—REVISED NOVEMBER 1988

TL066M, TL066I, TL066C, TL066AC, TL066BC ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

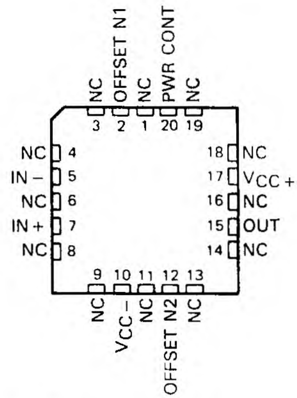
5 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- **Very Low, Adjustable ("Programmable") Power Consumption**
- **Adjustable Supply Current . . . 5 μA to 200 μA**
- **Very Low Input Bias and Offset Currents**
- **Wide Supply Range . . . ±1.2 V to ±18 V**
- **Wide Common-Mode and Differential Voltage Range**
- **Output Short-Circuit Protection**
- **High Input Impedance . . . JFET-Input Stage**
- **Unity-Gain Bandwidth . . . 1 MHz Typ (100 kHz at 25 μW)**
- **High Slew Rate . . . 3.5 V/μs Typ**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

TL066M . . . JG PACKAGE
TL066I, TL066C, TL066AC, TL066BC . . . D, JG, OR P PACKAGE
(TOP VIEW)



TL066M . . . FK PACKAGE
(TOP VIEW)



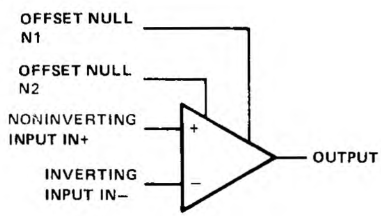
NC—No internal connection

TL066M IS NOT RECOMMENDED FOR NEW DESIGNS

description

The TL066, TL066A, and TL066B are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 μW of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable." The JFET-input stage combined with the adjustable-low-power feature results in superior bandwidth and slew-rate performance compared to low-power bipolar-input devices.

symbol



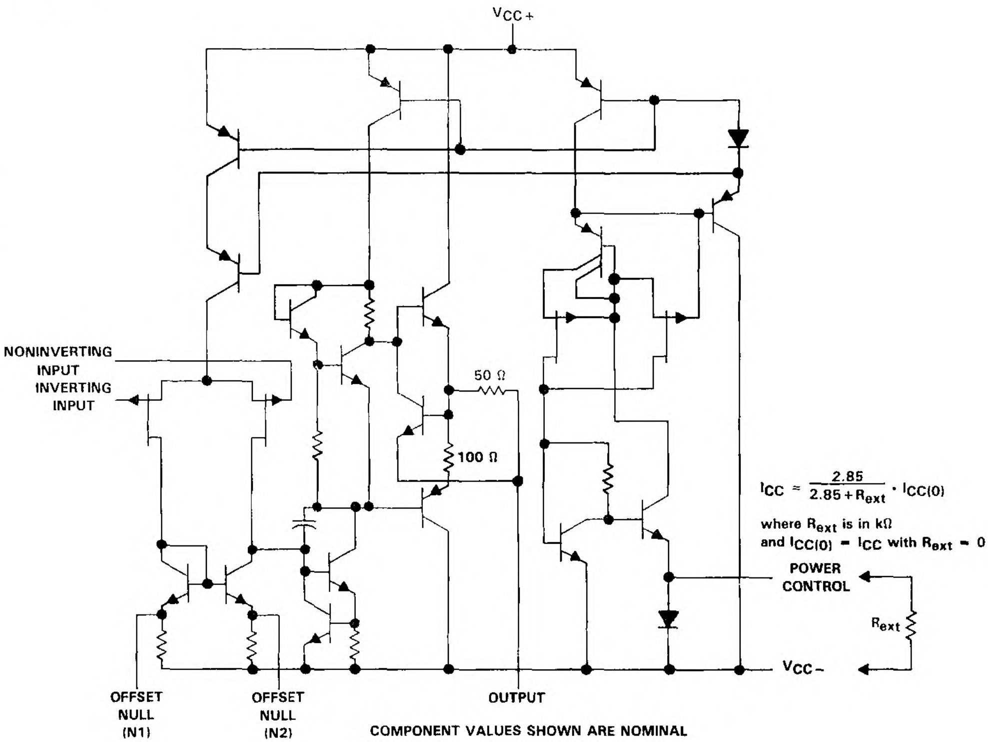
The TL066M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL066I is characterized for operation from −40°C to 85°C; the TL066C, TL066AC, and TL066BC are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	15 mV 6 mV 3 mV	TL066CD TL066ACD TL066BCD		TL066CJG TL066ACJG TL066BCJG	TL066CP TL066ACP TL066BCP
−40°C to 85°C	6 mV	TL066ID		TL066IJG	TL066IP
−55°C to 125°C	6 mV		TL066MFK	TL066MJG	

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TL066CDR).

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL066M	TL066I	TL066C, TL066AC, TL066BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to [illegible]	−65 to 150	°C
Case temperature for 60 seconds	FK package	260	[illegible]	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	[illegible]	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		[illegible]	[illegible]	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG (TL066M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

2 Operational Amplifiers

electrical characteristics, $V_{CC} = \pm 15$ V

PARAMETER		TEST CONDITIONS†	TL066M			TL066I			TL066C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		3	6		3	6		3	15	mV
		$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			9			9			20	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$, $T_A = 25°C$		5	100		5	100		5	200	pA
		$V_O = 0$, T_A = full range			20			10			5	nA
I_{IB}	Input bias current‡	$V_O = 0$, $T_A = 25°C$		30	200		30	200		30	400	pA
		$V_O = 0$, T_A = full range			50			20			10	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$	±11.5	−12 to +15		±11.5	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$, $R_L \geq 10\ k\Omega$	±10	±13.5		±10	±13.5		±10	±13.5		V
		T_A = full range, $R_L \geq 10\ k\Omega$	±10	±13.5		±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 10\ k\Omega$, $V_O = \pm 10$ V, $T_A = 25°C$	4	6		4	6		3	6		V/mV
		$R_L \geq 10\ k\Omega$, $V_O = \pm 10$ V, T_A = full range	4						3			
B_1	Unity-gain bandwidth	$T_A = 25°C$, $R_L = 10\ k\Omega$		1			1			1		MHz
r_i	Input resistance	$T_A = 25°C$		10^{12}			10^{12}			10^{12}		Ω
r_o	Output resistance	$T_A = 25°C$, f = 1 kHz		220			220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$	80	86		80	86		70	76		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$	80	95		80	95		70	95		dB
P_D	Total power dissipation	$V_O = 0$, No load, $T_A = 25°C$		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current	$V_O = 0$, No load, $T_A = 25°C$		200	250		200	250		200	250	μA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is −55°C to 125°C for TL066M; −40°C to 85°C for TL066I; and 0°C to 70°C for TL066C. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†		TL066AC			TL066BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, T_A = 25°C	R_S = 50 Ω,		3	6		2	3	mV
		V_O = 0, T_A = full range	R_S = 50 Ω,			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, T_A = full range	R_S = 50 Ω,		10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0,	T_A = 25°C		5	100		5	100	pA
		V_O = 0,	T_A = full range			3			3	nA
I_{IB}	Input bias current‡	V_O = 0,	T_A = 25°C		30	200		30	200	pA
		V_O = 0,	T_A = full range			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to ±15		±11.5	−12 to ±15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L ≥ 10 kΩ,	±10	±13.5		±10	±13.5		V
		T_A = full range,	R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, T_A = 25°C	V_O = ±10 V,	4	6		4	6		V/mV
		R_L ≥ 10 kΩ, T_A = full range	V_O = ±10 V,	4			4			
B_1	Unity-gain bandwidth	T_A = 25°C,	R_L = 10 kΩ		1			1		[illegible]
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		[illegible]
r_o	Output resistance	T_A = 25°C,	f = 1 kHz		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	95		80	95		dB
P_D	Total power dissipation	No load, T_A = 25°C	V_O = 0,		6	7.5		6	7.5	mW
I_{CC}	Supply current	No load, T_A = 25°C	V_O = 0,		200	250		200	250	μA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is −55°C to 125°C for TL066M; −40°C to 85°C for TL066I; and 0°C to 70°C for TL066C, TL066AC, and TL066BC. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$, $R_{ext} = 0$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ		0.2		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz		42		nV/$\sqrt{Hz}$

PARAMETER MEASUREMENT INFORMATION

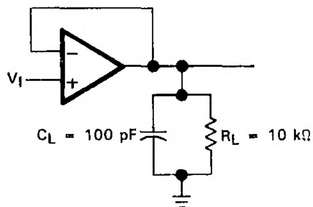


FIGURE 1. UNITY-GAIN AMPLIFIER

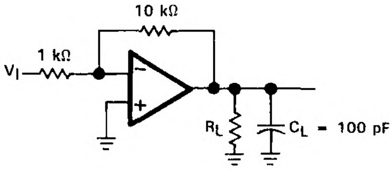


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

INPUT OFFSET VOLTAGE NULL CIRCUIT

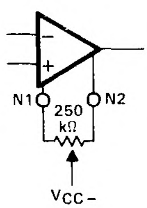


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

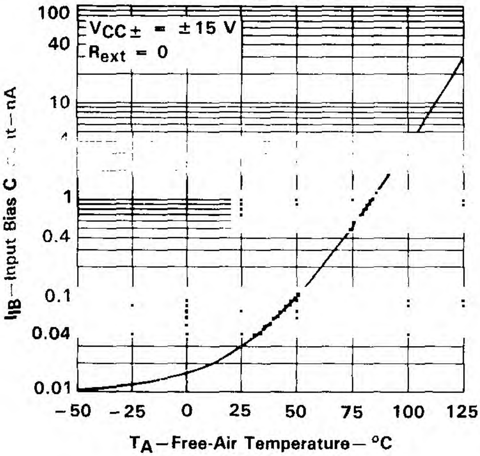


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

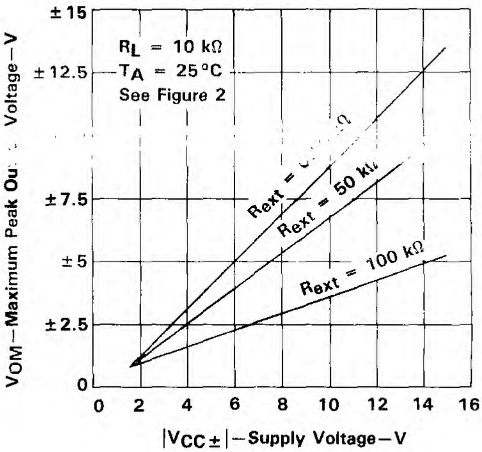


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
EXTERNAL CONTROL RESISTANCE

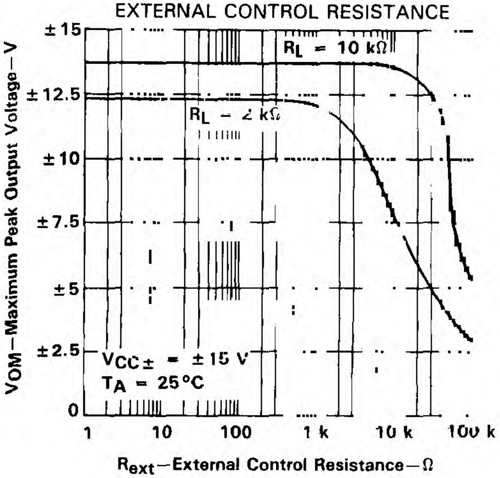


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

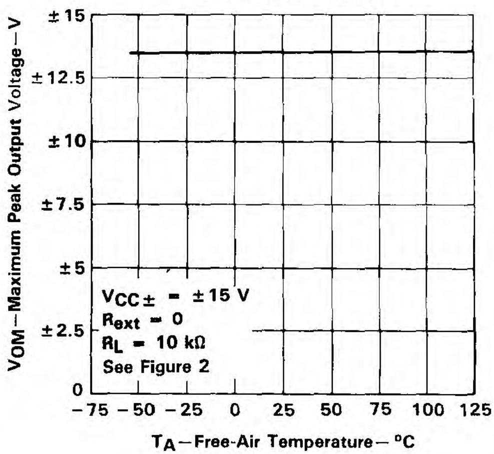


FIGURE 7

† Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

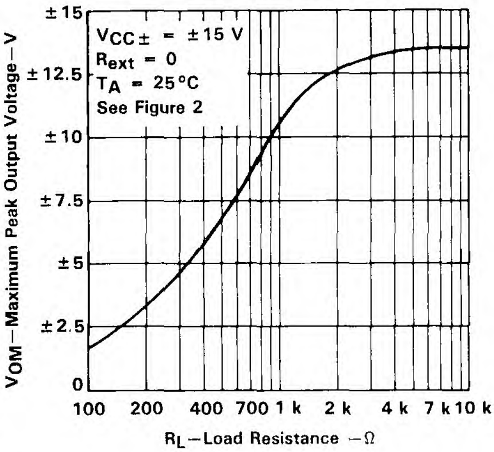


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

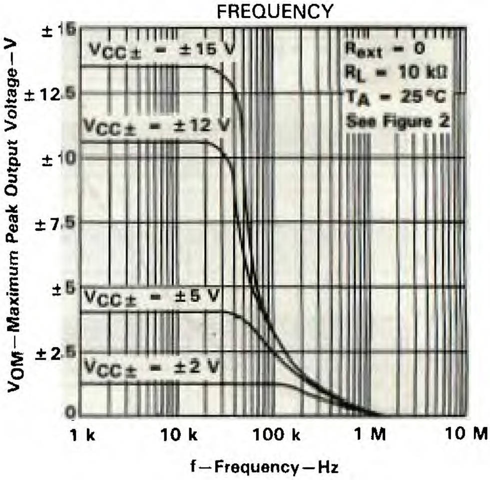


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
EXTERNAL CONTROL RESISTANCE

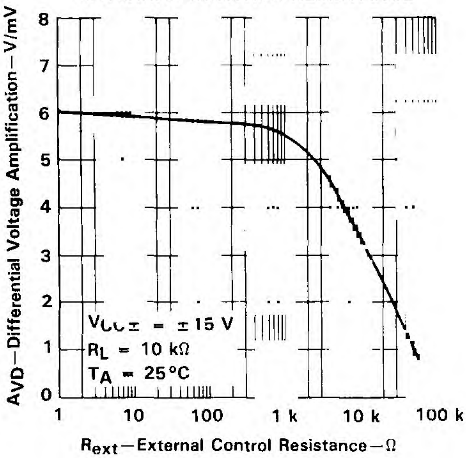


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

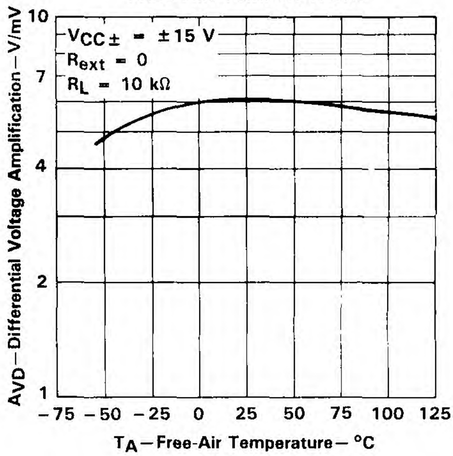


FIGURE 11

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

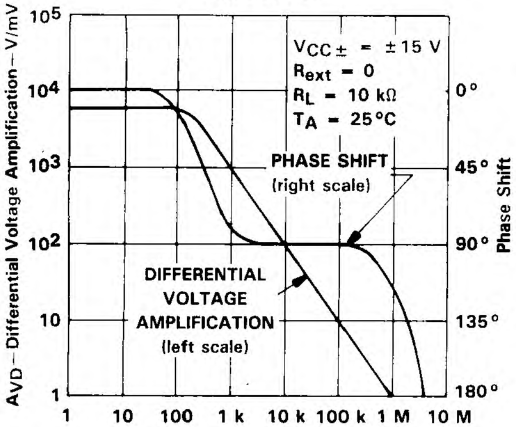


FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

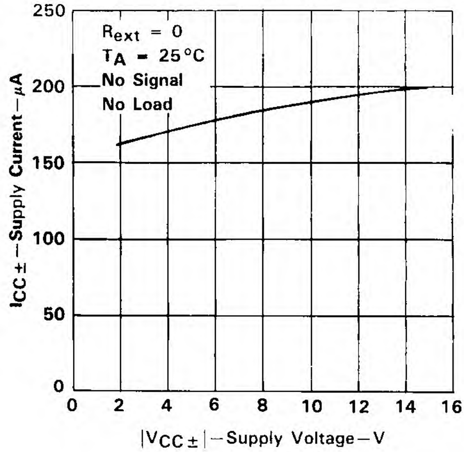


FIGURE 13

SUPPLY CURRENT
vs
EXTERNAL CONTROL RESISTANCE

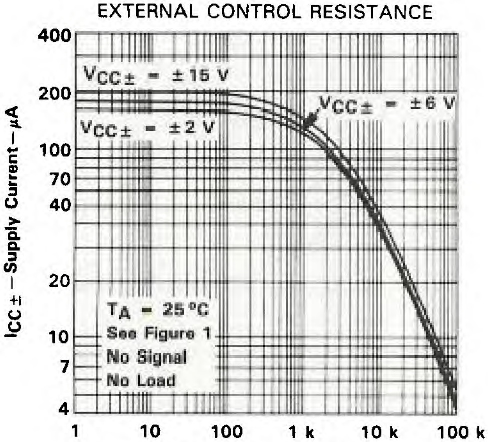


FIGURE 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

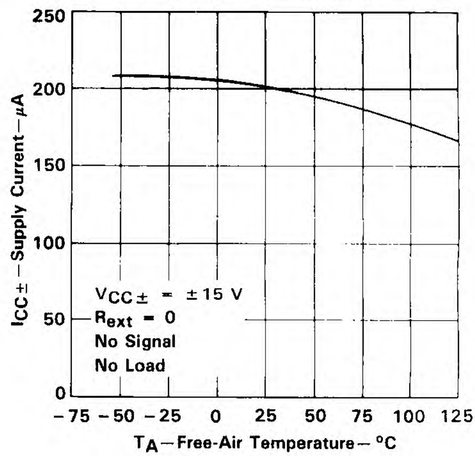


FIGURE 15

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATION
vs
EXTERNAL CONTROL RESISTANCE

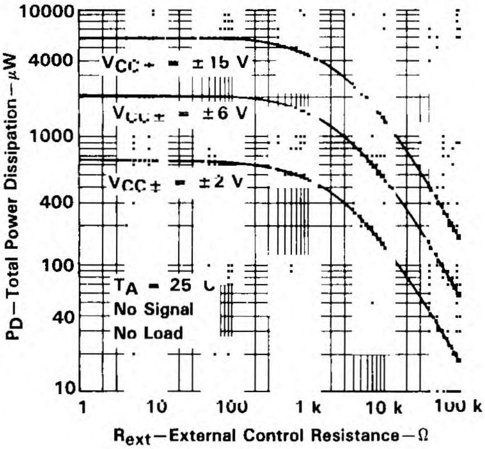


FIGURE 16

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
EXTERNAL CONTROL RESISTANCE

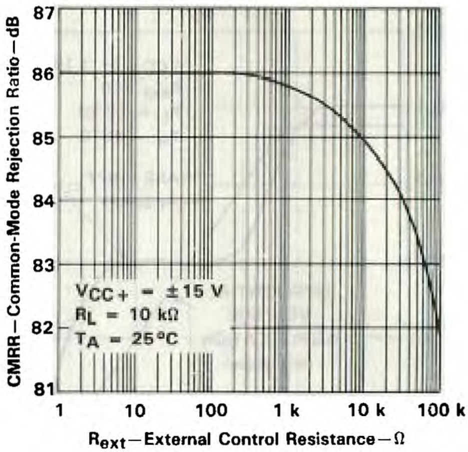


FIGURE 17

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

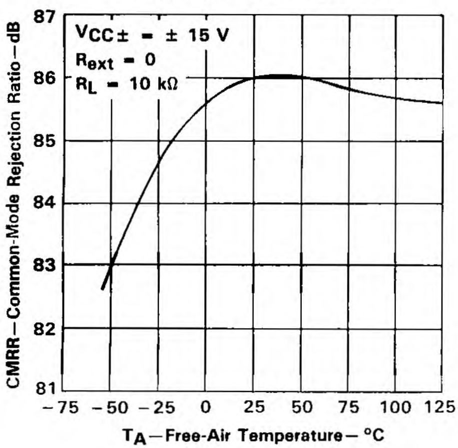


FIGURE 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

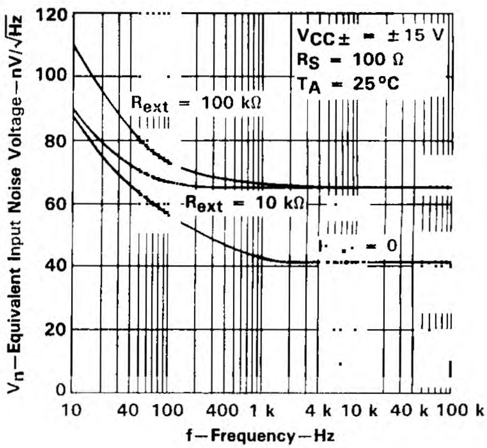


FIGURE 19

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

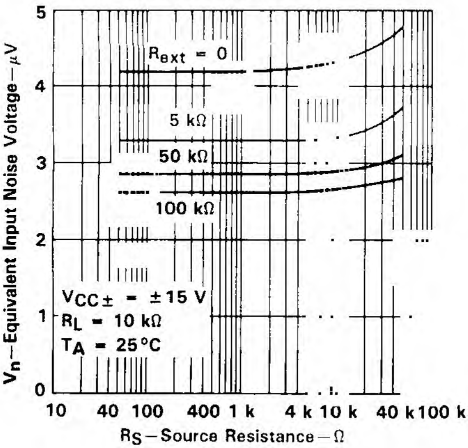


FIGURE 20

UNITY GAIN BANDWIDTH
vs
EXTERNAL CONTROL RESISTANCE

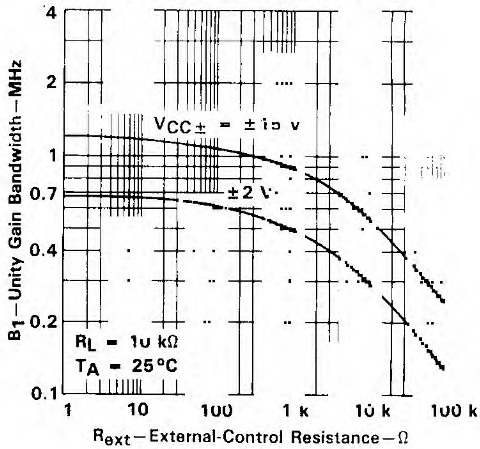


FIGURE 21

SLEW RATE
vs
EXTERNAL CONTROL RESISTANCE

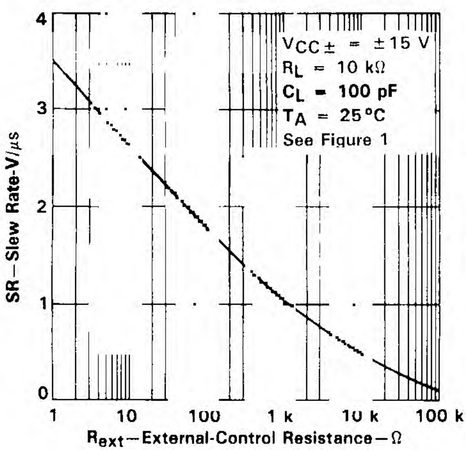


FIGURE 22

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

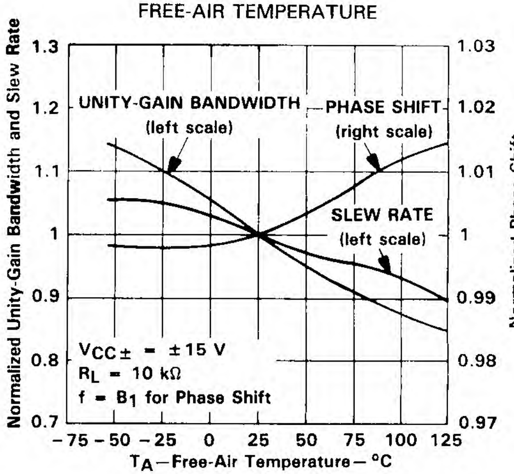


FIGURE 23

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

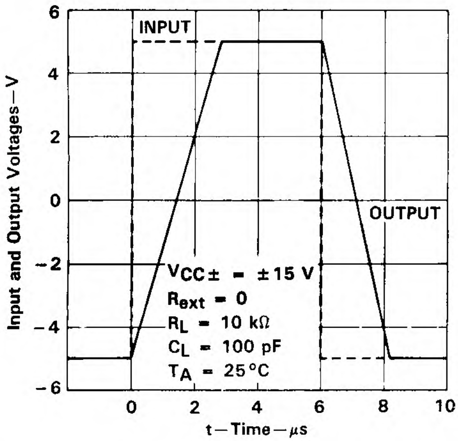


FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

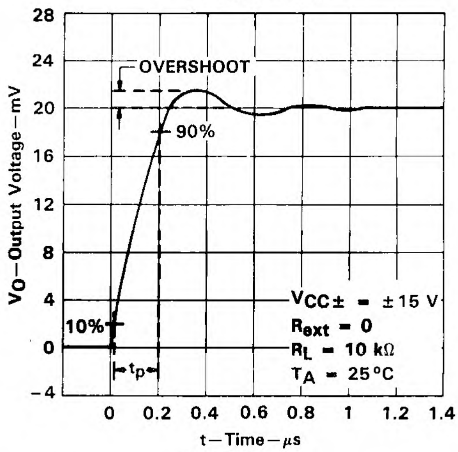


FIGURE 25

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

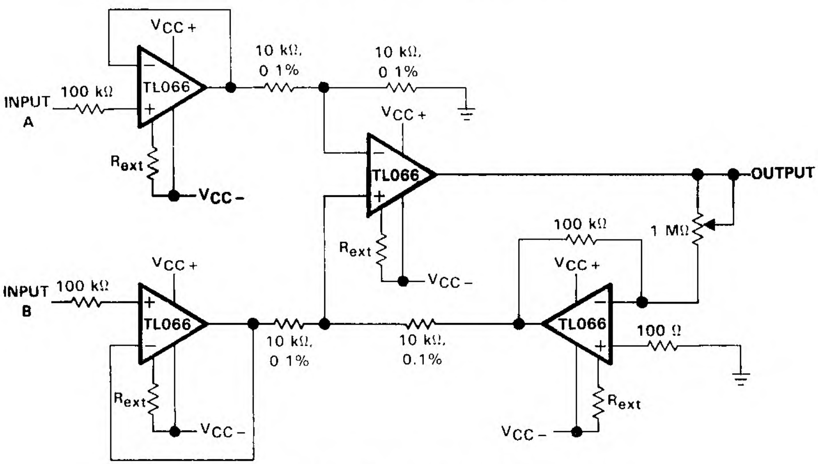


FIGURE 26. INSTRUMENTATION AMPLIFIER

TYPICAL APPLICATION DATA

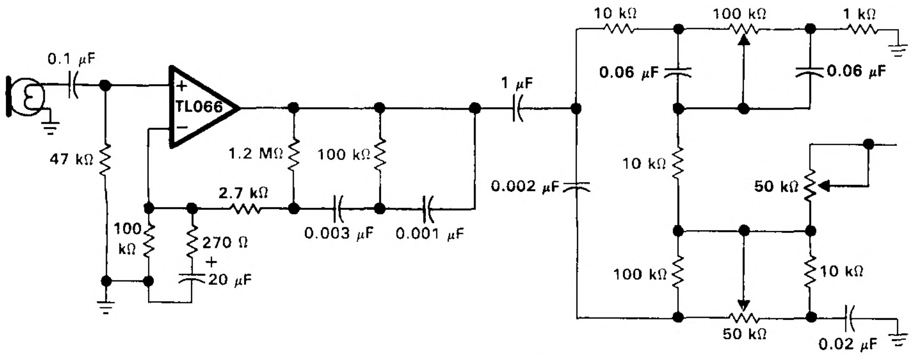


FIGURE 27. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

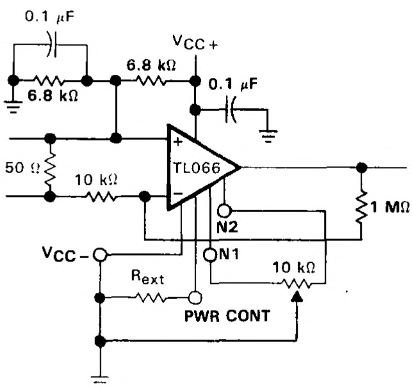


FIGURE 28. AC AMPLIFIER

TYPICAL APPLICATION DATA

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

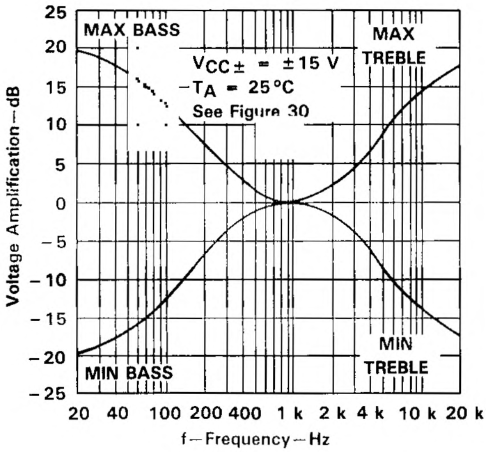


FIGURE 29

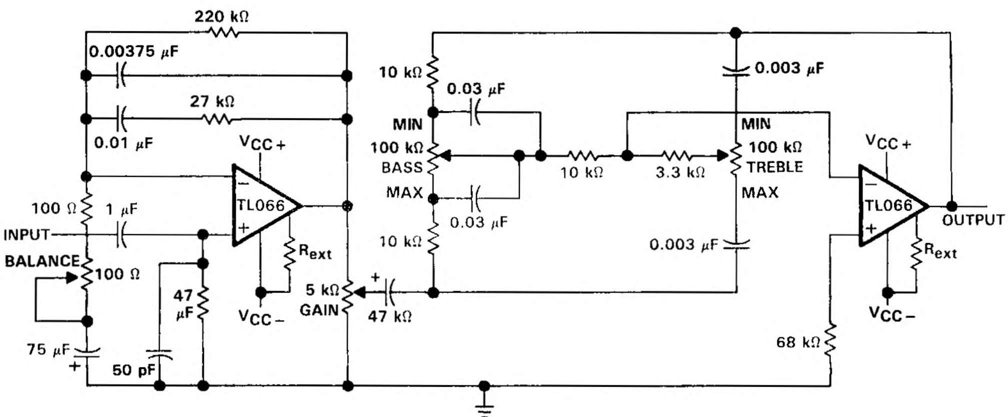


FIGURE 30. IC PREAMPLIFIER

19 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Low Noise . . . V_n = 18 nV/√Hz Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation (Except TL070, TL070A)**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**

description

The JFET-input operational amplifiers in the TL07__ series are designed as low-noise versions of the TL08__ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07__ series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

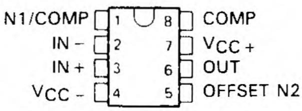
The M suffix devices are characterized for operation over the full military temperature range of −55 °C to 125 °C. The I suffix devices are characterized for operation from −40 °C to 85 °C, and the C suffix devices are characterized for operation from 0 °C to 70 °C.

AVAILABLE OPTIONS

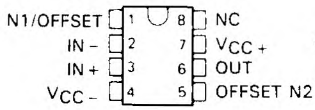
T_A	V_{IO} MAX AT 25 °C	PACKAGE							
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (W)
0 °C to 70 °C	10 mV	TL070CD			TL[illegible]G			TL070CP	
	6 mV	TL070ACD			TL070ACJG			TL070ACP	
	10 mV	TL071CD			TL071CJG			TL071CP	
	6 mV	TL071ACD			TL071ACJG			TL071ACP	
	3 mV	TL071BCD			TL071BCJG			TL071BCP	
	10 mV	TL072CD			TL072CJG			TL072CP	
	6 mV	TL072ACD			TL072ACJG			TL072ACP	
	3 mV	TL0[illegible]			TL072BCJG			TL072BCP	
	10 mV	TL0[illegible]		TL074CJ			TL074CN		
	6 mV	TL074ACD		TL074ACJ			TL074ACN		
	3 mV	TL074BCD		TL074BCJ			TL07[illegible]		
	10 mV						TL0[illegible]		
−40 °C to 85 °C	6 mV	TL070ID			TL070IJG			TL070IP	
	6 mV	TL071ID			TL071IJG			TL071IP	
	6 mV	TL072ID			TL072IJG			TL072IP	
	6 mV	TL074ID		TL074IJ			TL074IN		
−55 °C to 125 °C	6 mV		TL071MFK		TL071MJG	TL071ML			
	6 mV		TL072MFK		TL072MJG	TL072ML			
	9 mV		TL074MFK	TL074MJ					TL074MW

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR).

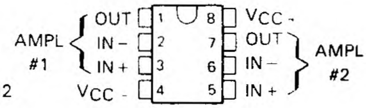
TL070, TL070A
D, JG, OR P PACKAGE
(TOP VIEW)



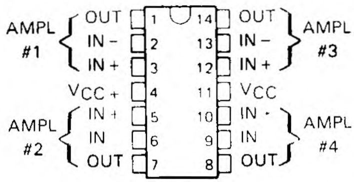
TL071, TL071A, TL071B
D, JG, OR P PACKAGE
(TOP VIEW)



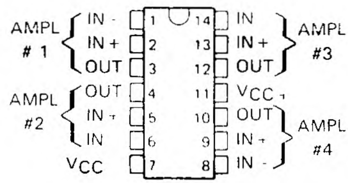
TL072, TL072A, TL072B
D, JG, OR P PACKAGE
(TOP VIEW)



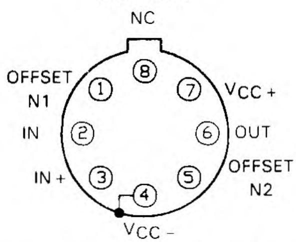
TL074, TL074A, TL074B
D, J, OR N PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



TL075
N PACKAGE
(TOP VIEW)

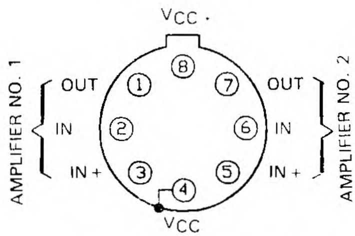


TL071 . . . L PACKAGE
(TOP VIEW)



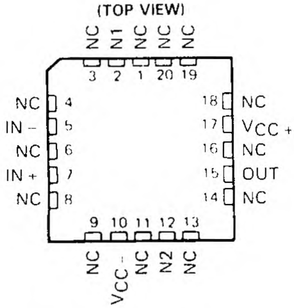
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL072 . . . L PACKAGE
(TOP VIEW)

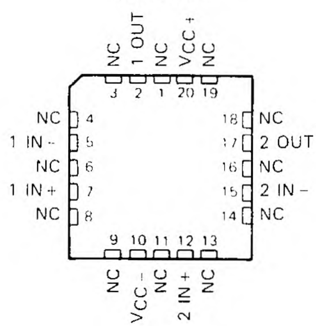


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

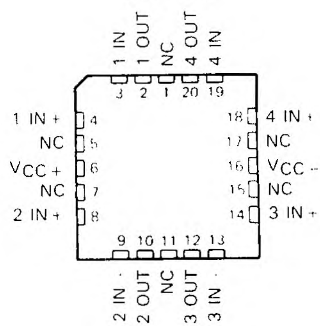
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)

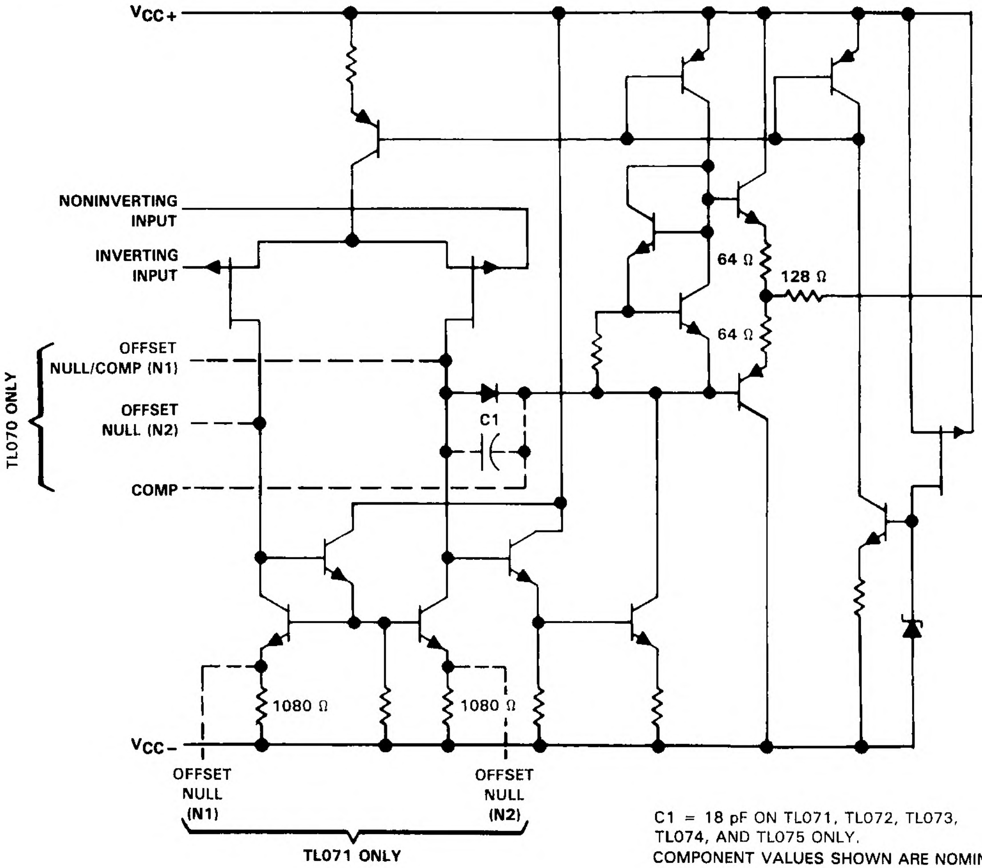


TL074
FK PACKAGE
(TOP VIEW)



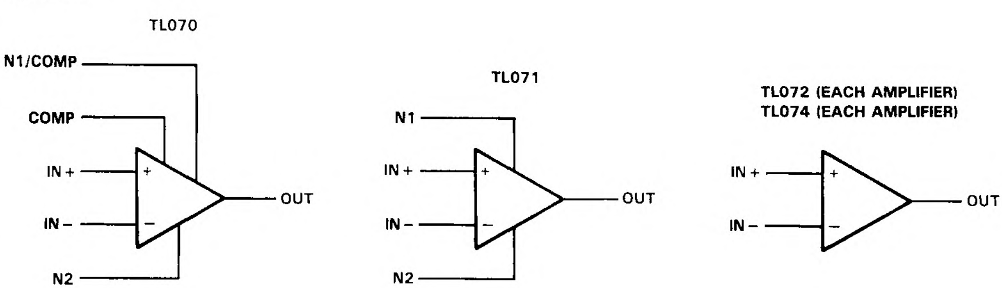
NC – No internal connection.

schematic (each amplifier)



C1 = 18 pF ON TL071, TL072, TL073, TL074, AND TL075 ONLY.
COMPONENT VALUES SHOWN ARE NOMINAL.

symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
[illegible]ly voltage, V_{CC-} (see [illegible] 1)		−18	−18	−18	V
[illegible]rential input voltage (se[illegible] 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to [illegible]	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 1[illegible]	[illegible]65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	[illegible]			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300			°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	[illegible] mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL07_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL07_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
L	680 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω,	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	mV
αV_{IO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	[illegible]		5	100	pA
			T_A = −55°C to 125°C			[illegible]			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		65	[illegible]		65	200	pA
			T_A = −55°C to 125°C			[illegible]			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = −55°C to 125°C	±12			±12			V
		R_L ≥ 2 kΩ		±10			±10			V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	35	200		35	200		V/mV
			T_A = −55°C to 125°C	15			15			V/mV
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

2 Operational Amplifiers

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TL070I TL071I TL072I TL074I			TL070C TL071C TL072C TL074C			TL070AC TL071AC TL072AC TL074AC			TL070BC TL071BC TL072BC TL074BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	10		3	6		2	3	mV
			T_A = full range			8			13			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			18			18			18			18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	100		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		65	200		65	200		65	200		65	200	pA
			T_A = full range			20			7			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	$T_A = 25°C$	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = full range	±12			±12			±12			±12			
		$R_L \geq 2\ k\Omega$	T_A = full range	±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$T_A = 25°C$	50	200		25	200		50	200		50	200		V/mV
		$R_L \geq 2\ k\Omega$	T_A = full range	25			15			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	100		70	100		80	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC\pm}/\Delta V_{IO})$	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	100		70	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL07_I and 0°C to 70°C for TL07_C, TL07_AC, and TL07_BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07_M MIN	TL07_M TYP	TL07_M MAX	ALL OTHERS MIN	ALL OTHERS TYP	ALL OTHERS MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	8	13		8	13		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
	overshoot factor				20			20		%
V_n	Equivalent input noise voltage	R_S = 100 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 100 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, $R_L \geq$ 2 kΩ,	$R_S \leq$ 1 kΩ, f = 1 kHz		0.003			0.003		%

PARAMETER MEASUREMENT INFORMATION

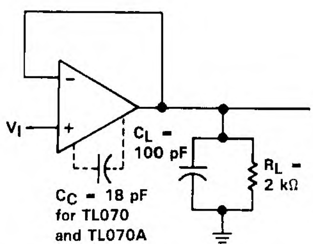


FIGURE 1. UNITY-GAIN AMPLIFIER

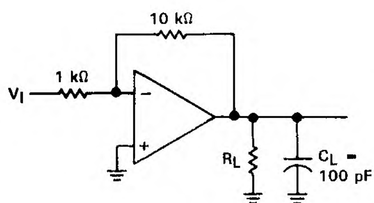


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

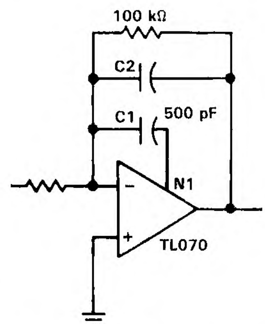


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

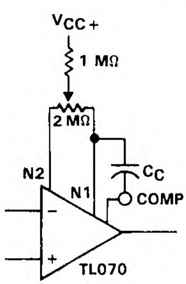


FIGURE 4

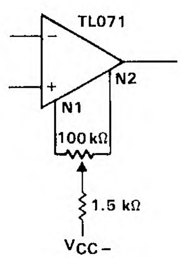


FIGURE 5

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

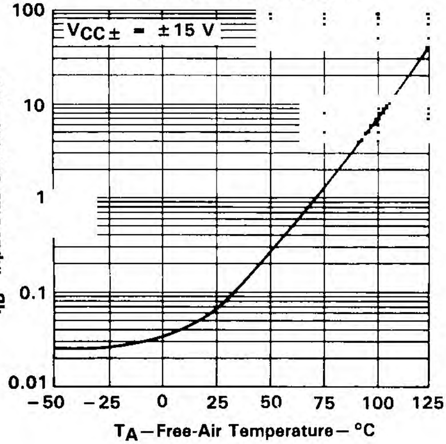


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

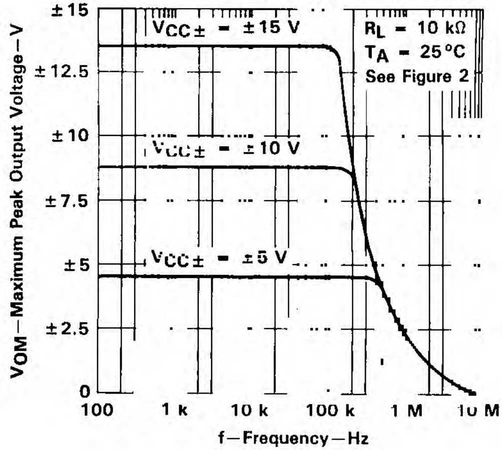


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

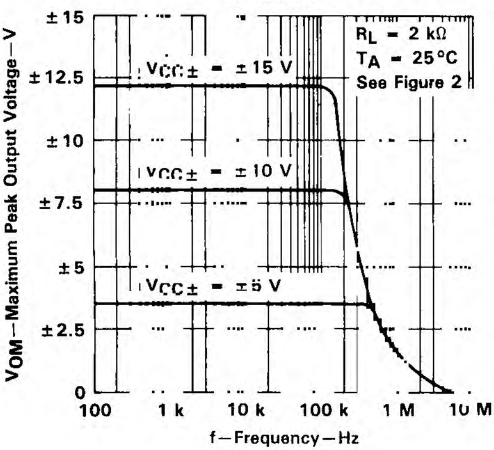


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

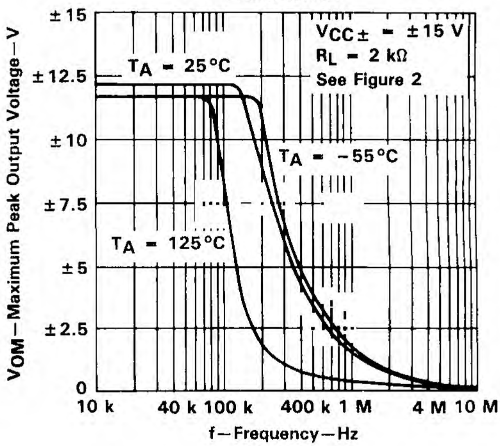


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

2

Operational Amplifiers

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

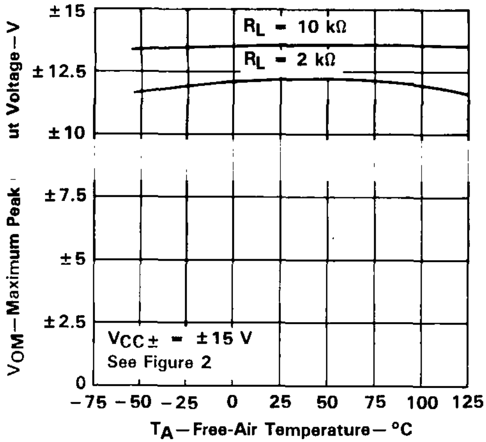

FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

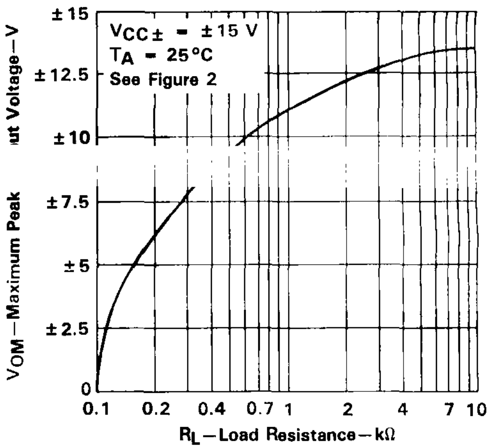

FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

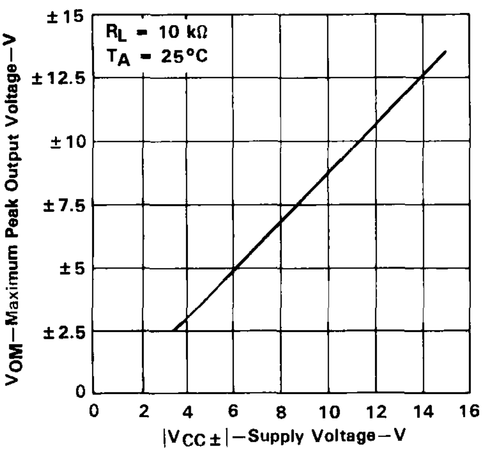

FIGURE 12

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

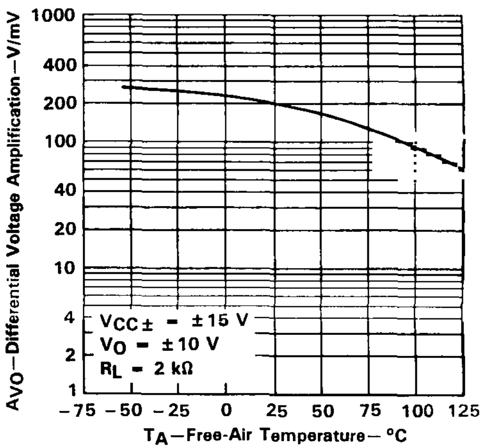

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

Operational Amplifiers

TYPICAL CHARACTERISTICS†

TL070
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

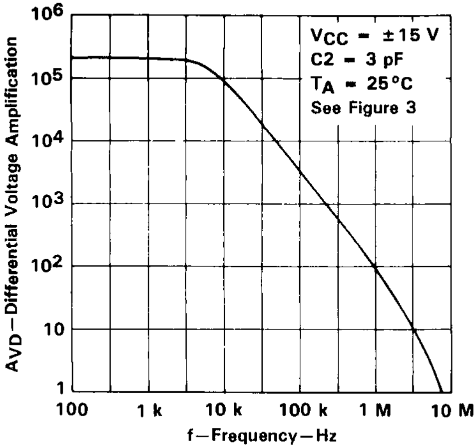

FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

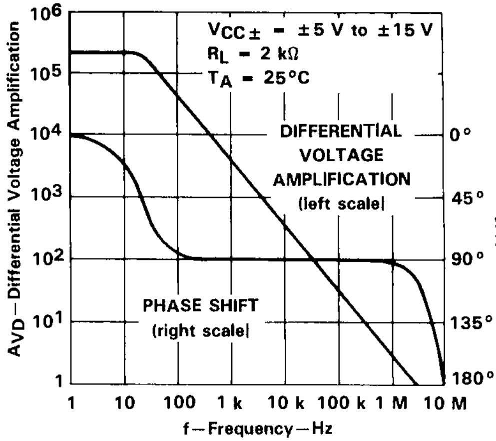

FIGURE 15

NORMALIZED UNITY-GAIN BANDWIDTH
and PHASE SHIFT
vs
FREE-AIR TEMPERATURE

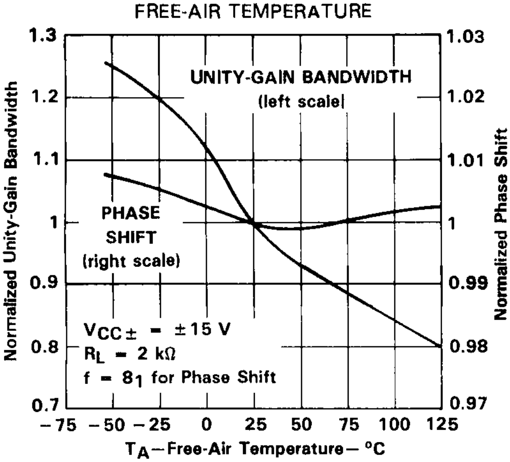

FIGURE 16

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

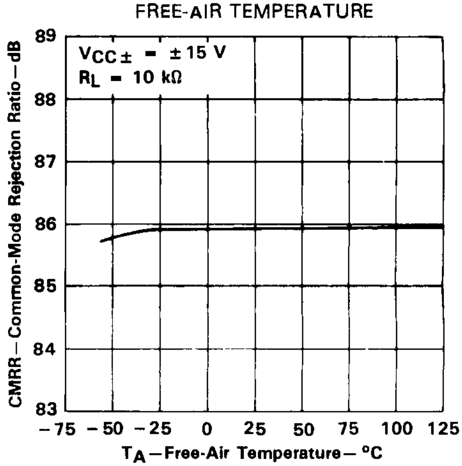

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

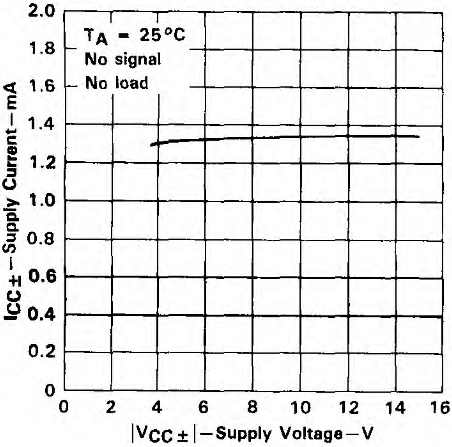

FIGURE 18

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

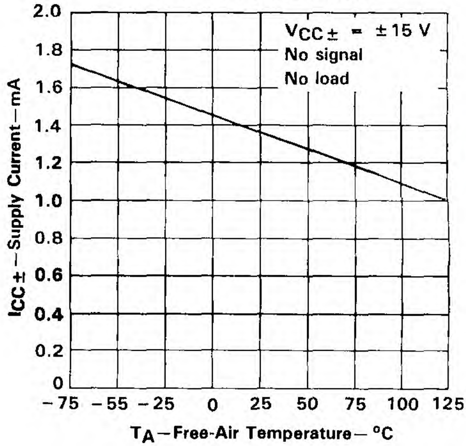

FIGURE 19

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

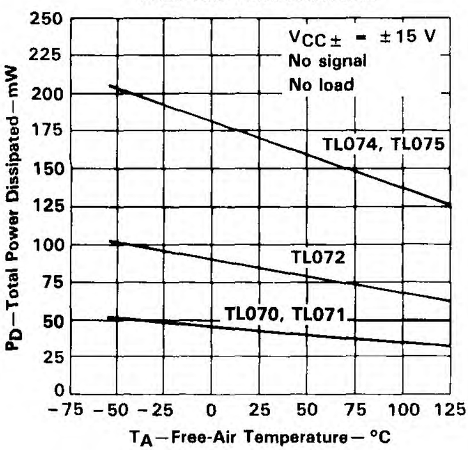

FIGURE 20

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

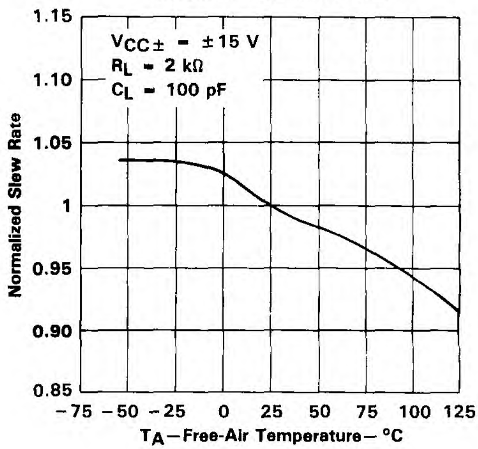

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

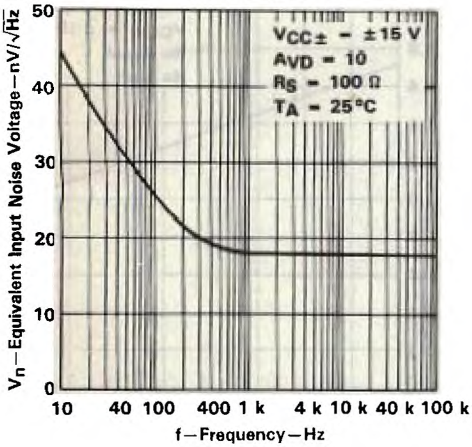

FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

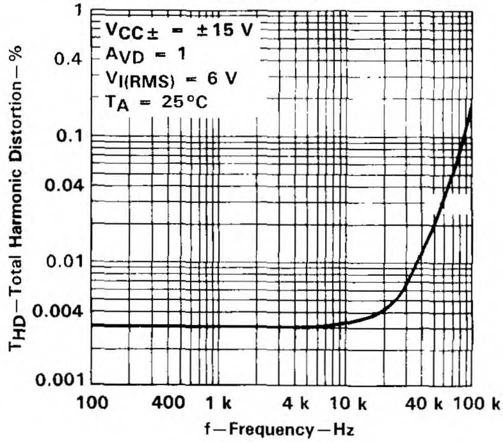

FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

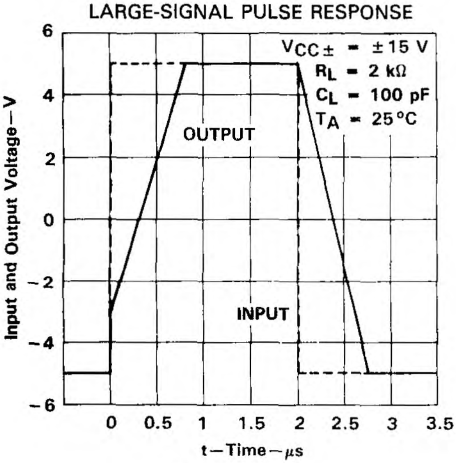

FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

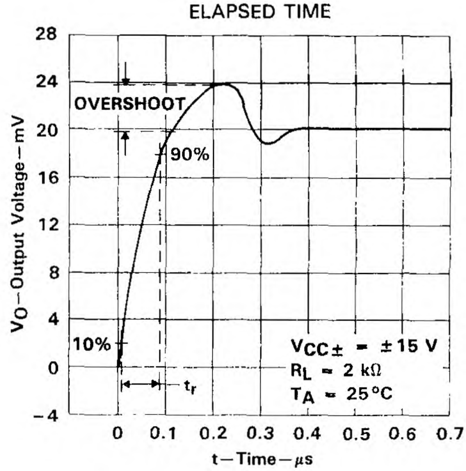

FIGURE 25

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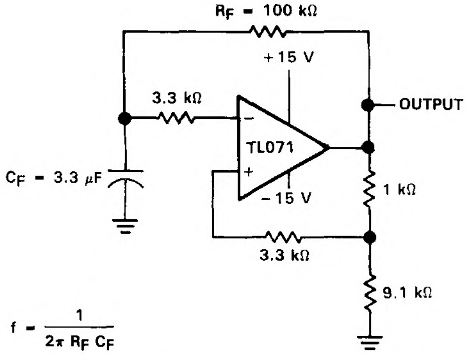
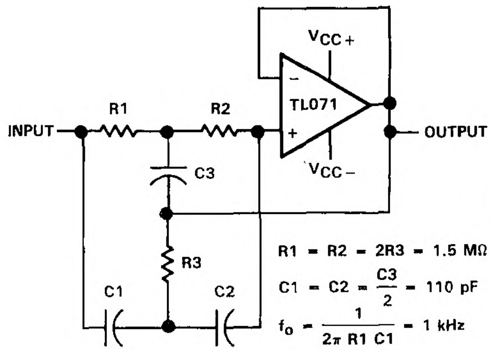
TYPICAL APPLICATION DATA



$$f = \frac{1}{2\pi R_F C_F}$$

FIGURE 26. 0.5-Hz SQUARE-WAVE OSCILLATOR

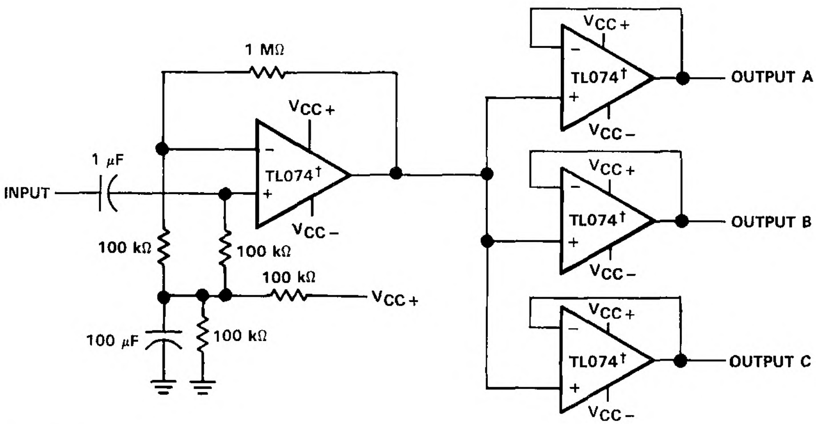


$R1 = R2 = 2R3 = 1.5\ M\Omega$

$C1 = C2 = \frac{C3}{2} = 110\ pF$

$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$

FIGURE 27. HIGH-Q NOTCH FILTER



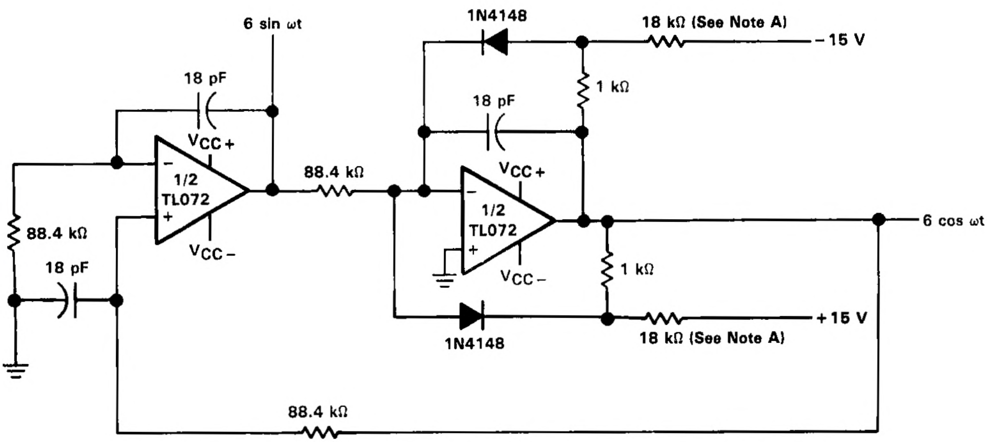
†or TL075

FIGURE 28. AUDIO DISTRIBUTION AMPLIFIER

2

Operational Amplifiers

TYPICAL APPLICATION DATA



Note A: These resistor values may be adjusted for a symmetrical output.

FIGURE 29. 100-kHz QUADRATURE OSCILLATOR

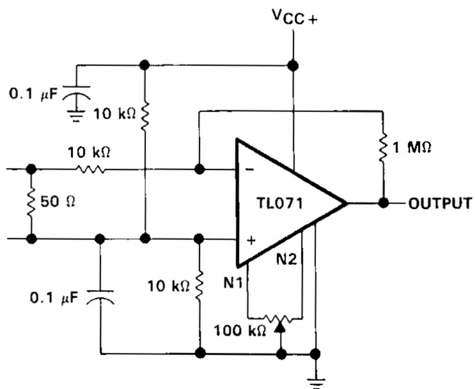


FIGURE 30. AC AMPLIFIER

TYPICAL APPLICATION DATA

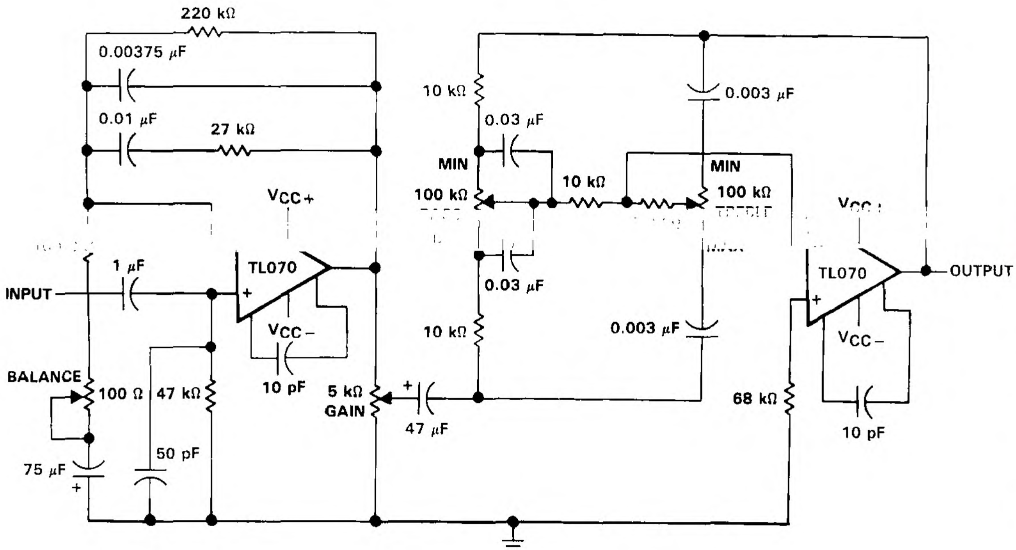


FIGURE 31. IC PREAMPLIFIER

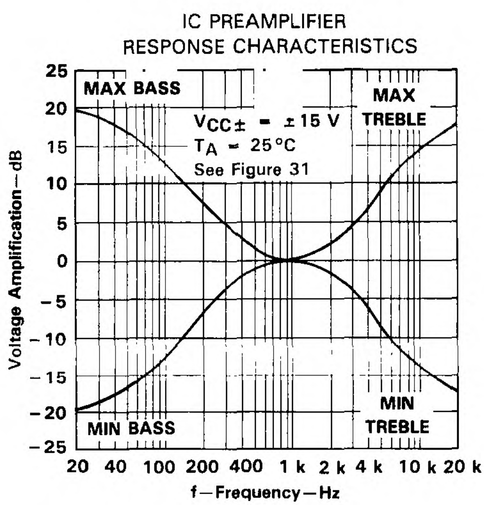


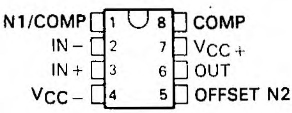
FIGURE 32

TL080 THRU TL085, TL080A THRU TL084A TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

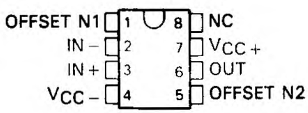
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- **Low-Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation (Except TL080, TL080A)**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

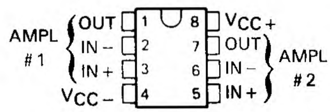
TL080, TL080A
D, JG, OR P PACKAGE
(TOP VIEW)



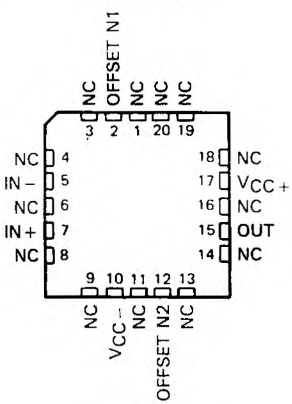
TL081, TL081A, TL081B
D, JG, OR P PACKAGE
(TOP VIEW)



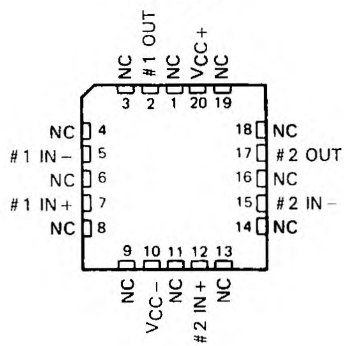
TL082, TL082A, TL082B
D, JG, OR P PACKAGE
(TOP VIEW)



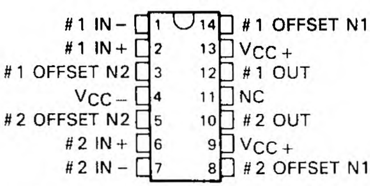
TL081M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



TL082M . . . FK CHIP CHARRIER PACKAGE
(TOP VIEW)

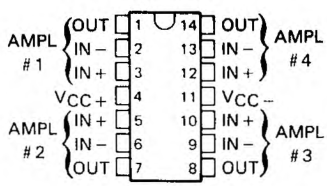


TL083, TL083A
D, J, OR N PACKAGE
(TOP VIEW)



Pins 9 and 13 are internally interconnected

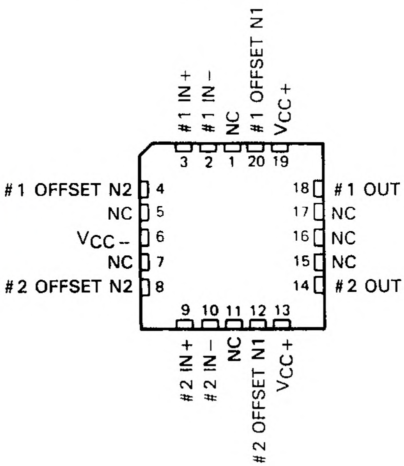
TL084, TL084A, TL084B
D, J, OR N PACKAGE
(TOP VIEW)



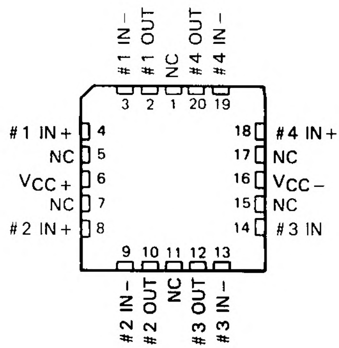
NC—No internal connection

2
Operational Amplifiers

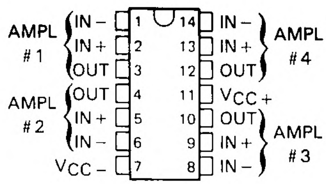
TL083M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



TL084M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



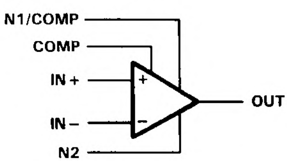
TL085
N PACKAGE
(TOP VIEW)



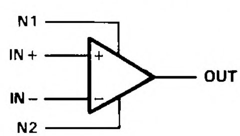
NC—No internal connection

symbols

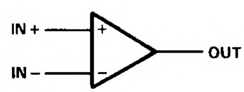
TL080



TL081
TL083 (each amplifier)



TL082 (each amplifier)
TL084 (each amplifier)
TL085 (each amplifier)



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2 Operational Amplifiers

description

The TL08_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08_ family.

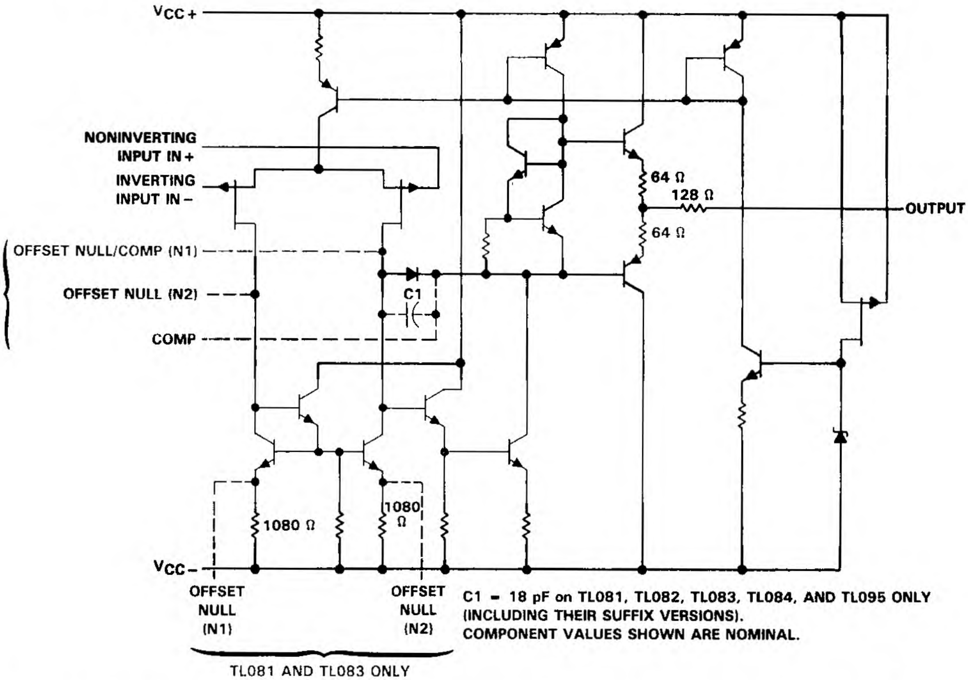
Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −40°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C TO 70°C	15 mV	TL080CD			TL080CJG		TL080CP
	6 mV	TL080ACD			TL080ACJG		TL080ACP
	15 mV	TL081CD			TL081CJG		TL081CP
	6 mV	TL081ACD			TL081ACJG		TL081ACP
	3 mV	TL08[illegible]			TL081BCJG		TL081BCP
	15 mV	TL08[illegible]			TL082CJG		TL082CP
	6 mV	TL082ACD			TL082ACJG		TL082ACP
	3 mV	TL082BCD			TL082BCJG		TL082BCP
	15 mV	TL083CD		TL083CJ		TL083CN	
	6 mV	TL083ACD		TL083ACJ		TL[illegible]ACN	
	15 mV	TL084CD		TL084CJ		T[illegible]N	
	6 mV	TL084ACD		TL084ACJ		TL084ACN	
	3 mV	TL084BCD		TL084BCJ		TL084BCN	
	15 mV					TL085CN	
−40°C TO 85°C	6 mV	TL080ID			TL080IJG		TL080IP
	6 mV	TL081ID			TL081IJG		TL081IP
	6 mV	TL082ID			TL082IJG		TL082IP
	6 mV	TL083ID		TL083IJ		TL083IN	
	6 mV	TL084ID		TL084IJ		TL084IN	
−55°C TO 125°C	6 mV				TL080MJG		
	6 mV		TL081MFK		TL081MJG		
	6 mV		TL082MFK		TL082MJG		
	6 mV		TL083MFK	TL083MJ			
	9 mV		TL084MFK	TL084MJ			

The D package is available taped and reeled. Add "R" suffix to device type (e.g., TL080CDR).

schematic (each amplifier)



C1 = 18 pF on TL081, TL082, TL083, TL084, AND TL095 ONLY (INCLUDING THEIR SUFFIX VERSIONS).
COMPONENT VALUES SHOWN ARE NOMINAL.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see **Note 4**)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	[illegible]			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 Pin)	[illegible] mW	5.8 mW/°C	32°C	464 mW	377 mW	N/A
D (14 Pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL08_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL08_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080M, TL081M, TL082M, TL083M			TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	9	mV
			$T_A = -55°C$ to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $T_A = -55°C$ to 125°C	$R_S = 50\ \Omega$,		18			18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	100	pA
			$T_A = 125°C$			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	200	pA
			$T_A = 125°C$			50			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		V
		$T_A = -55°C$ to 125°C	$R_L \ge 10\ k\Omega$	±12			±12			
			$R_L \ge 2\ k\Omega$	±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $T_A = 25°C$	$R_L \ge 2\ k\Omega$,	25	200		25	200		V/mV
		$V_O = \pm 10$ V, $T_A = -55°C$ to 125°C	$R_L \ge 2\ k\Omega$,	15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ±9 V, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$,	$T_A = 25°C$		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080I TL081I TL082I TL083I TL084I			TL080C TL081C TL082C TL083C TL084C TL085C			TL080AC TL081AC TL082AC TL083AC TL084AC			TL081BC TL082BC TL084BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			18			18			18			18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	400		30	200		30	200	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		T_A = full range	$R_L = \geq 10\ k\Omega$	±12			±12			±12			±12			
			$R_L \geq 2\ k\Omega$	±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, $T_A = 25°C$		50	200		25	200		50	200		50	200		V/mV
		$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, T_A = full range		25			15			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL08_I and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	8	13		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		0.05		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		20%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	$R_S = 100$ Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)} = 10$ V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz		0.003%		

PARAMETER MEASUREMENT INFORMATION

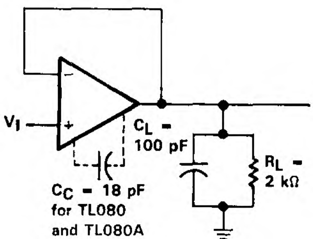


FIGURE 1. UNITY-GAIN AMPLIFIER

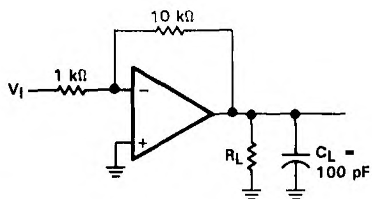


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

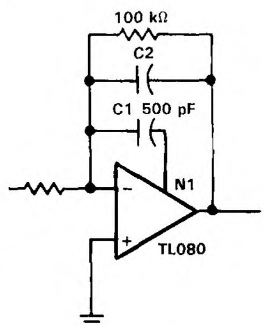


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

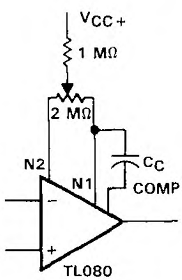


FIGURE 4

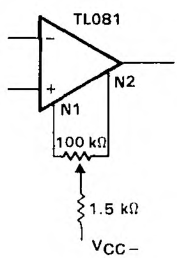


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

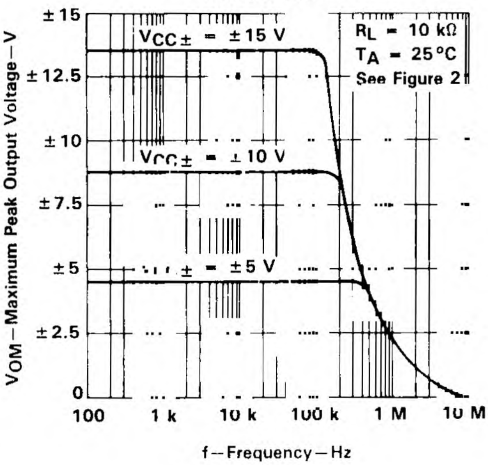


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

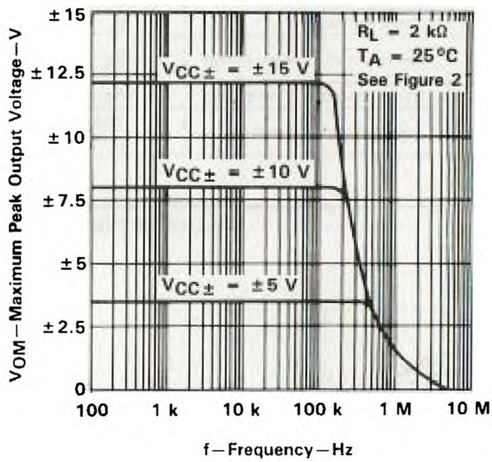


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

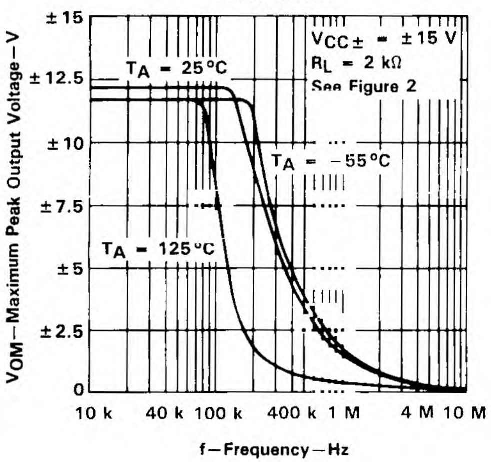


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

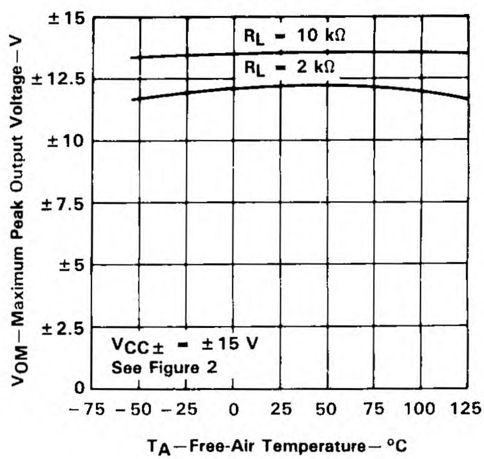


FIGURE 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

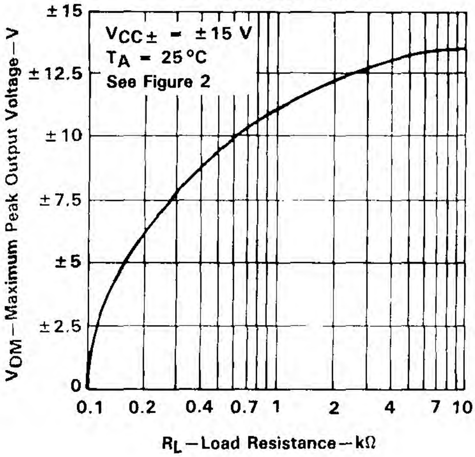


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

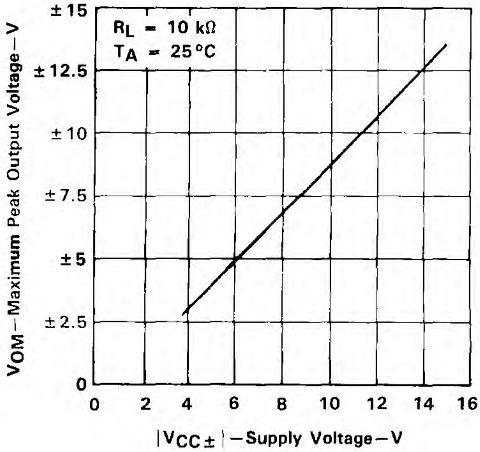


FIGURE 11

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

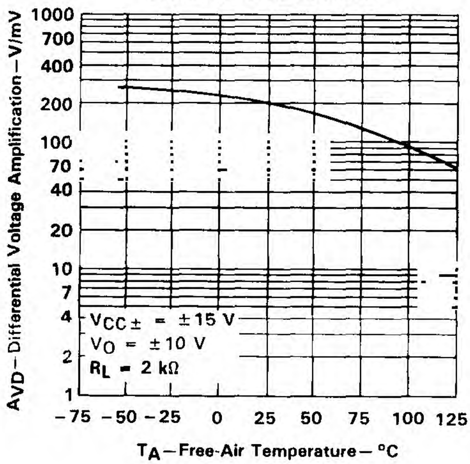


FIGURE 12

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

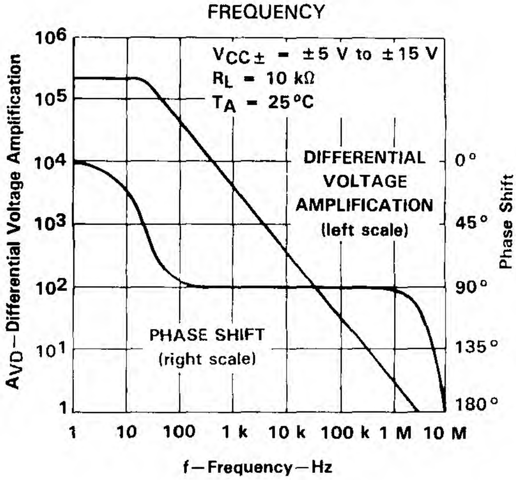


FIGURE 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

2 Operational Amplifiers

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

TL080, TL080A
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

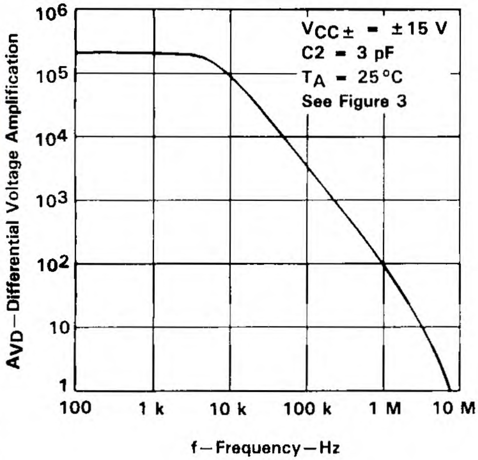


FIGURE 14

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

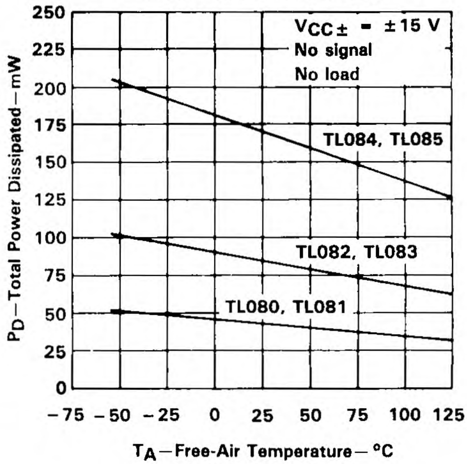


FIGURE 15

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

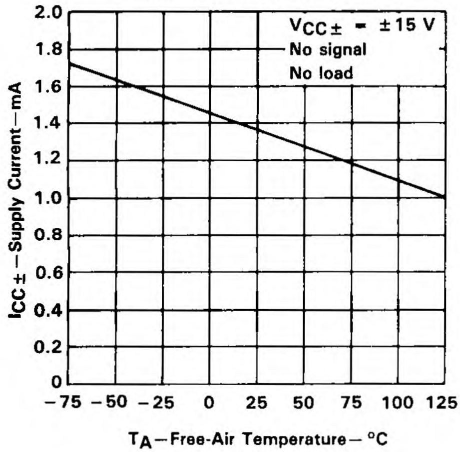


FIGURE 16

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

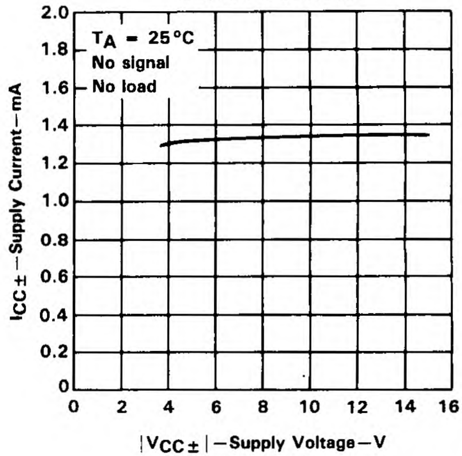


FIGURE 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

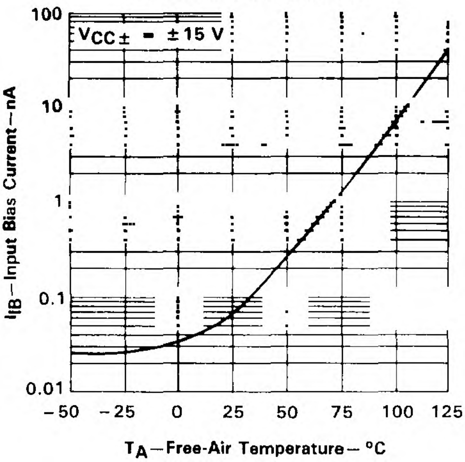

FIGURE 18

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

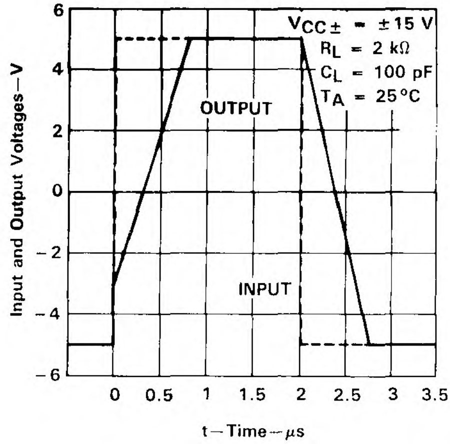

FIGURE 19

OUTPUT VOLTAGE
vs
ELAPSED TIME

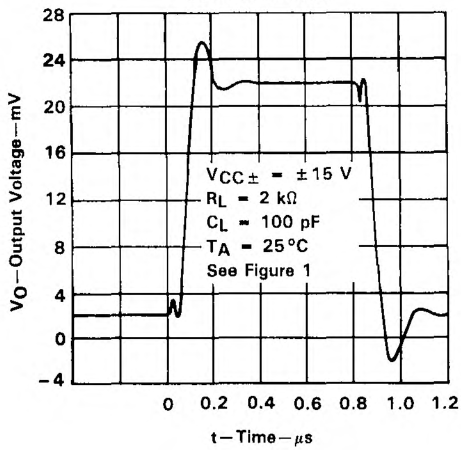

FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

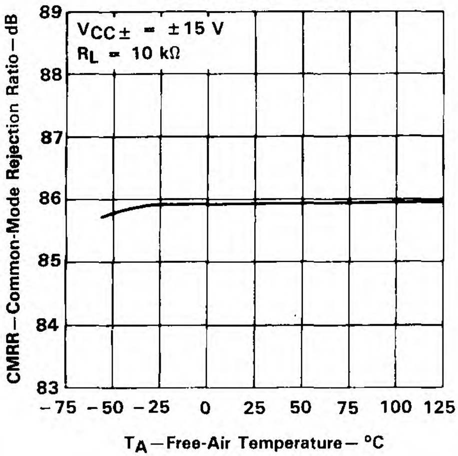

FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

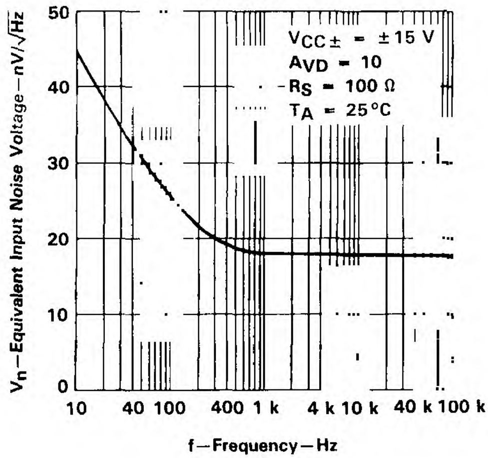

FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

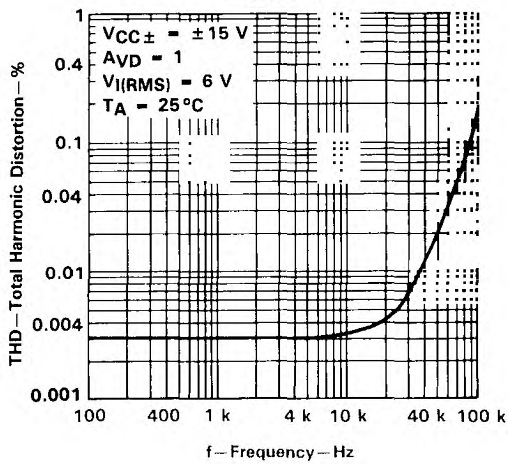

FIGURE 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

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TYPICAL APPLICATION DATA

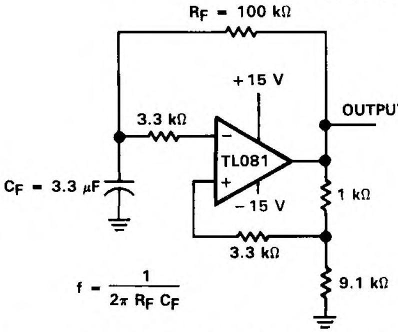


FIGURE 24. 0.5-Hz SQUARE-WAVE OSCILLATOR

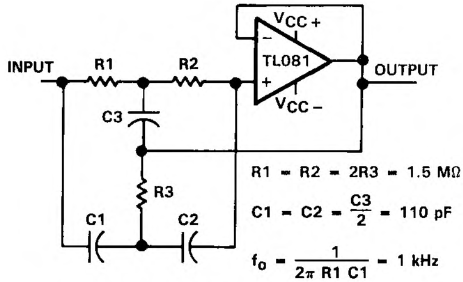
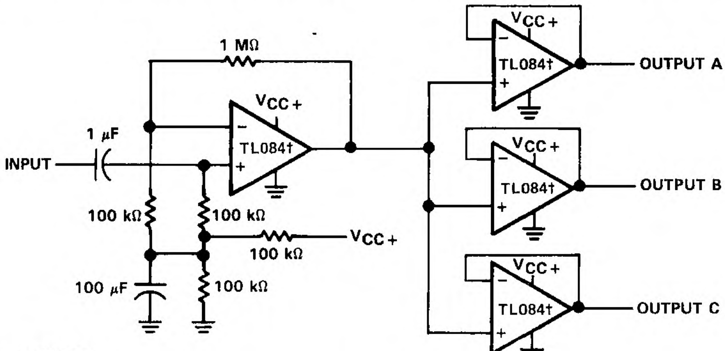
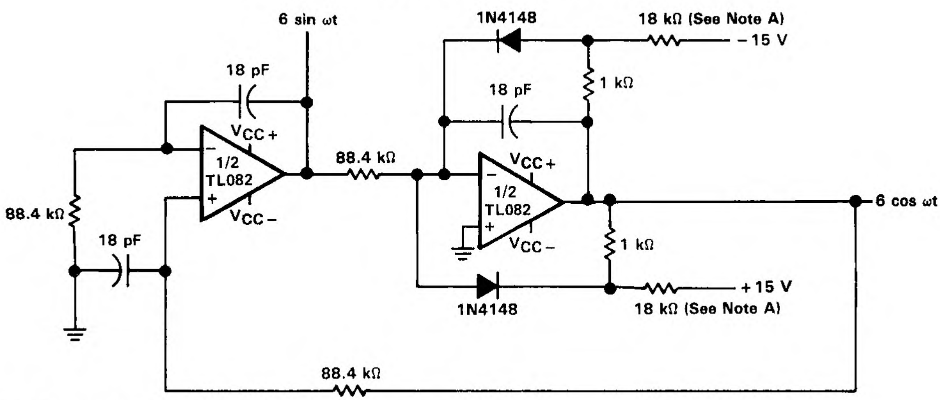


FIGURE 25. HIGH-Q NOTCH FILTER



† or TL085

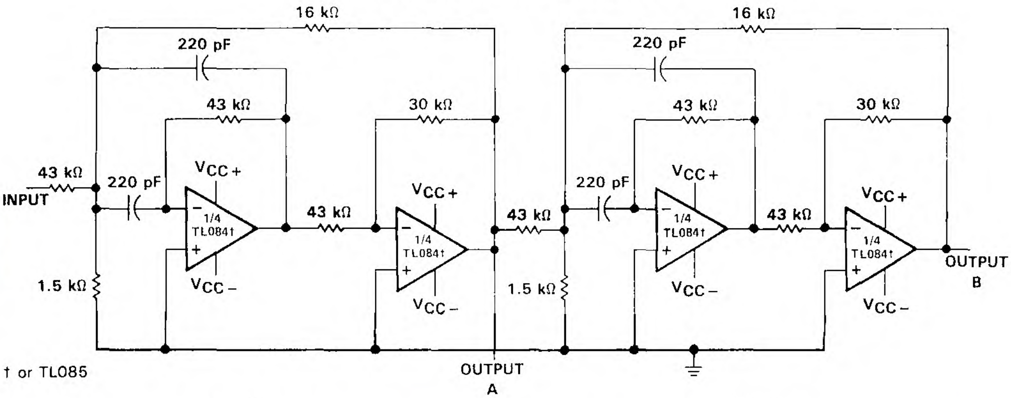
FIGURE 26. AUDIO DISTRIBUTION AMPLIFIER



NOTE A: These resistor values may be adjusted for a symmetrical output.

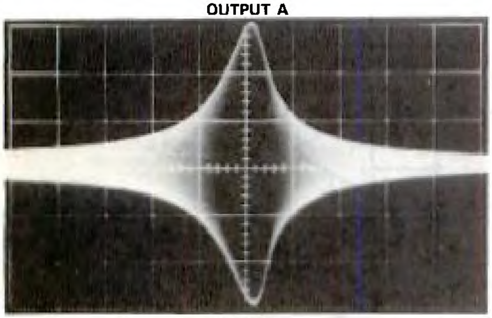
FIGURE 27. 100-kHZ QUADRATURE OSCILLATOR

TYPICAL APPLICATION DATA



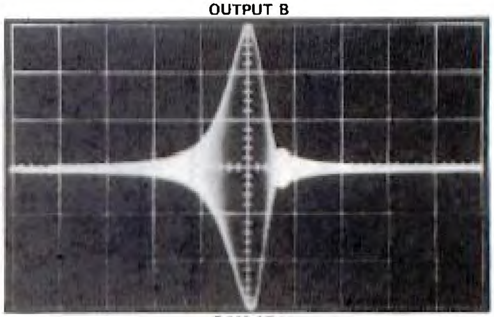
† or TL085

OUTPUT A



2 kHz/div
SECOND-ORDER BANDPASS FILTER
f_o = 100 kHz, Q = 30, GAIN = 4

OUTPUT B



2 kHz/div
CASCADED BANDPASS FILTER
f_o = 100 kHz, Q = 69, GAIN = 16

FIGURE 28. POSITIVE-FEEDBACK BANDPASS FILTER

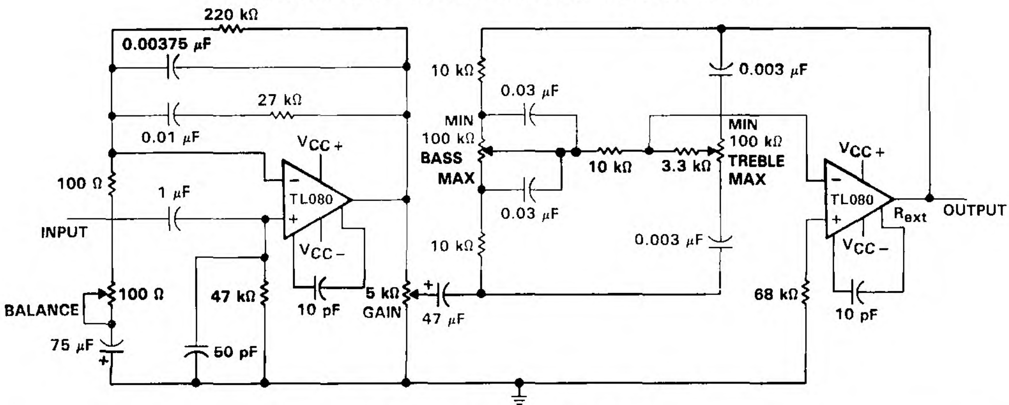


FIGURE 29. IC PREAMPLIFIER

D2484, MARCH 1979—REVISED MARCH 1989

- Low Input Offset Voltage . . . 0.5 mV Max
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 18 V/μs Typ
- Low Total Harmonic Distortion . . . 0.003% Typ

description

These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset currents, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	TYPE	V_{IO} MAX AT 25°C	PACKAGE				
			SMALL OUTLINE (D)	CERAMIC DIP [illegible]	METAL CAN (L)	PLASTIC DIP (P)	FLAT (U)
0°C to 70°C	Single	0.5 mV	TL087CD	[illegible]	TL087CL	TL087CP	
		1 mV	[illegible]	[illegible]	[illegible]	[illegible]	
	Dual	0.5 mV	[illegible]	[illegible]	[illegible]	[illegible]	
		1 mV	[illegible]	[illegible]	[illegible]	[illegible]	
−40°C to 85°C	Single	0.5 mV	[illegible]	[illegible]	[illegible]	[illegible]	
		1 mV	TL088ID	TL088IJG	[illegible]	[illegible]	
	Dual	0.5 mV	TL287ID	TL287IJG	[illegible]	[illegible]	
		1 mV	TL288ID	TL288IJG	TL288IL	TL288IP	
−55°C to 125°C	Single	1 mV		TL088MJG	TL088ML		TL088MU
	Dual	1 mV		TL288MJG	TL288ML		TL288MU

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL087CDR).

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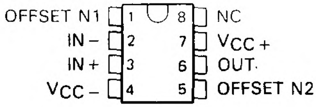
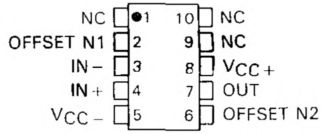
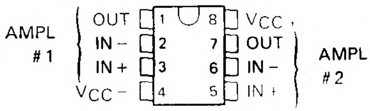
TL087, TL088
D, JG, OR P PACKAGE
(TOP VIEW)



TL088M
U PACKAGE
(TOP VIEW)

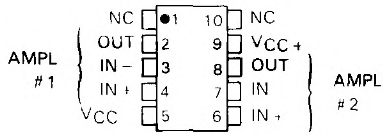


TL287, TL288
D, JG, OR P PACKAGE
(TOP VIEW)

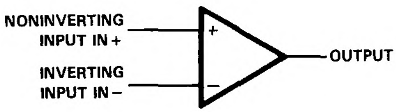


NC—No internal connection

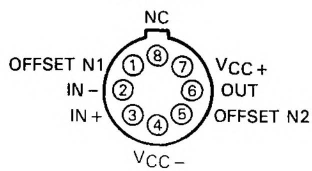
TL288M
U PACKAGE
(TOP VIEW)



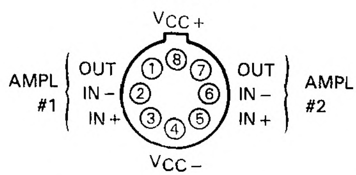
symbol (each amplifier)



TL087, TL088
L PACKAGE
(TOP VIEW)



TL287, TL288
L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Input current, I_I (each input)		±1	±1	±1	mA
Output current, I_O (each output)		±80	[illegible]	±80	mA
Total V_{CC+} terminal current		160	[illegible]	160	mA
Total V_{CC-} terminal current		−160	−160	−160	mA
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, L, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	[illegible]	N/A
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		±5		±15	±5		±15	±5		±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−1		4	−1		4	−1		4	V
	$V_{CC\pm} = \pm15$ V	−11		11	−11		11	−11		11	V
Input voltage, V_I	$V_{CC\pm} = \pm5$ V	−1		4	−1		4	−1		4	V
	$V_{CC\pm} = \pm15$ V	−11		11	−11		11	−11		11	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS†		TL088M TL288M MIN	TYP	MAX	TL087I TL088I TL287I TL288I MIN	TYP	MAX	TL087C TL088C TL287C TL288C MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$, $V_O = 0$, $T_A = 25°C$	TL087, TL287					0.1	0.5		0.1	0.5	mV
			TL088, TL288		0.1	3		0.1	1		0.1	1	
		$R_S = 50\ \Omega$, $V_O = 0$, T_A = full range	TL087, TL287						2			1.5	
			TL088, TL288			6			3			2.5	
αV_{IO}	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	$T_A = 25°C$ to MAX		10			8			8		μV/°C
I_{IO}	Input offset current	$T_A = 25°C$			5			5	100		5	100	pA
		T_A = full range				25			3			2	nA
I_{IB}	Input bias current‡	$T_A = 25°C$			30			30	200		30	200	pA
		T_A = full range				100			20			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			V
V_{OPP}	Maximum-peak-to-peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq 10\ k\Omega$	24			24			24			
			$R_L \geq 2\ k\Omega$	20			20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $T_A = 25°C$	$V_O = \pm 10$ V,	50	105		50	105		50	105		V/mV
		$R_L \geq 2\ k\Omega$, T_A = full range	$V_O = \pm 10$ V,	25			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min,	$V_O = 0$ V, $T_A = 25°C$	80	93		80	93		80	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$R_S = 50\ \Omega$, $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25°C$	$V_O = 0$ V,	80	99		80	99		80	99		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		2.6	2.8		2.6	2.8		2.6	2.8	mA

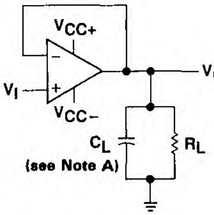
†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TL__88M; −40°C to 85°C for TL__8__I; and 0°C to 70°C for TL__8__C.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics $V_{CC} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL088M, TL288M			TL087I, TL087C TL088I, TL088C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, $A_{VD} = 1$		18		8	18		V/μs
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		55			55		ns
	Overshoot factor	$C_L = 100$ pF, $A_{VD} = 1$		25%			25%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω, f = 1 kHz		15			15		nV/$\sqrt{Hz}$

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

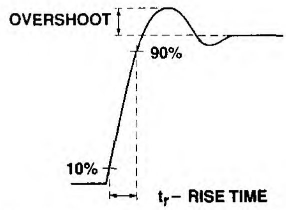


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

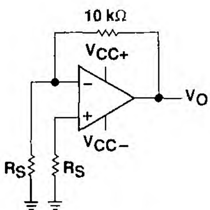
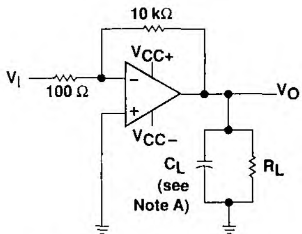


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

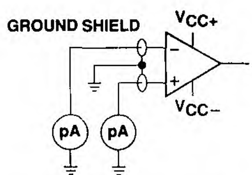


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp bias current level typical of these JFET operational amplifiers, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
αV_{IO}	Temperature coefficient of input offset voltage	Distribution	6, 7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Common-mode input voltage range limits	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	13
		vs Output current	17
		vs Frequency	14, 15, 16
		vs Temperature	18
A_{VD}	Differential voltage amplification	vs R_L	19
		vs Frequency	20
		vs Temperature	21
z_o	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency	22
		vs Temperature	23
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	25
I_{OS}	Short-circuit output current	vs V_{CC}	26
		vs Time	27
		vs Temperature	28
I_{CC}	Supply current	vs V_{CC}	29
		vs Temperature	30
SR	Slew Rate	vs R_L	31
		vs Temperature	32
	Overshoot factor	vs C_L	33
V_n	Equivalent input noise voltage	vs Frequency	34
THD	Total harmonic distortion	vs Frequency	35
B_1	Unity-gain bandwidth	vs V_{CC}	36
		vs Temperature	37
ϕ_m	Phase margin	vs V_{CC}	38
		vs C_L	39
		vs Temperature	40
	Phase shift	vs Frequency	20
	Pulse response	Small-signal	41
		Large-signal	42

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL088
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

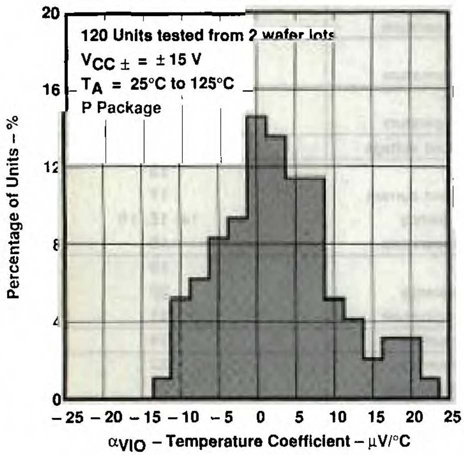


FIGURE 6

DISTRIBUTION OF TL288
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

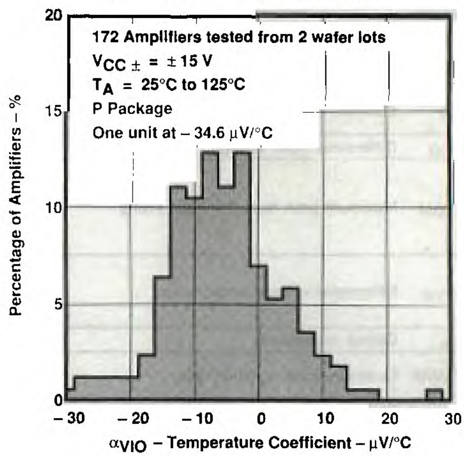


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

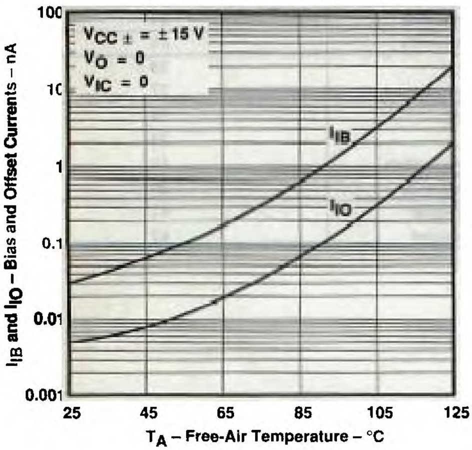


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

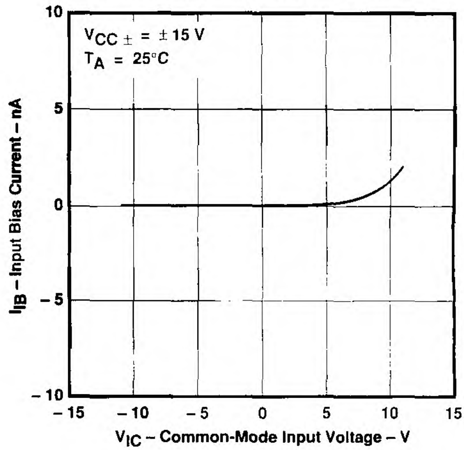


FIGURE 9

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

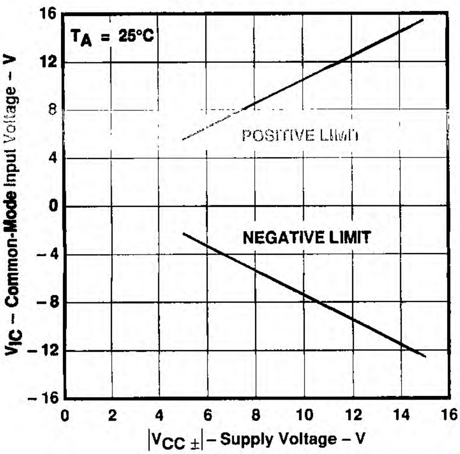

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

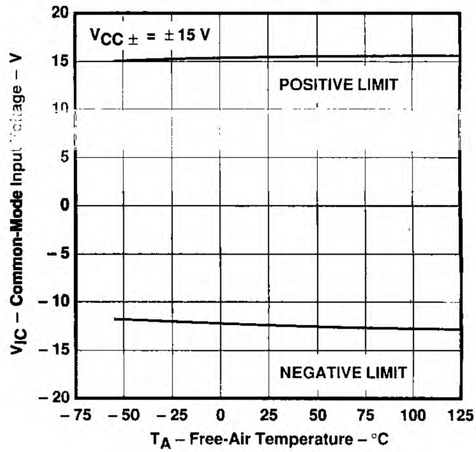

FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

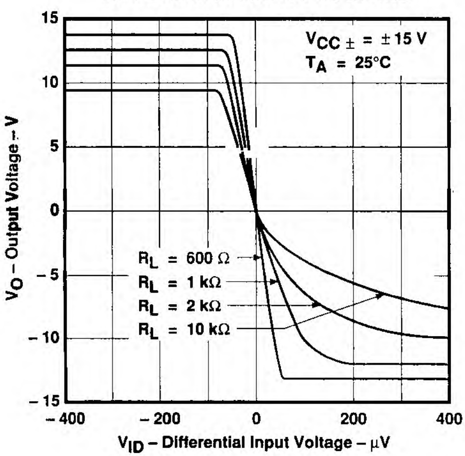

FIGURE 12

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

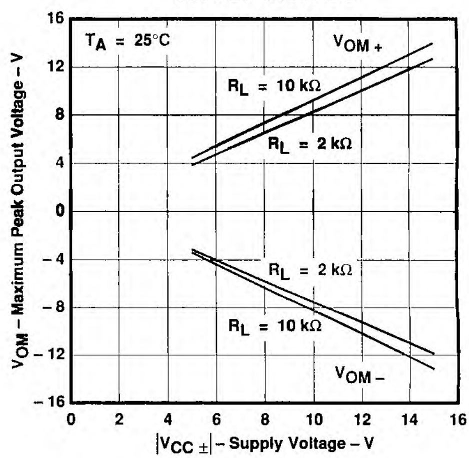

FIGURE 13

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

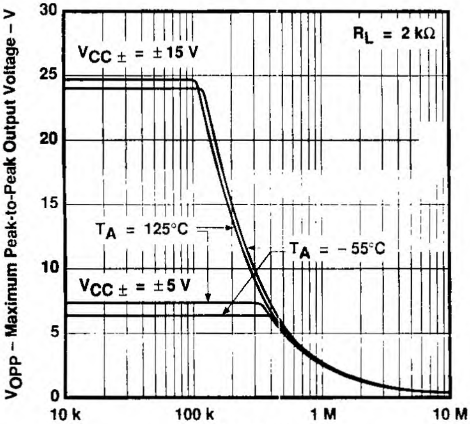

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

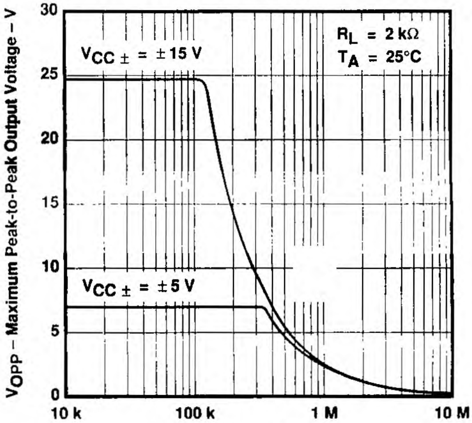

FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

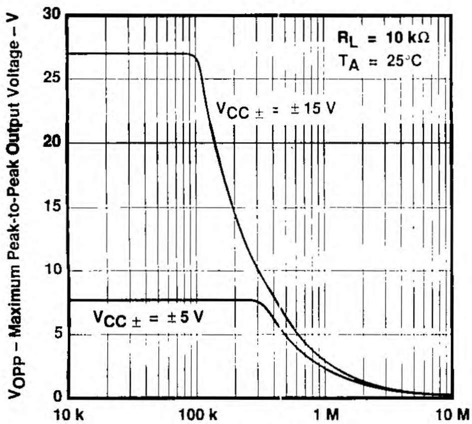

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

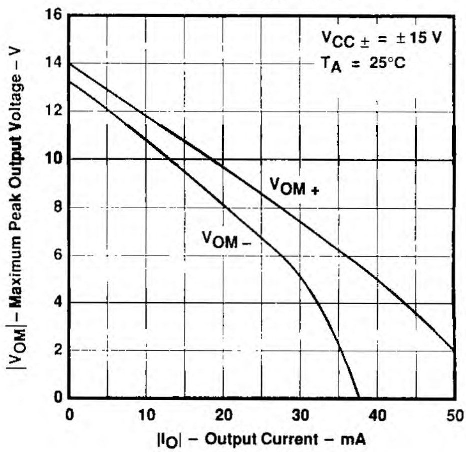

FIGURE 17

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

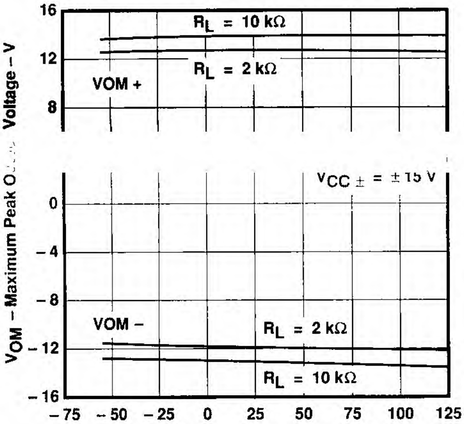

FIGURE 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

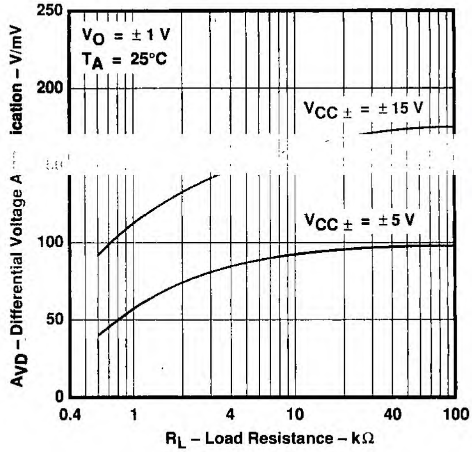

FIGURE 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

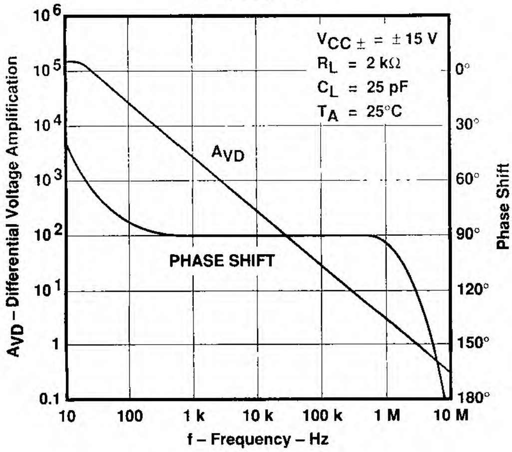

FIGURE 20

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

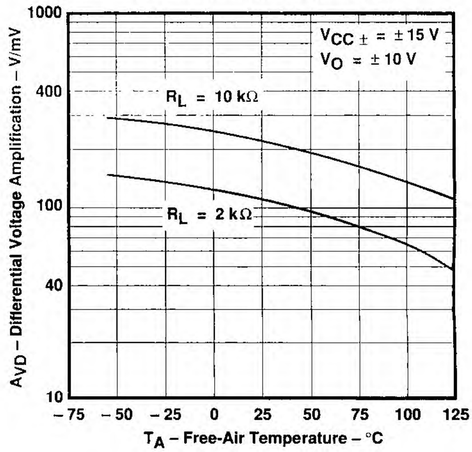

FIGURE 21

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

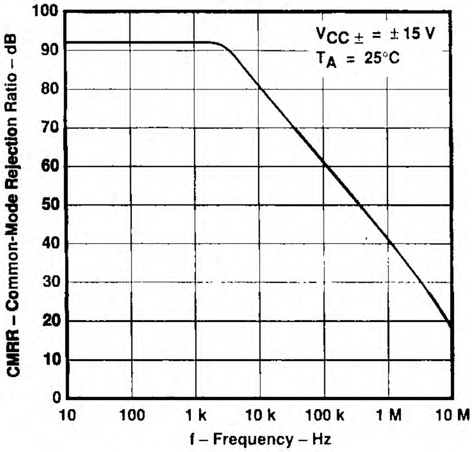

FIGURE 22

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

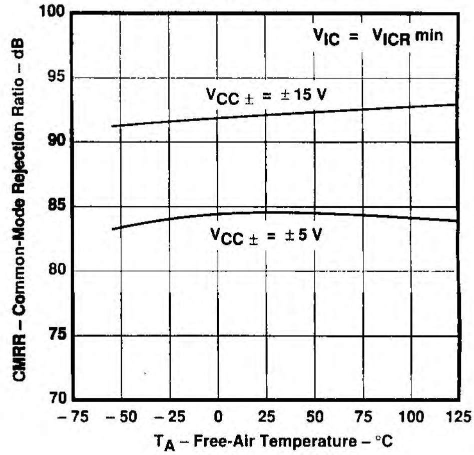

FIGURE 23

OUTPUT IMPEDANCE
vs
FREQUENCY

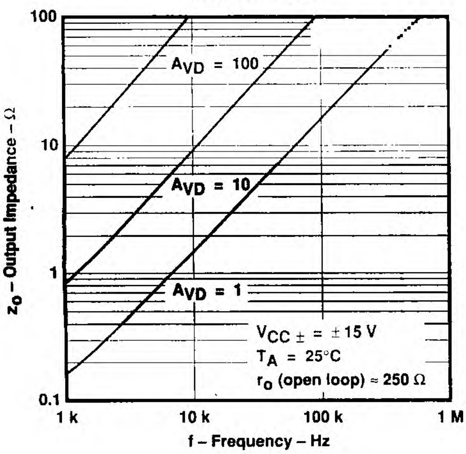

FIGURE 24

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

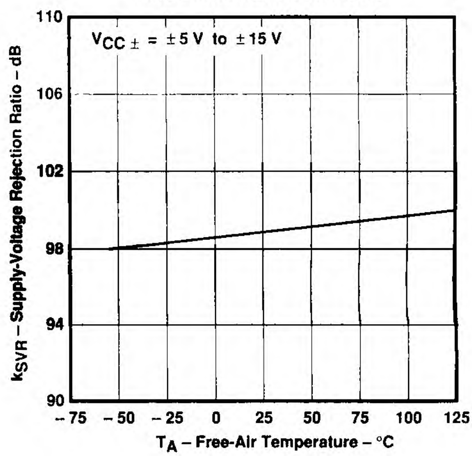

FIGURE 25

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

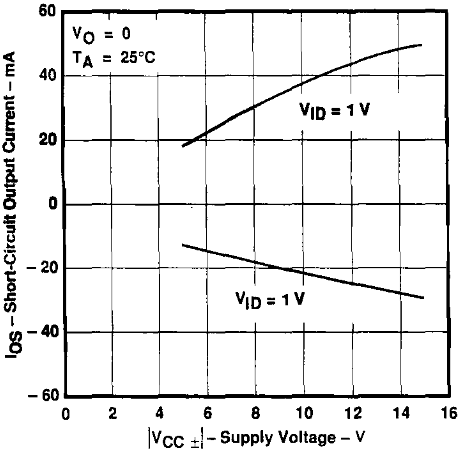

FIGURE 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

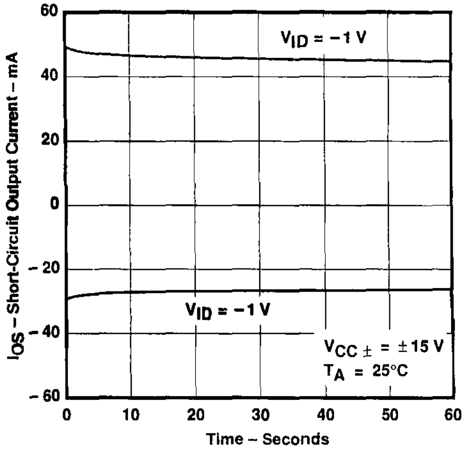

FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

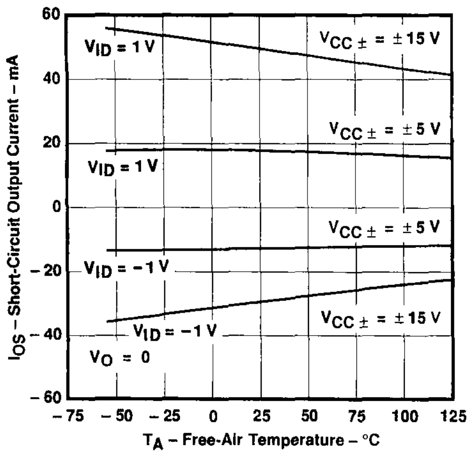

FIGURE 28

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

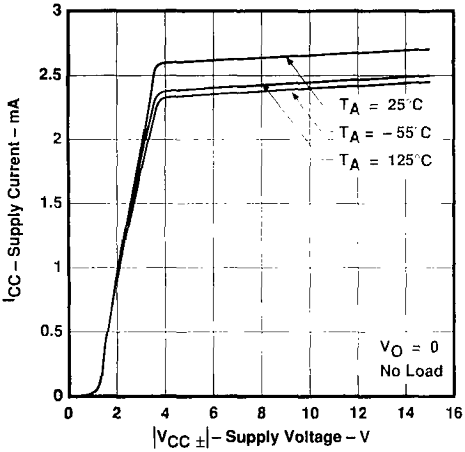

FIGURE 29

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

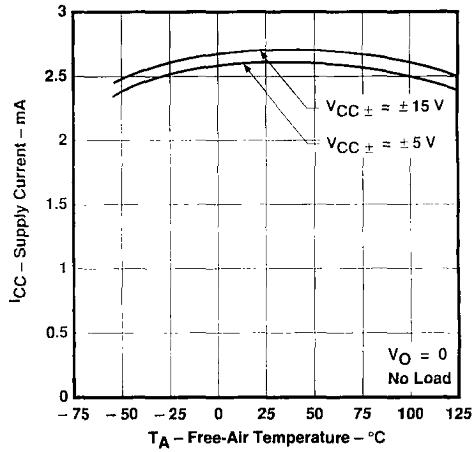

FIGURE 30

SLEW RATE
vs
LOAD RESISTANCE

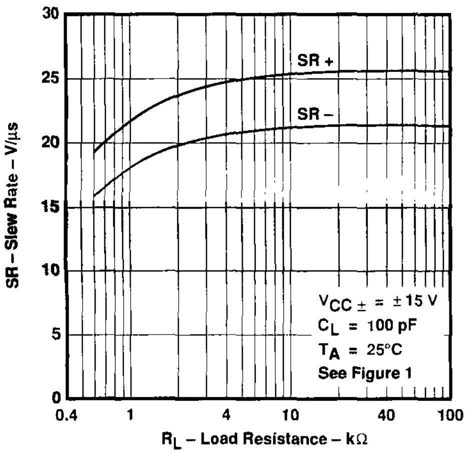

FIGURE 31

SLEW RATE
vs
FREE-AIR TEMPERATURE

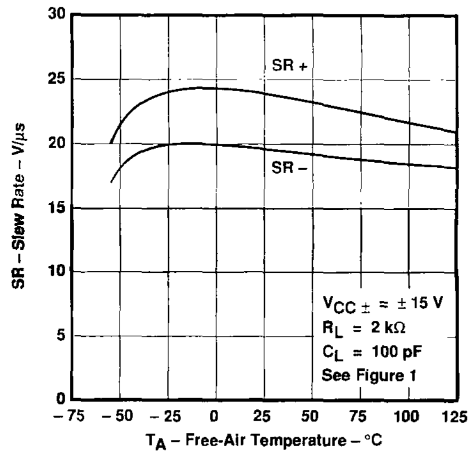

FIGURE 32

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

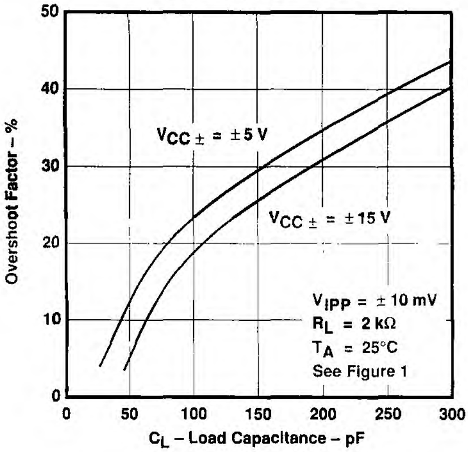

FIGURE 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

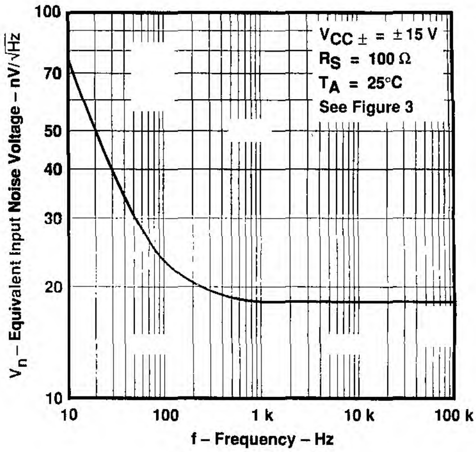

FIGURE 34

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

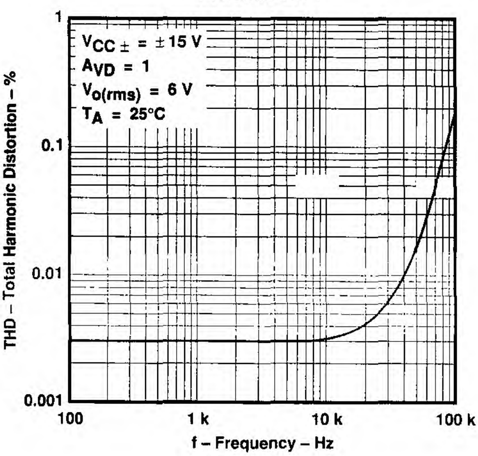

FIGURE 35

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

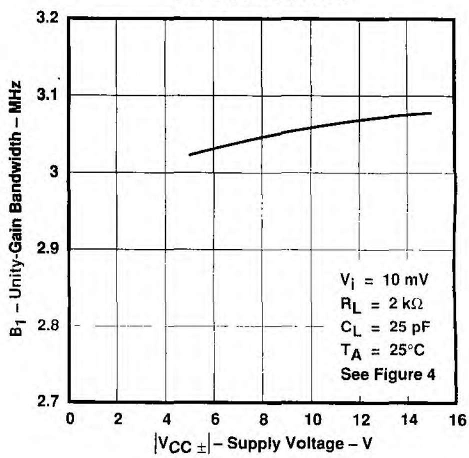

FIGURE 36

2
Operational Amplifiers

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

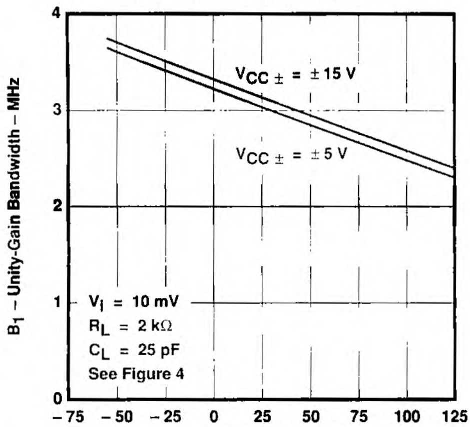

FIGURE 37

PHASE MARGIN
vs
SUPPLY VOLTAGE

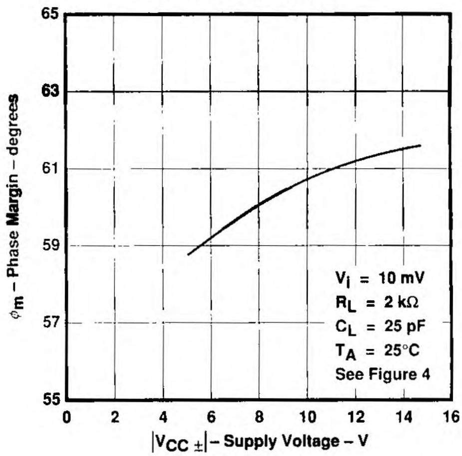

FIGURE 38

PHASE MARGIN
vs
LOAD CAPACITANCE

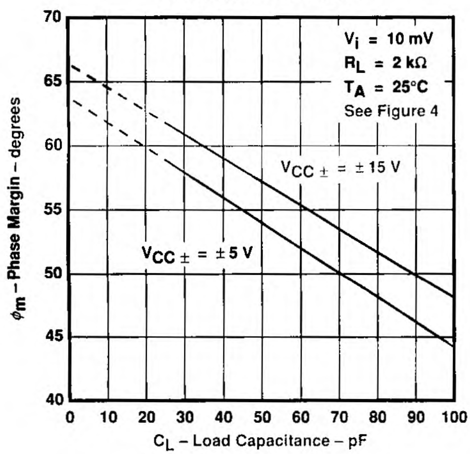

FIGURE 39

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

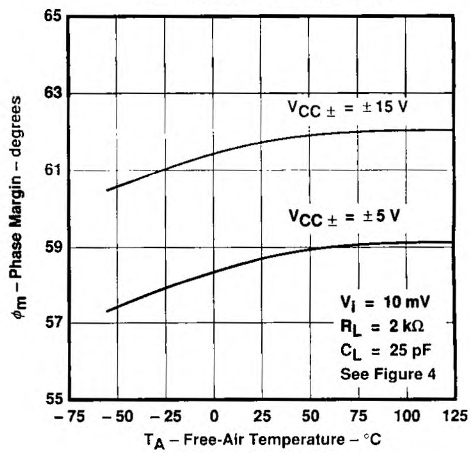

FIGURE 40

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

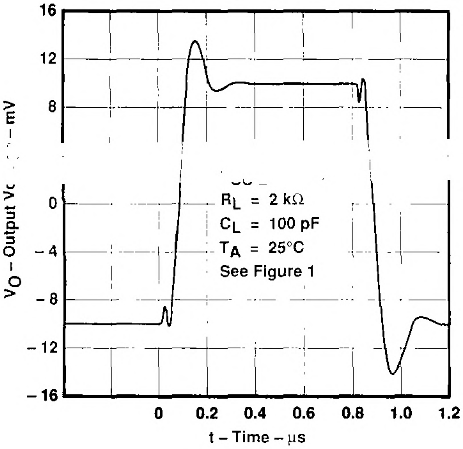


FIGURE 41

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

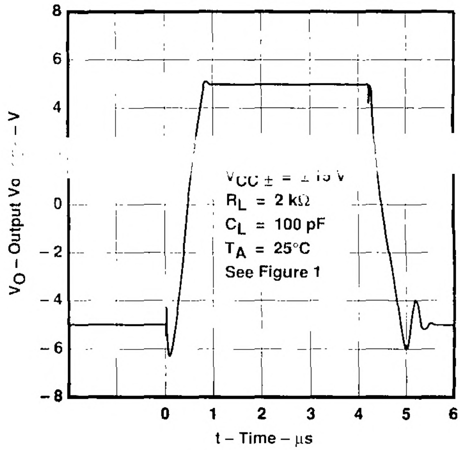
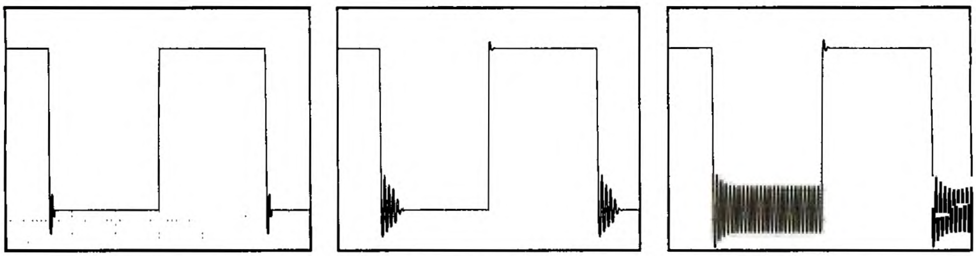


FIGURE 42

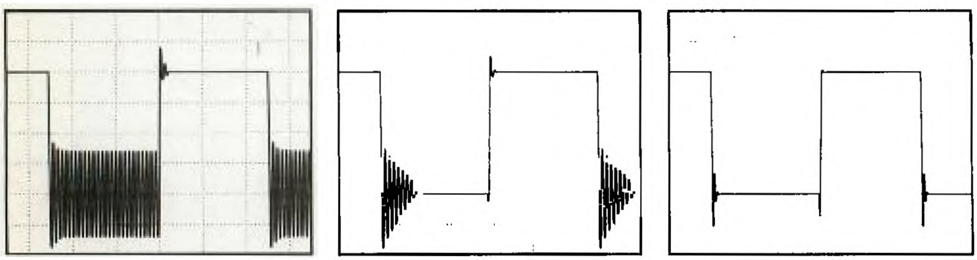
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics are specified with 100-pF load capacitance. These amplifiers will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 43).

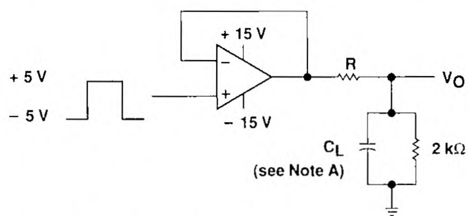


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 43. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

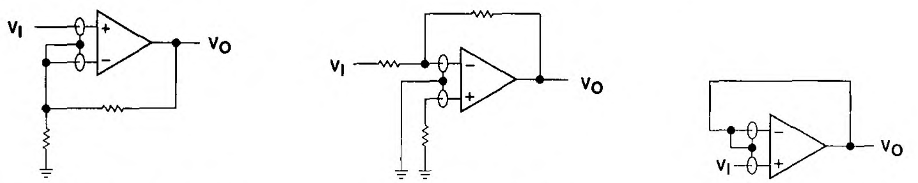
FIGURE 44. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

These amplifiers are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, these amplifiers are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 45). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 45. USE OF GUARD RINGS

noise performance

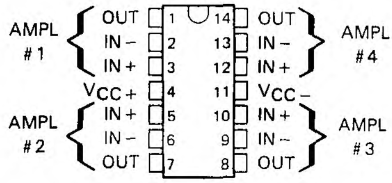
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of these amplifiers result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TL136C
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

D2604, NOVEMBER 1981 – MAY 1988

- Continuous-Short Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers

N PACKAGE
(TOP VIEW)



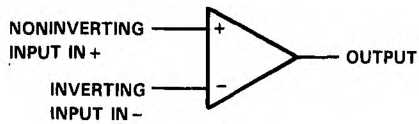
description

The TL136C is a quad high-performance operational amplifier with each amplifier electrically similar to the uA741 except that offset null capability is not provided.

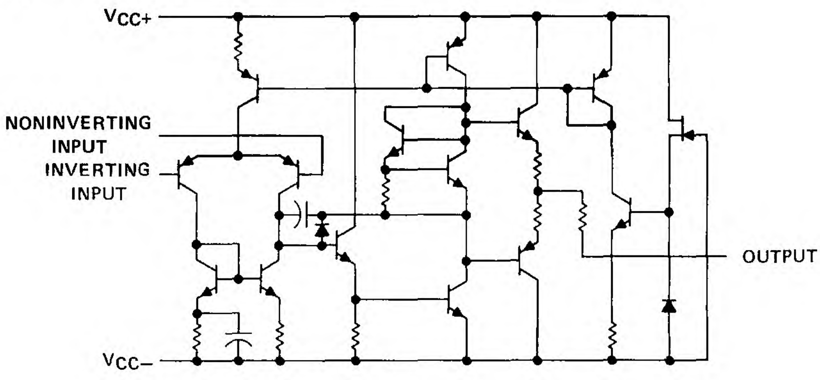
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The TL136C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	18 V
Supply voltage V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (any input, see Notes 1 and 3)	±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
N	800 mW	9.2 mW/°C	736 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω	25°C		0.5	6	mV
				0°C to 70°C			7.5	
I_{IO}	Input offset current	V_O = 0		25°C		5	200	nA
				0°C to 70°C			300	
I_{IB}	Input bias current	V_O = 0		25°C		40	500	nA
				0°C to 70°C			800	
V_{ICR}	Common-mode input voltage range			25°C	±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ		25°C	24	28		V
		R_L = 2 kΩ		25°C	20	26		
		R_L ≥ 2 kΩ		0°C to 70°C	20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ,	V_O = ±10 V	25°C	20	300		V/mV
				0°C to 70°C	15			
B_1	Unity-gain bandwidth			25°C		3		MHz
r_i	Input resistance			25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio	V_C = V_{ICR} min, R_S = 50 Ω		25°C	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±9 V to ± 15 V, R_S = 50 Ω		25°C		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, f = 1 kHz,	R_S = 100 Ω, BW = 1 Hz	25°C		7.5		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	No load,	V_O = 0 V	25°C		5	11.3	mA
				0°C		6	13.7	
				70°C		4.5	11.3	
P_D	Total power dissipation (All four amplifiers)	No load,	V_O = 0 V	25°C		150	340	mW
				0°C		180	400	
				70°C		135	300	
$V_{o1}V_{o2}$	Crosstalk attenuation Open loop A_{VD}	R_S = 1 kΩ,	f = 10 kHz	25°C		105		dB
				25°C		105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, C_L = 100 pF	R_L = 2 kΩ,		0.13		µs
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF	R_L = 2 kΩ,		2.0		V/µs

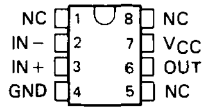
2

Operational Amplifiers

D2343, APRIL 1977 – REVISED OCTOBER 1988

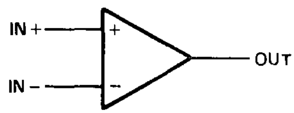
- Wide Range of Supply Voltages Single Supply . . 3 V to 30 V or Dual Supplies
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Low Input Bias and Offset Parameters Input
  Input Offset Voltage . . . 2 mV Typ
  Input Offset Current . . . 3 nA Typ (TL321I)
  Input Bias Current . . . 45 nA Typ
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V
- Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

TL321I, TL321C . . . D, JG OR P PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



description

The TL321 is a high-gain, frequency-compensated operational amplifier that was designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible as long as the difference between the two supplies is 3 V to 30 V and pin 7 is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the TL321 can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

The TL321I is characterized for operation from −25°C to 85°C. The TL321C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	7 mV	TL321CD	TL321CJG	TL321CP
−25°C to 85°C	5 mV	TL321ID	TL321IJG	TL321IP

The D packages are available taped and reeled. Add the suffix R to the device type. (e.g., TL321CDR)

TEXAS INSTRUMENTS

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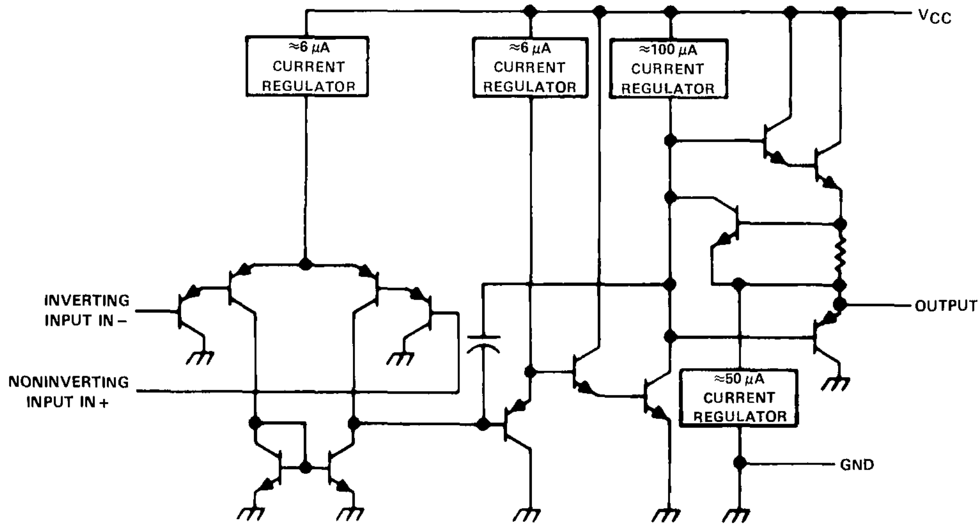
schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 32 V
Differential input voltage (see Note 2) . . . . ±32 V
Input voltage range (either input) . . . . −0.3 V to 32 V
Duration of output short-circuit to ground at (or below) 25°C free-air temperature
(V_{CC} ≤ 15 V) (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range: TL321I . . . . −25°C to 85°C
TL321C . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	680 mW	5 8 mW/°C	33°C	464 mW	377 mW
JG	680 mW	6 6 mW/°C	47°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

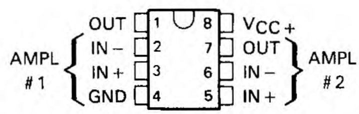
PARAMETER		TEST CONDITIONS†		TL321I MIN	TL321I TYP	TL321I MAX	TL321C MIN	TL321C TYP	TL321C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_S = 50 kΩ	25°C		2	5		2	7	mV
			Full range			7			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	30		5	50	nA
			Full range			100			150	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−45	−150		−45	−250	nA
			Full range			−300			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
		V_{CC} = 30 V, R_L ≥ 10 kΩ	Full range	27	28		27	28		
		R_L ≥ 2 kΩ	25°C	3.5			3.5			
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, R_S = 50 Ω	25°C	70	85		65	85		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V, R_S = 50 Ω	25°C	65	100		65	100		dB
I_O	Output current — Source	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−25	−40		−20	−40		mA
			Full range	−10	−20		−10	−20		
	Output current — Sink	V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5	8		5	8		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		μA
I_{CC}	Supply current	No load, V_O = 15 V, V_{CC} = 30 V	Full range			2			2	mA
		No load, V_O = 2.5 V, V_{CC} = 5 V	Full range		0.4	1			1	

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is −25°C to 85°C for TL321I, and 0°C to 70°C for TL321C.

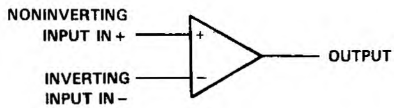
D2567, OCTOBER 1979—REVISED OCTOBER 1988

- Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies
- Class AB Output Stage
- True Differential Input Stage
- Low Input Bias Current
- Internal Frequency Compensation
- Short-Circuit Protection

D, JG, OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TL322I and the TL322C are dual operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC-} 1.5 V. Quiescent supply currents per amplifier are typically less than one-half those of the uA741.

The TL322I is characterized for operation from −40°C to 85°C. The TL322C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

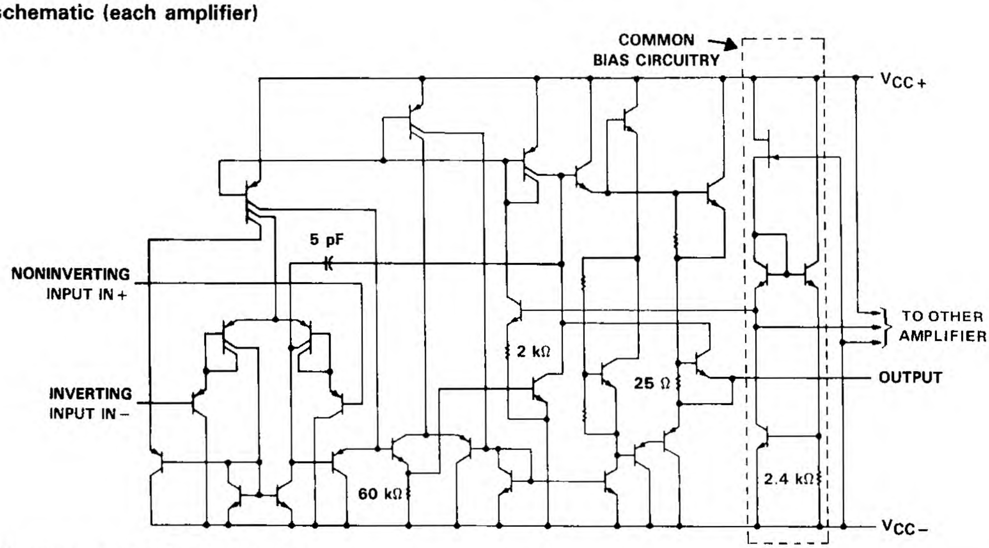
T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	10 mV	TL322CD	TL322CJG	TL322CP
−40°C to 85°C	8 mV	TL322ID	TL322IJG	TL322IP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g. TL322CDR)

2

Operational Amplifiers

schematic (each amplifier)



All component values shown are nominal

TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL322I	TL322C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	V
Differential input voltage (see Note 2)		±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	[illegible] mW	5.8 [illegible]	33°C	464 mW	[illegible] mW
JG	680 mW	6.6 mW/°C	47°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature; $V_{CC\pm}$ = 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL322I MIN	TL322I TYP	TL322I MAX	TL322C MIN	TL322C TYP	TL322C MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	25°C		10			10		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		30	75		30	50	nA
			Full range			250			200	
α_{IIO}	Temperature coefficient of input offset current	V_O = 0	25°C		50			50		pA/°C
I_{IB}	Input bias current	V_O = 0	25°C		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	±12	±12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	±10	±12		±10	±13		
			Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 200 pF	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±2.5 V to ±15 V, R_S = 50 Ω	25°C		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§	V_O = 0	25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	V_O = 0, No load	25°C		1.4	4		1.4	4	mA

†All characteristics are noted under open-loop conditions unless otherwise noted. Full range for T_A is −40°C to 85°C for TL322I, and 0°C to 70°C for TL322C.
‡The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.
§Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL322I			TL322C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω			8		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current				−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	$V_{CC+}-1.7$			$V_{CC+}-1.7$			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±2.5 V to ±15 V			150			150	μV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		1.2	4		1.2	4	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, f = 1 kHz to 20 kHz		120			120		dB

†All characteristics are specified under open-loop conditions.
‡Output will swing essentially to ground.

switching characteristics: V_{CC+} = ±15 V, A_{VD} = 1, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = [illegible] pF, See Figure 1		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		μs
t_f	Fall time			0.35		μs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

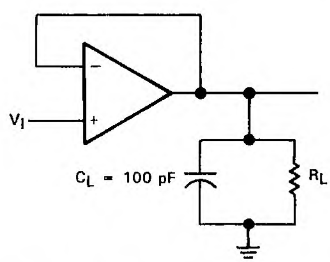

FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

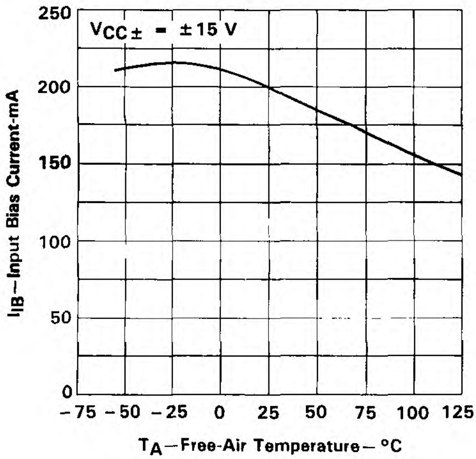

FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

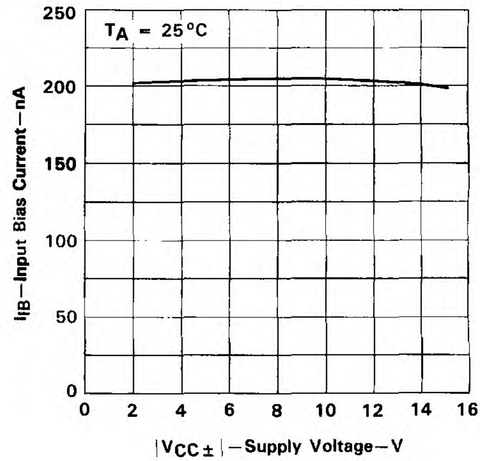

FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

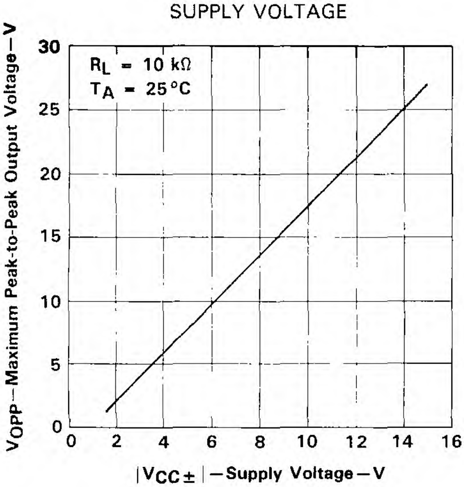

FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

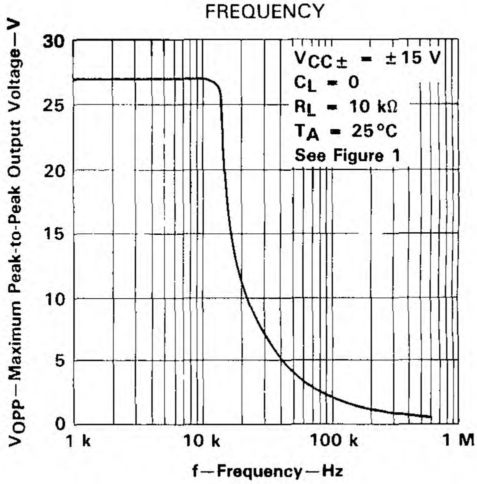

FIGURE 5

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

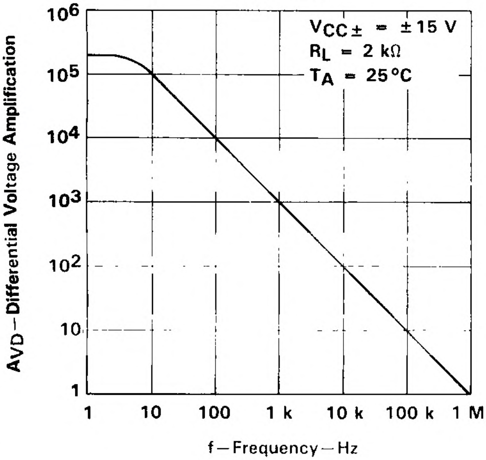

FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

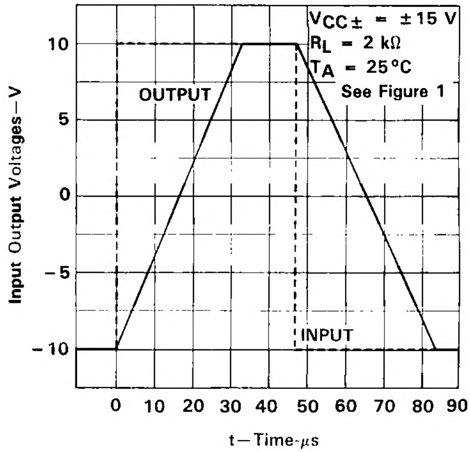

FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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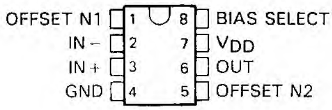
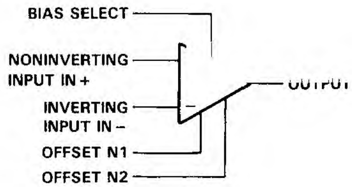
D2751, 1983—REVISED SEPTEMBER 1988

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV √Hz Typ at 1 kHz (High Bias)**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features operation down to a 1.4-V supply and is stable at unity gain.

The TLC251C series is characterized for operation from 0°C to 70°C.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)
0°C	10 mV	[illegible]CD	[illegible]CP	[illegible]CJG
to	5 mV	T[illegible]	[illegible]	[illegible]G
70°C	2 mV	T[illegible]	T[illegible]	T[illegible]G

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC251CDR).

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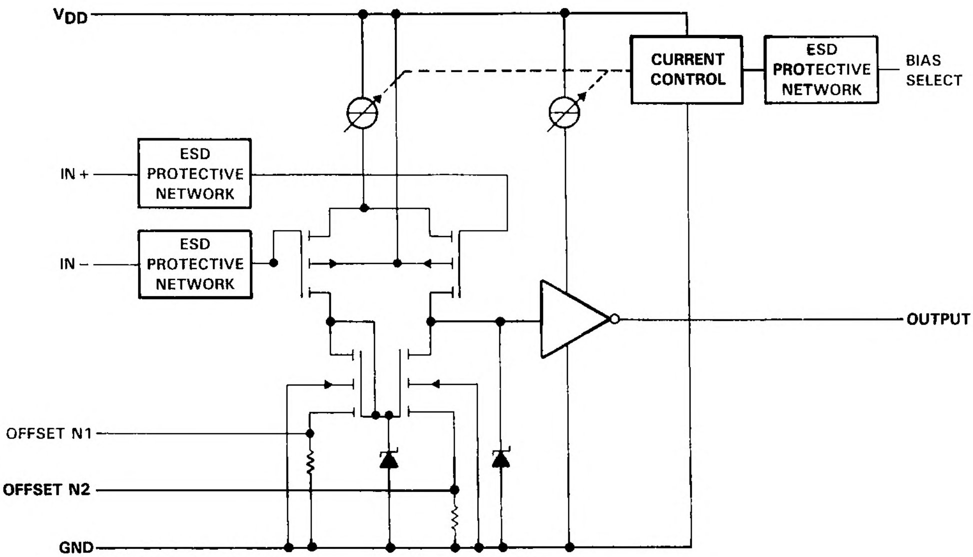
description (continued)

inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

schematic



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . ±18 V
Input voltage range (any input) . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C
Bias Select pin voltage		See Application Information			

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, R_S = 50 Ω	·	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	Low		0.7		μV/°C
					Medium		2		
					High		5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	−0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		V
				0°C to 70°C		7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	[illegible]		V/mV
					Medium	20	[illegible]		
					High	10	40		
				0°C to 70°C	Low	25			
					Medium	15			
					High	7.5			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	88		dB
					Medium	70	88		
					High	65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV				15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3		μA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	23	μA
					Medium		[illegible]	[illegible]	
					High		[illegible]	[illegible]	
				0°C to 70°C	Low			33	
					Medium			400	
					High			2200	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS[†]		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25 °C	Any			10	mV
				0 °C to 70 °C				12	
		TLC251AC		25 °C	Any			5	
				0 °C to 70 °C				6.5	
		TLC251BC		25 °C	Any			2	
				0 °C to 70 °C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25 °C to 70 °C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25 °C	Any		1		pA
				0 °C to 70 °C				300	
I_{IB}	Input bias current		V_O = 0.2 V	25 °C	Any		1		pA
				0 °C to 70 °C				600	
V_{ICR}	Common-mode input voltage range			25 °C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing[‡]		V_{ID} = 100 mV	25 °C	Any	450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25 °C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{IC} min	25 °C	Any	60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25 °C	Low		5	17	μA
					High		150	190	

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

[‡] The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25 °C

PARAMETER		TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1	Unity-gain bandwidth	C_L = 100 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		·		
			High		30%		

2 Operational Amplifiers

operating characteristics, $V_{DD} = 10$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1 Unity-gain bandwidth	$A_V = 40$ dB, $C_L = 100$ pF, $R_S = 50\ \Omega$	Low		0.1		MHz
		Medium		0.7		
		High		[illegible]		
SR Slew rate at unity gain	See Figure 1	Low		0.04		V/µs
		Medium		0.6		
		High		4.5		
Overshoot factor	See Figure 1	Low		30%		
		Medium		35%		
		High		35%		
ϕ_m Phase margin at unity gain	$A_V = 40$ dB, $R_S = 100\ \Omega$, $C_L = 100$ pF	Low		43°		
		Medium		43°		
		High		50°		
V_n Equivalent input noise voltage	f = 1 kHz, $R_S = 100\ \Omega$	Low		70		nV/√Hz
		Medium		38		
		High		30		

PARAMETER MEASUREMENT INFORMATION

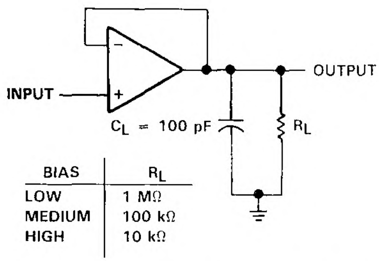

FIGURE 1. UNITY-GAIN AMPLIFIER

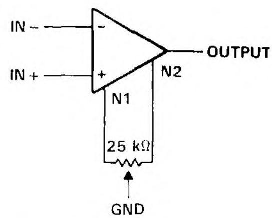

FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

2

Operational Amplifiers

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

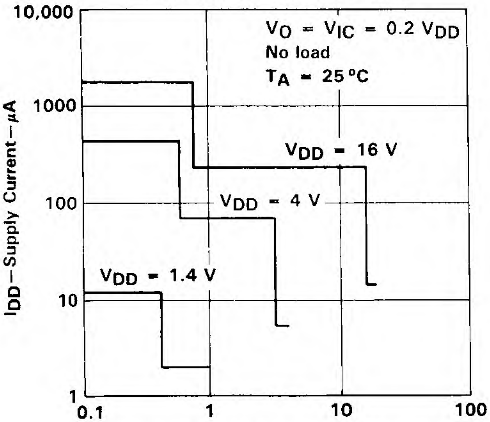


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

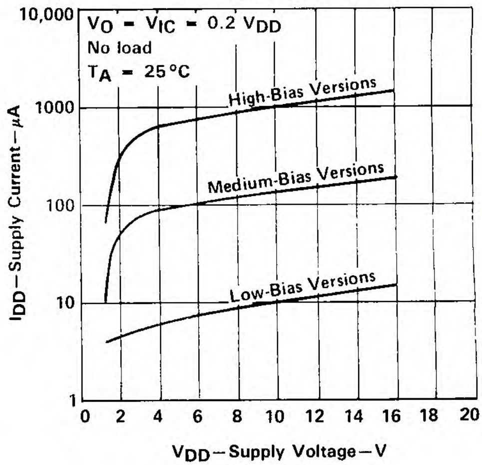


FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

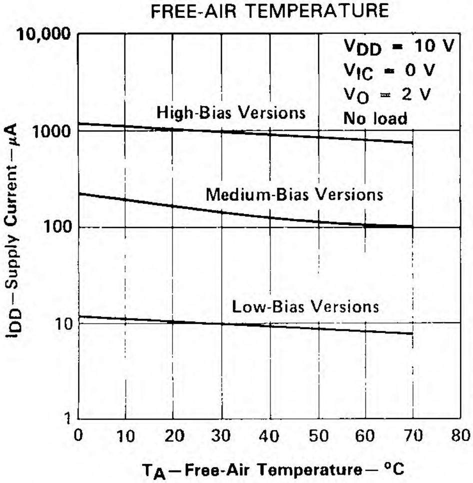


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

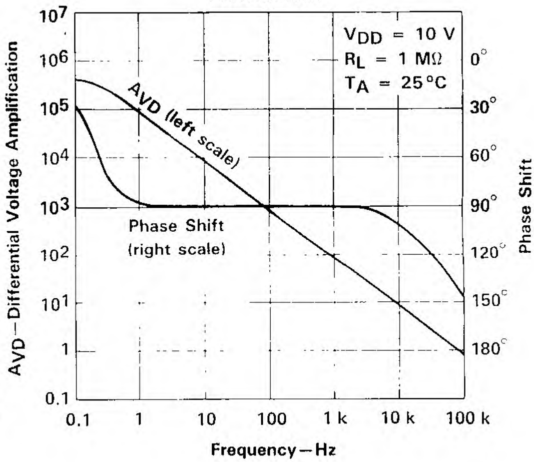


FIGURE 6

2

Operational Amplifiers

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

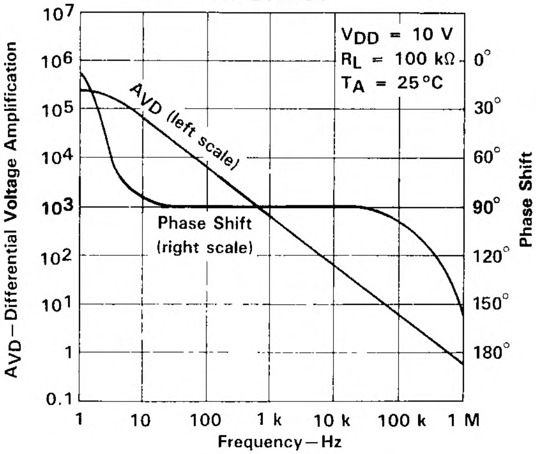


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

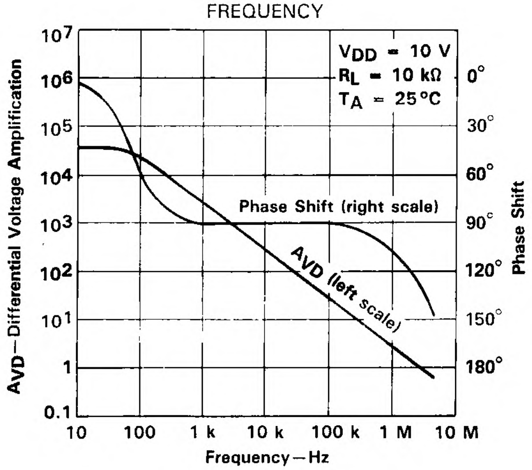


FIGURE 8

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251C series has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 V to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1.4 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.
‡For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At an I_{DD} setting of 1000 μA (high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low or medium bias or when the amplifier is used below 4 V, total nulling may not be possible for all units.

supply configurations

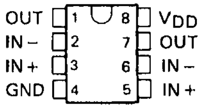
Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

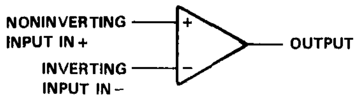
The user is cautioned that when ever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)

D, JG, OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC252C, TLC25L2C, and TLC25M2C are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC252C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252C series devices. Remote and inaccessible equipment

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)
0°C to 70°C	10 mV	TLC252CD	TLC252CP	TLC252CJG
	5 mV	TLC252ACD	TLC252ACP	TLC252ACJG
	2 mV	[illegible]	[illegible]	TLC252BCJG
	10 mV	[illegible]	[illegible]	TLC25L2CJG
	5 mV	TLC25L2ACD	TLC25L2ACP	TLC25L2ACJG
	2 mV	[illegible]	TLC25L2BCP	[illegible]
	10 mV	[illegible]	TLC25M2CP	[illegible]
	5 mV	TLC25M2ACD	TLC25M2ACP	TLC25M2ACJG
	2 mV	TLC25M2BCD	TLC25M2BCP	TLC25M2BCJG

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC252CDR).

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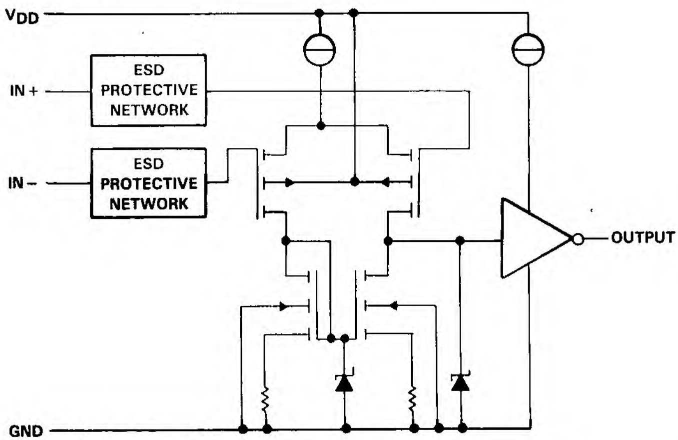
description (continued)

applications are possible using their low-voltage and low-power capabilities. The TLC252C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) .... 18 V
Differential input voltage (see Note 2) .... ±18 V
Input voltage range (any input) .... −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperture range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC[illegible]_C			TLC[illegible]_C			UNIT
					MIN	TYP	MAX	MIN	[illegible]	MAX	MIN	[illegible]	MAX	
V_O	Input offset voltage	TLC25_2C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		5			0.7			2		µV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		50	500		25	280		V/mV
				0°C to 70°C	7.5			50			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	65	88		65	88		65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C		2000	4000		20	46		300	600	µA
				0°C to 70°C			4400			66			800	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			[illegible]			[illegible]			UNIT
					[illegible]	TYP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			[illegible]			[illegible]			[illegible]	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6 5	
		TLC25_2BC		[illegible]			2			2			2	
				[illegible]o 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				[illegible] 70°C			[illegible]			[illegible]			[illegible]	
I_{IB}	Input bias current		V_O = 0.2 V	[illegible]		1			1			1		pA
				[illegible] 70°C			[illegible]			[illegible]			[illegible]	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		300	375		25	34		200	250	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 100 pF, R_S = 50 Ω		2.2			0.11			0.635		MHz
SR	Slew rate at unity gain	See Figure 1		4.6			0.05			0.56		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 100 pF		49°			38°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25			68			32		nV/√Hz
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

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operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS	TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1 Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
Overshoot factor	See Figure 1		30%			[illegible]			[illegible]		

PARAMETER MEASUREMENT INFORMATION

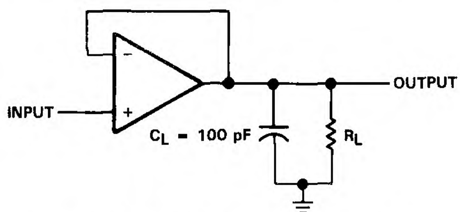


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

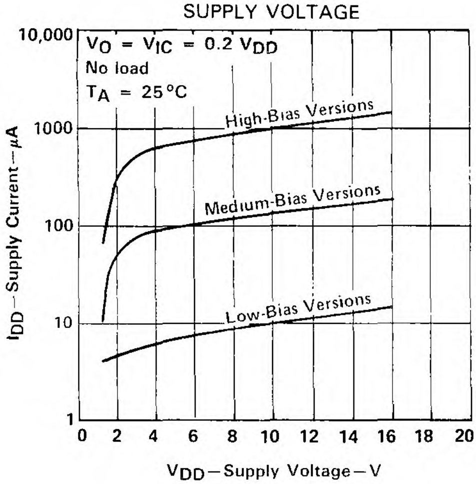


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

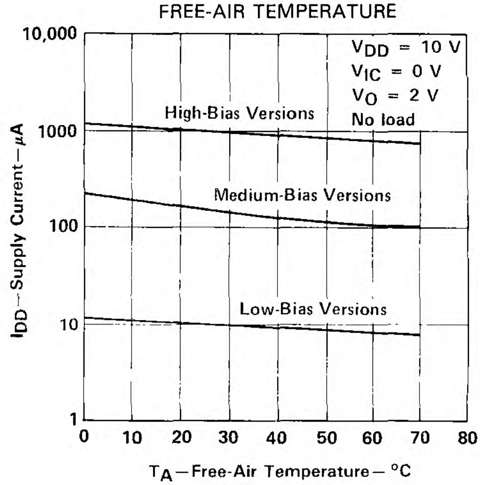


FIGURE 3

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

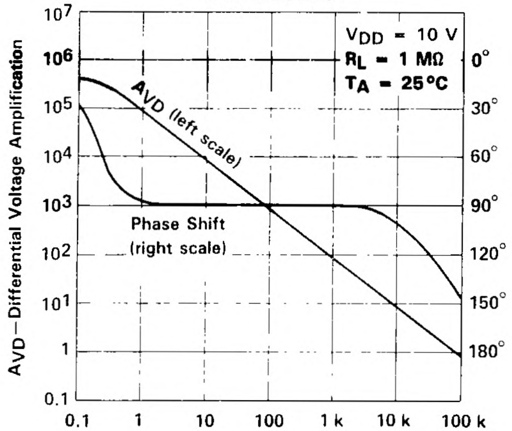


FIGURE 4

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

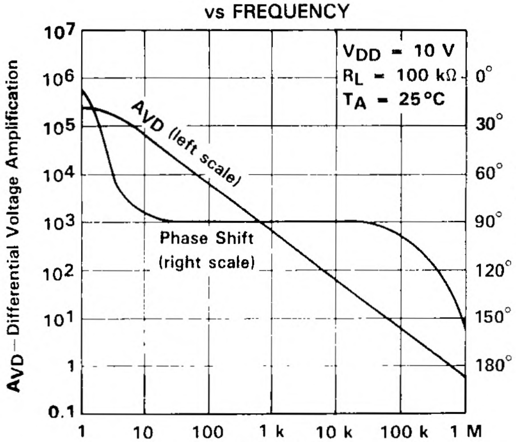


FIGURE 5

TYPICAL CHARACTERISTICS

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

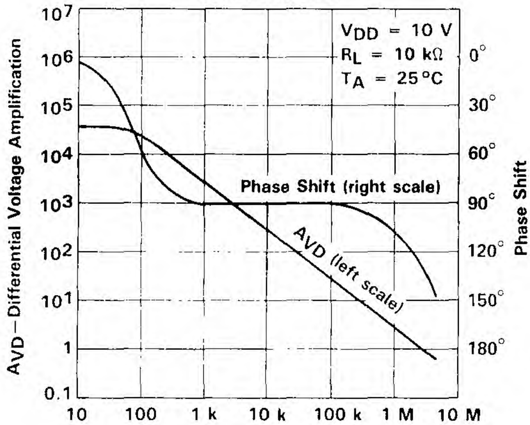


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

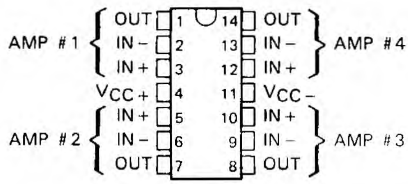
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

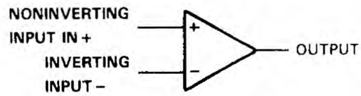
D2753, JUNE 1983—REVISED OCTOBER 1988

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each amplifier)



2

description

The TLC254C, TLC25L4C, and TLC25M4C are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC254C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	TLC254CD	TLC254CJ	TLC254CN
	5 mV	TLC254ACD	TLC254ACJ	TLC254ACN
	2 mV	[illegible]	TLC254BCJ	TLC254BCN
	10 mV	[illegible]	TLC25L4CJ	TLC25L4CN
	5 mV	TLC25L4ACD	TLC25L4ACJ	TLC25L4ACN
	2 mV	TLC25L4BCD	[illegible]	[illegible]
	10 mV	TLC25M4CD	[illegible]	[illegible]
	5 mV	TLC25M4ACD	TLC25M4ACJ	TLC25M4ACN
	2 mV	TLC25M4BCD	TLC25M4BCJ	TLC25M4BCN

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC254CDR).

LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

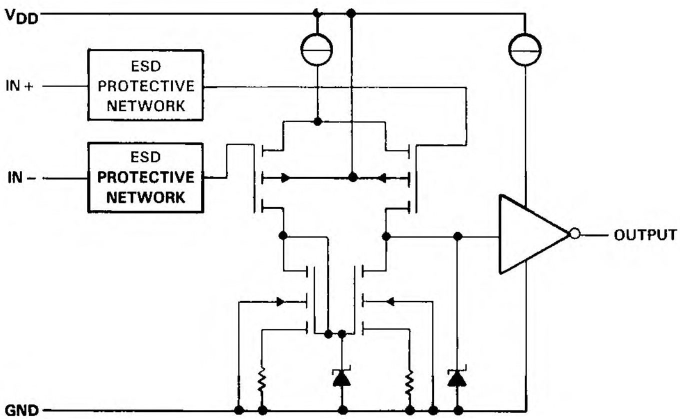
buffering are all easily designed with the TLC254C series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC254C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

DEVICE FEATURES

PARAMETER	TLC25L4C (LOW BIAS)	TLC25M4C (MEDIUM BIAS)	TLC254C (HIGH BIAS)
Supply current (Typ)	40 μA	[illegible] μA	4000 μA
Slew rate (Typ)	0.04 V/μs	[illegible] V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV [illegible]†	0.1 μV [illegible]†	0.1 μV [illegible]†
Offset voltage temperature coefficient (Typ)	0.7 [illegible]	2 μ[illegible]	5 μ[illegible]
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . ±18 V
Input voltage range (any input) . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C MIN	TLC254_C TYP	TLC254_C MAX	TLC25L4_C MIN	TLC25L4_C TYP	TLC25L4_C MAX	TLC25M4_C MIN	TLC25M4_C TYP	TLC25M4_C MAX	UNIT
V_{IO}	Input offset voltage	TLC25_4C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		5			0.7			2		µV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		50	500		25	280		V/mV
				0°C to 70°C	7.5			50			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	65	88		65	88		65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C		4000	8000		40	92		600	1200	µA
				0°C to 70°C			8800			132			1600	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC[illegible]M[illegible]_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	[illegible]	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	[illegible]°C			10			10			10	mV
				[illegible] to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		600	750		50	68		400	500	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 100 pF, R_S = 50 Ω		2.2			0.11			0.635		MHz
SR	Slew rate at unity gain	See Figure 1		4.6			0.05			0.56		V/μs
	Overshoot factor	See Figure 1		30%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 100 pF		49°			38°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25			68			32		nV/√Hz
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		[illegible]			35%			35%		

PARAMETER MEASUREMENT INFORMATION

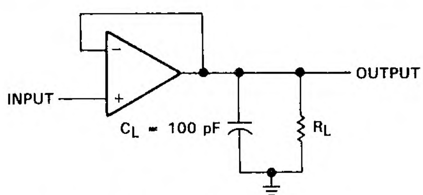


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

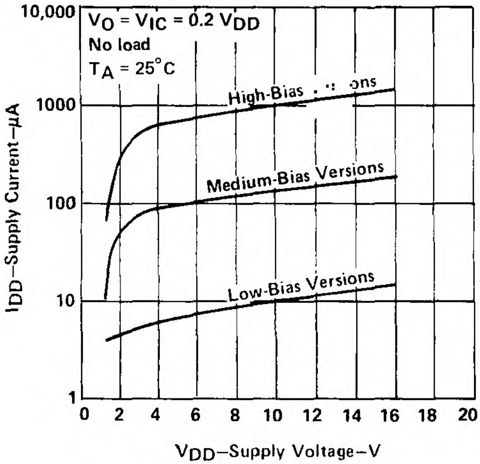


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

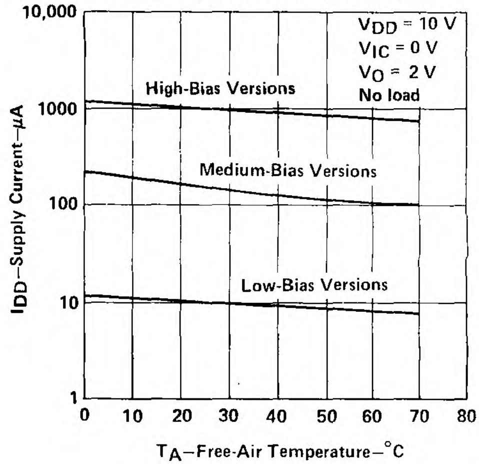


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

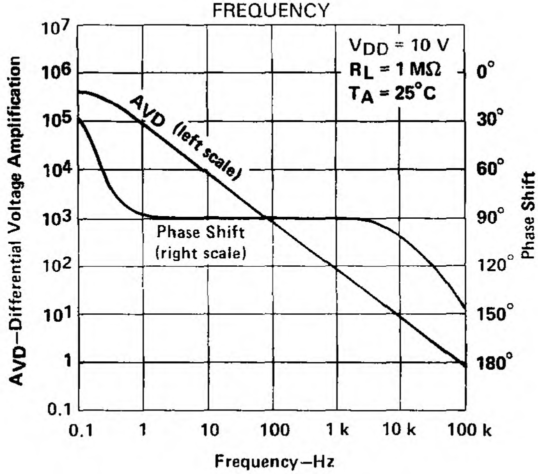


FIGURE 4

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

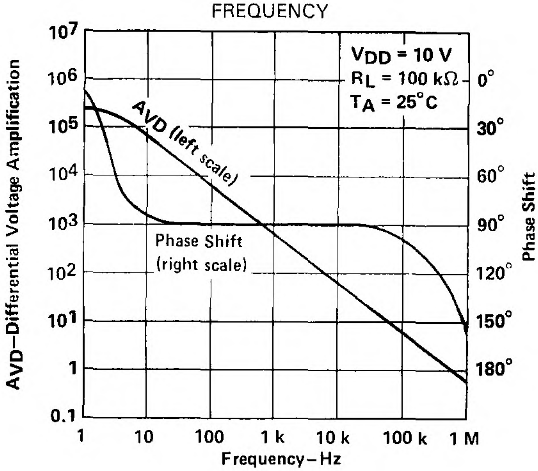


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

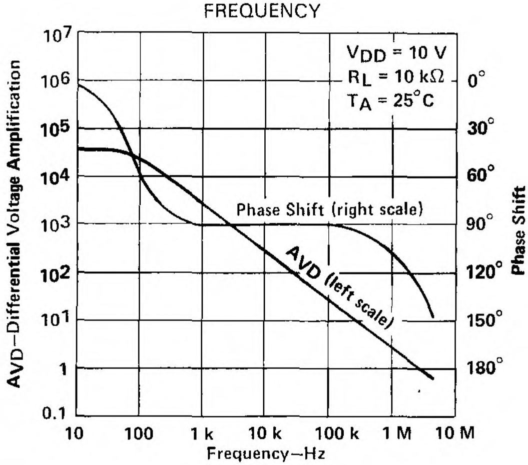


FIGURE 6

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TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC254C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

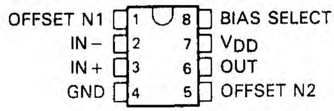
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

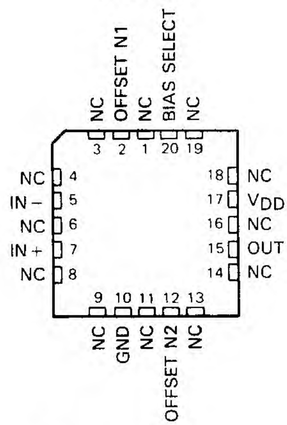
D3137, NOVEMBER 1987—REVISED MARCH 1989

- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  −55°C to 125°C . . . 5 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV $\sqrt{Hz}$ at f = 1 kHz (High-Bias Mode)
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latchup Immunity

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift, and high input impedance. In addition, the TLC271 offers a bias select mode which allows the user to select the best combination of power dissipation and AC performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

AVAILABLE OPTIONS

T_A	$V_{IO}max$ at 25°C	PACKAGE SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV	TLC271BCD	—	TLC271BC[illegible]	[illegible]
	5 mV	TLC271ACD	—	TLC27[illegible]	[illegible]
	10 mV	TLC271[illegible]	—	TLC27[illegible]	[illegible]
−40°C to 85°C	2 mV	TLC27[illegible]	—	TLC271BIJG	TLC271BIP
	5 mV	TLC27[illegible]	—	TLC271AIJG	TLC271AIP
	10 mV	TLC271ID	—	TLC271IJG	TLC271IP
−55°C to 125°C	10 mV	—	TLC271MFK	TLC271MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC271BCDR)

DEVICE FEATURES TYPICAL at V_{DD} = 5 V, T_A = 25°C	BIAS SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	[illegible]	μW
SR	[illegible]	0.4	[illegible]	V/μs
V_n	[illegible]	32	[illegible]	nV/$\sqrt{Hz}$
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

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description (continued)

Using the bias select option, these cost-effective devices can be "programmed" to span a wide range of applications which previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC271 (10 mV) to the TLC271B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC271. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC271 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

bias select feature

The TLC271 offers a bias select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The trade-offs between bias levels involve AC performance and power dissipation (see Table 1).

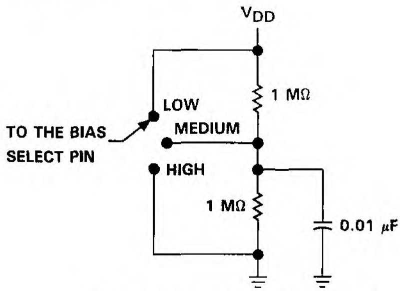
TABLE 1. EFFECT OF BIAS SELECTION ON PERFORMANCE

TYPICAL PARAMETER VALUES $T_A = 25°C$, $V_{DD} = 5$ V		MODE			UNITS
		HIGH-BIAS $R_L = 10$ kΩ	MEDIUM-BIAS $R_L = 100$ kΩ	LOW-BIAS $R_L = 1$ MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/$\sqrt{Hz}$
B_1	Unity-gain bandwidth	1.7	0.5	[illegible]	[illegible]
ϕ_m	Phase margin	46°	40°	[illegible]	
A_{VD}	Large-signal differential voltage amplification	23	170	[illegible]	V/mV

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This proceduce is simple in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.

bias selection (continued)



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
[illegible]M	1 V to [illegible] − 1 V
HIGH	[illegible]

FIGURE 1. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices, but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

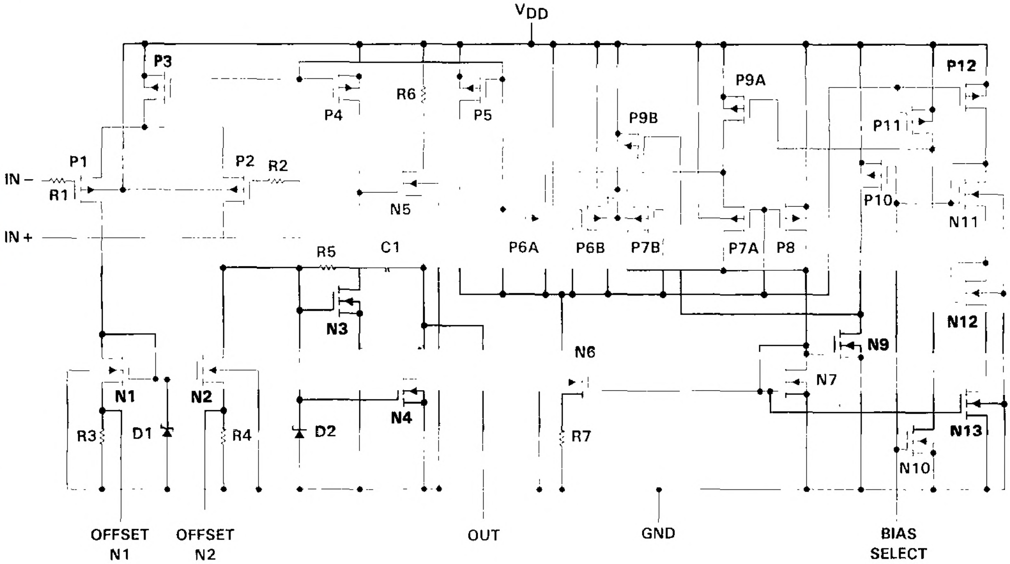
low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

ORDER OF CONTENTS

TOPIC	BIAS MODE
schematic	all
absolute maximum ratings	all
recommended operating conditions	all
electrical characteristics operating characteristics typical characteristics	high (Figures 2–33)
electrical characteristics operating characteristics typical characteristics	medium (Figures 34–65)
electrical characteristics operating characteristics typical characteristics	low (Figures 66–97)
parameter measurement information	all
typical application data	all

equivalent schematic



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) .... 18 V
Differential input voltage (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... −0.3 V to V_{DD}
Input current, I_I .... ±5 mA
Output current, I_O .... ±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... −55°C to 125°C
I-suffix .... −40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		5		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			−55°C	3	3.8		7.8	8.5		
			125°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
			−55°C	3.5	35		7	50		
			125°C	3.5	16		7	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
			−55°C	60	81		60	87		
			125°C	60	84		60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
			−55°C	60	90		60	90		
			125°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675			950		μA
			−55°C		1000			1475		
			125°C		475	1100		625	1400	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		[illegible]		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		[illegible]	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				−40°C	3	3.8		7.8	8.5		
				85°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				−40°C	3.5	32		7	46		
				85°C	3.5	19		7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				−40°C	60	81		60	87		
				85°C	60	86		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				−40°C	60	92		60	92		
				85°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		675	[illegible]		[illegible]	[illegible]	μA
				−40°C		[illegible]	[illegible]		[illegible]	[illegible]	
				85°C		[illegible]	[illegible]		725	1600	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	[illegible]		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	[illegible]	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		675	1600		[illegible]	[illegible]	μA
				0°C		775	1800		[illegible]	[illegible]	
				70°C		575	1300		[illegible]	[illegible]	

†Full range is −0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				[illegible] C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		49°		
				−55°C		52°		
				125°C		44°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN TYP MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C	3.6	V/μs
				−40°C	4.5	
				85°C	2.8	
			V_{IPP} = 2.5 V	25°C	2.9	
				−40°C	3.5	
				85°C	2.3	
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C	25	nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C	320	kHz
				−40°C	380	
				85°C	[illegible]	
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C	[illegible]	MHz
				−40°C	2.6	
				85°C	1.2	
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C	46°	
				−40°C	49°	
				85°C	43°	

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN TYP MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C	5.3	V/μs
				−40°C	6.8	
				85°C	4	
			V_{IPP} = 5.5 V	25°C	4.6	
				−40°C	5.8	
				85°C	3.5	
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C	25	nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C	200	kHz
				−40°C	260	
				85°C	130	
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C	2.2	MHz
				−40°C	3.1	
				85°C	1.7	
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C	49°	
				−40°C	52°	
				85°C	46°	

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		49°		
				0°C		50°		
				70°C		46°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

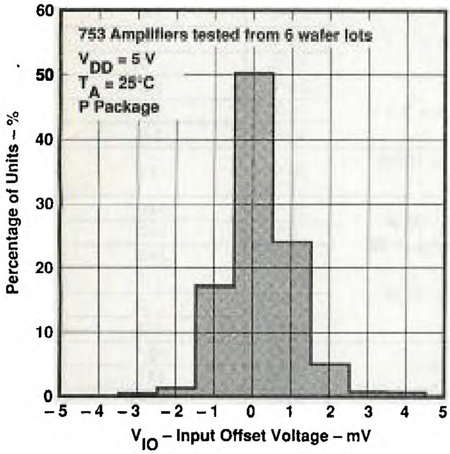

FIGURE 2

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

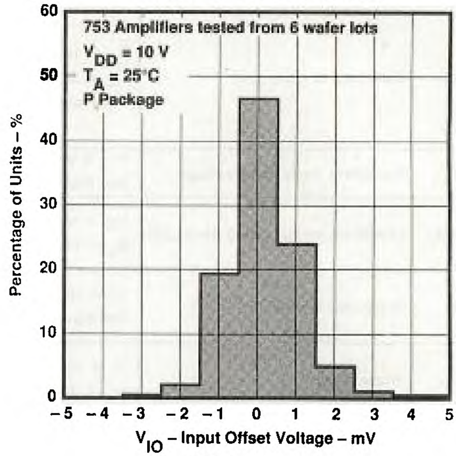

FIGURE 3

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

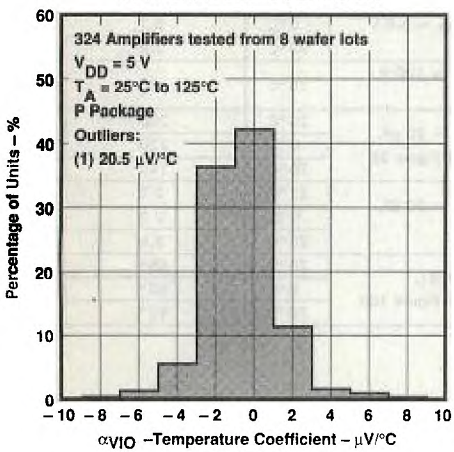

FIGURE 4

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

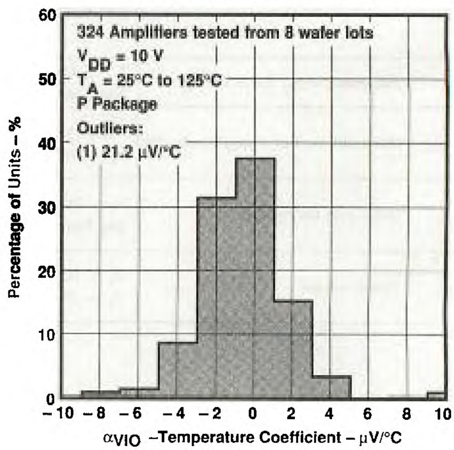

FIGURE 5

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

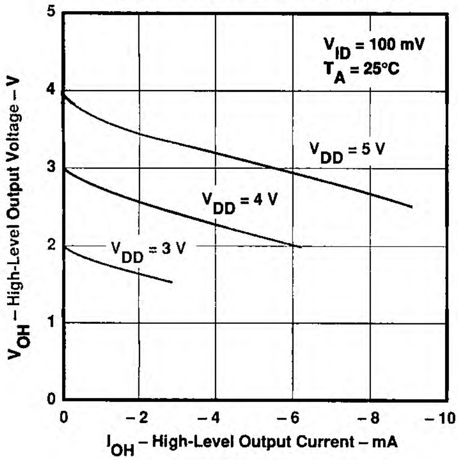

FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

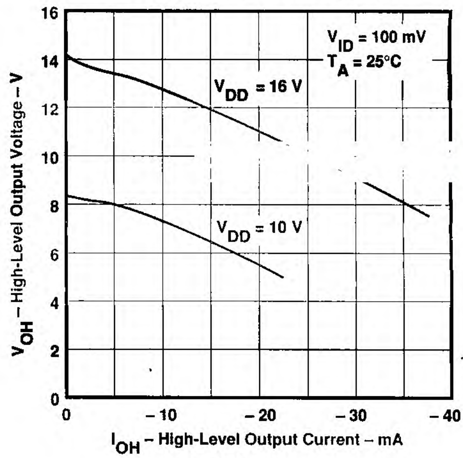

FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

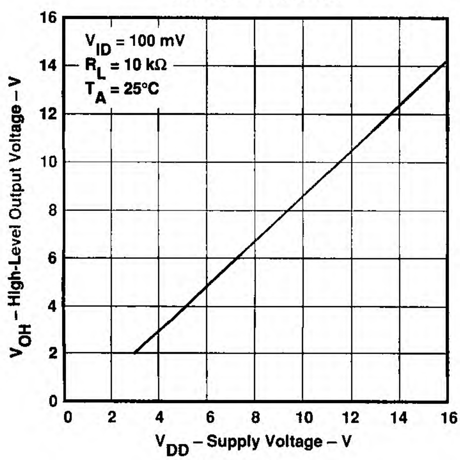

FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

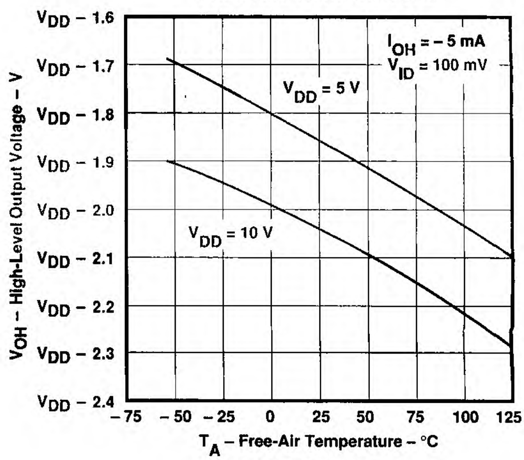

FIGURE 9

Operational Amplifiers

2

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

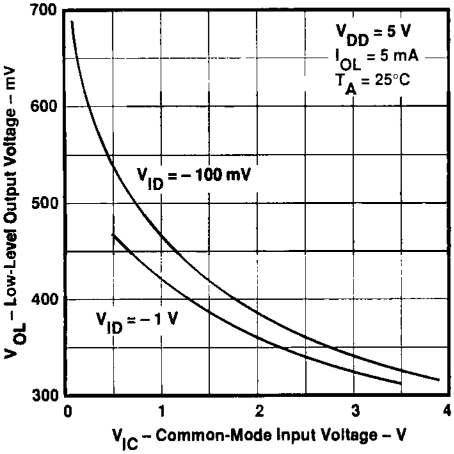

FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

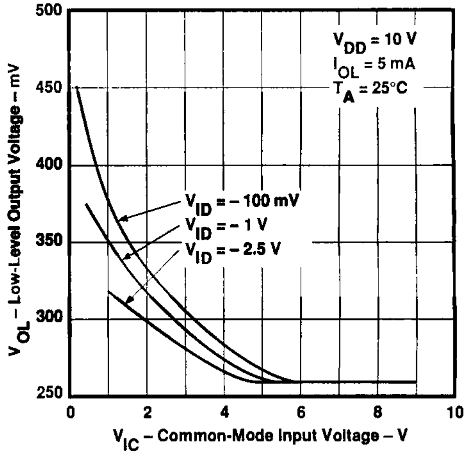

FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

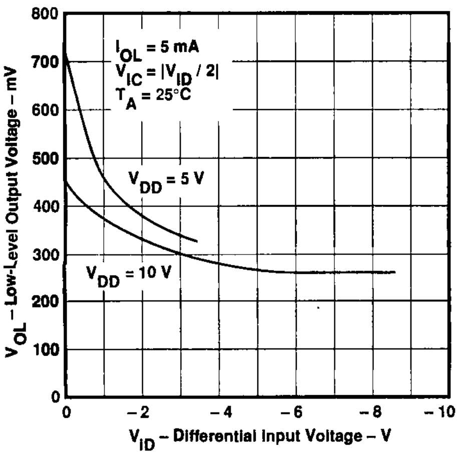

FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

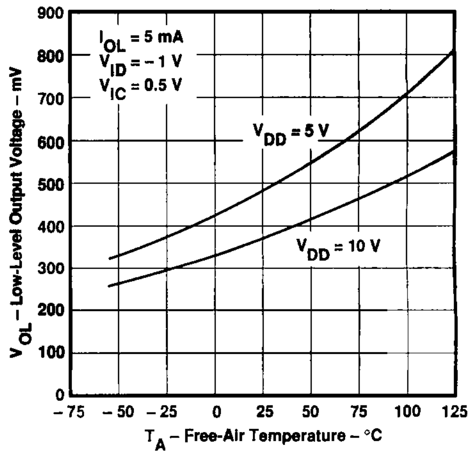

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

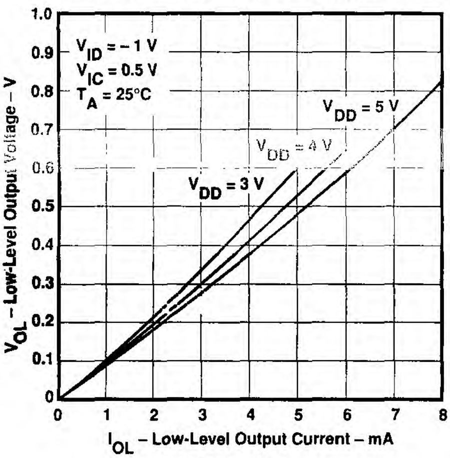

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

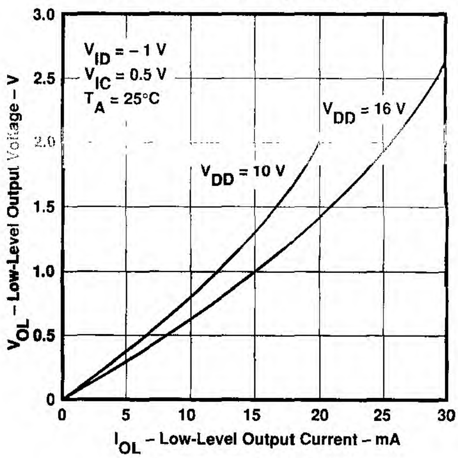

FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

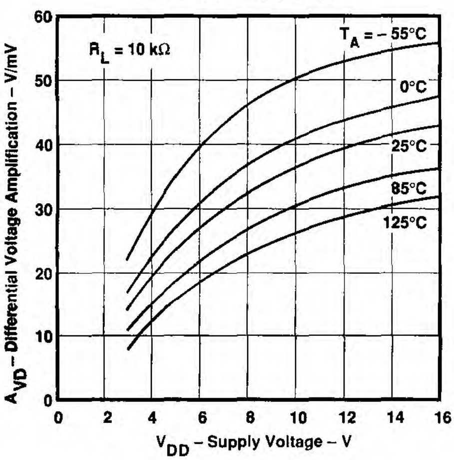

FIGURE 16

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

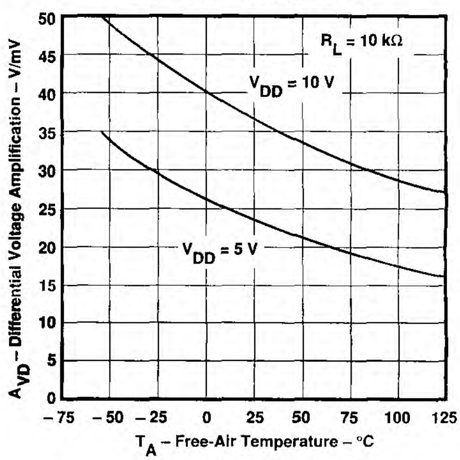

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

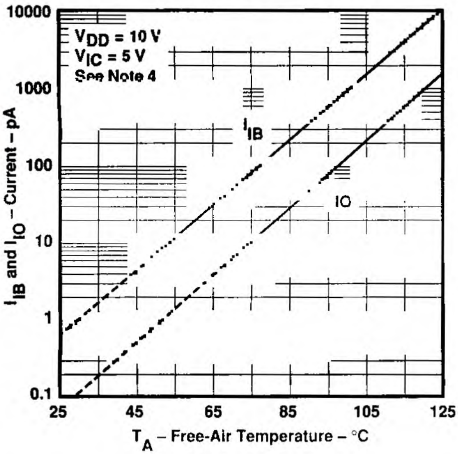

FIGURE 18

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

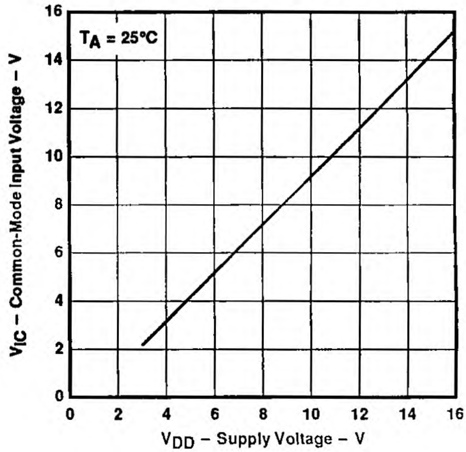

FIGURE 19

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

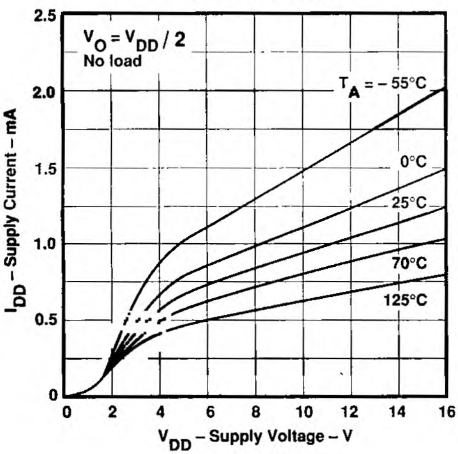

FIGURE 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

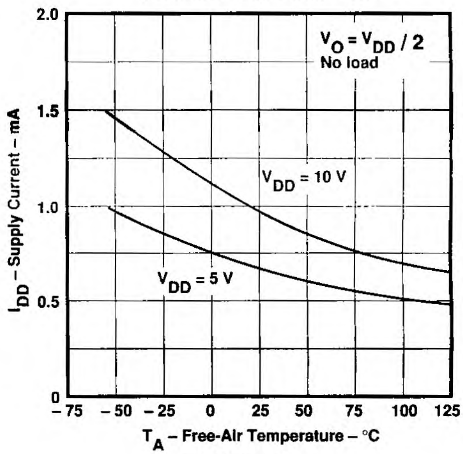

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

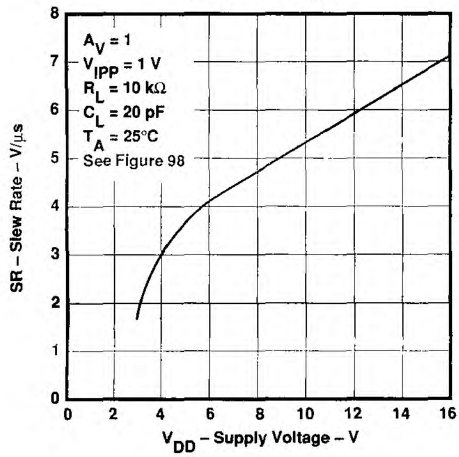

FIGURE 22

SLEW RATE
vs
FREE-AIR TEMPERATURE

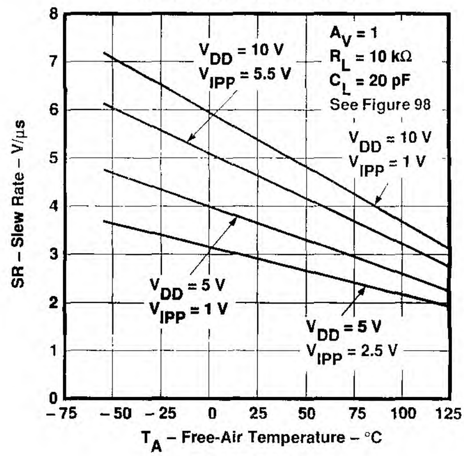

FIGURE 23

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

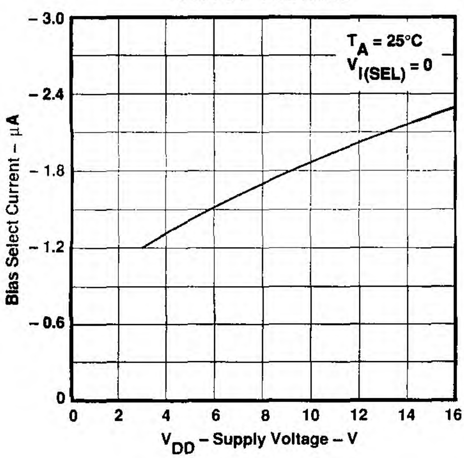

FIGURE 24

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

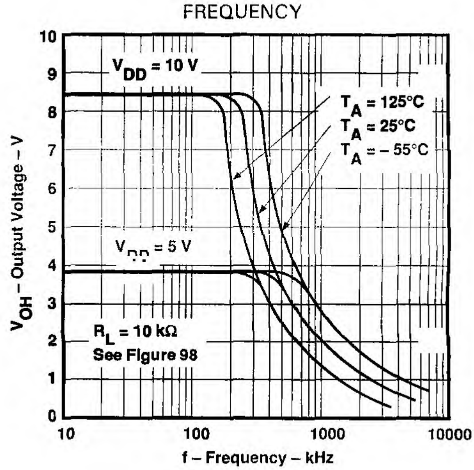

FIGURE 25

2

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

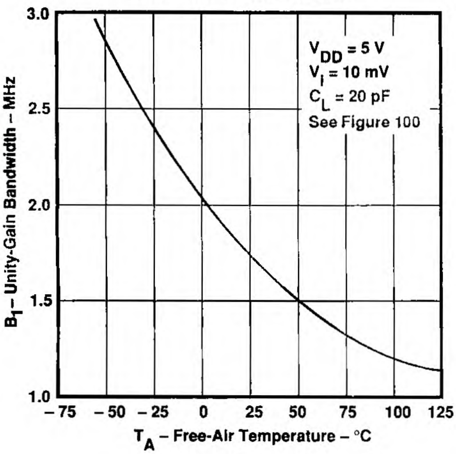

FIGURE 26

UNDITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

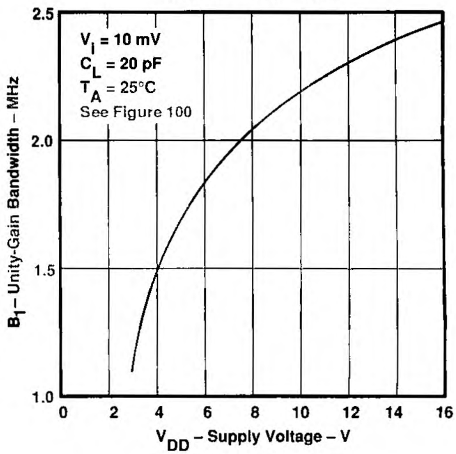

FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

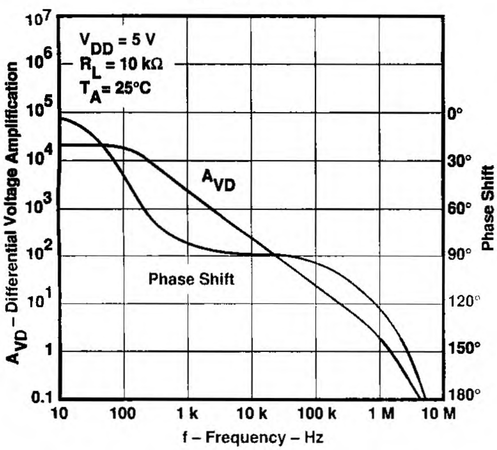

FIGURE 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

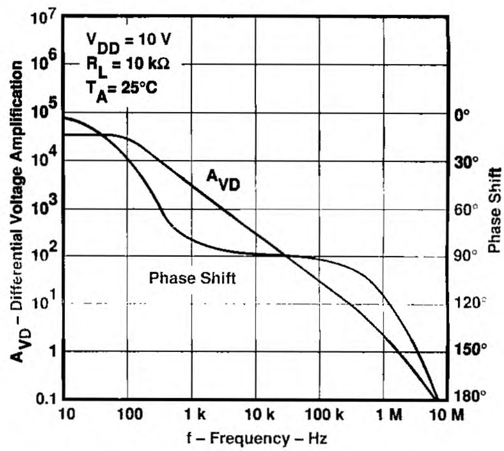

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

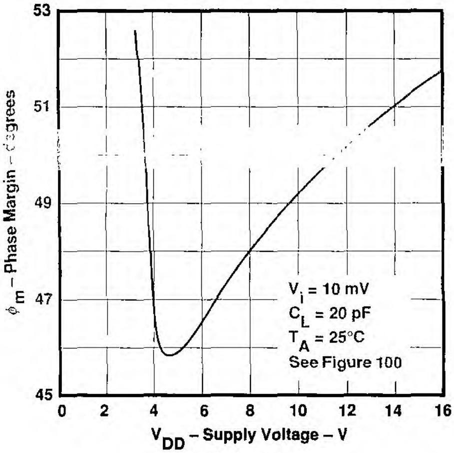

FIGURE 30

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

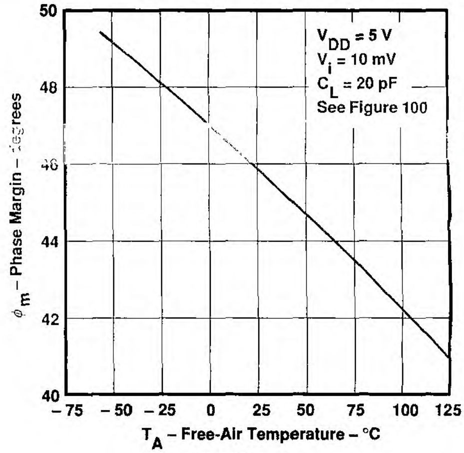

FIGURE 31

PHASE MARGIN
vs
CAPACITIVE LOAD

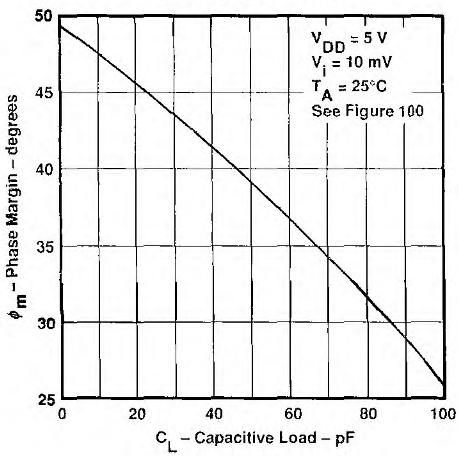

FIGURE 32

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

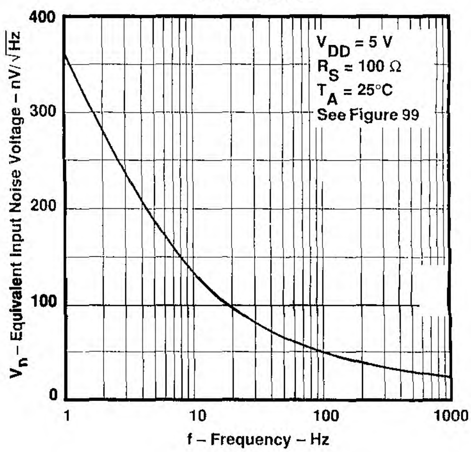

FIGURE 33

2

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			−55°C	3	3.9		7.8	8.6		
			125°C	3	4		7.8	8.8		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
			−55°C	15	[illegible]		15	420		
			125°C	15	[illegible]		15	190		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
			−55°C	60	89		60	93		
			125°C	60	91		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
			−55°C	60	91		60	91		
			125°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD}/2	25°C		[illegible]			−160		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		[illegible]	280		143	[illegible]	μA
			−55°C		170	440		245	[illegible]	
			[illegible]		70	180		90	240	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

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MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				−40°C	3	3.9		7.8	8.7		
				85°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				−40°C	15	270		15	[illegible]		
				85°C	15	130		15	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				−40°C	60	90		60	93		
				85°C	60	90		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				−40°C	60	91		60	91		
				85°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = $V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		105	280		143	300	μA
				−40°C		158	[illegible]		[illegible]	[illegible]	
				85°C		80	[illegible]		[illegible]	[illegible]	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

2

Operational Amplifiers

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	[illegible]		
				70°C	15	140		15	[illegible]		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		105	280		143	300	μA
				0°C		[illegible]	[illegible]		173	400	
				70°C		[illegible]	[illegible]		110	[illegible]	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

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MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−55°C		43°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−55°C		50		
				[illegible]		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−55°C		47°		
				125°C		39°		

2 Operational Amplifiers

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C				kHz
				−40°C				
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C				kHz
				−40°C				
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−40°C		46°		
				85°C		41°		

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MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0 36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	[illegible]		[illegible]		[illegible]
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				0°C		44°		
				70°C		42°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

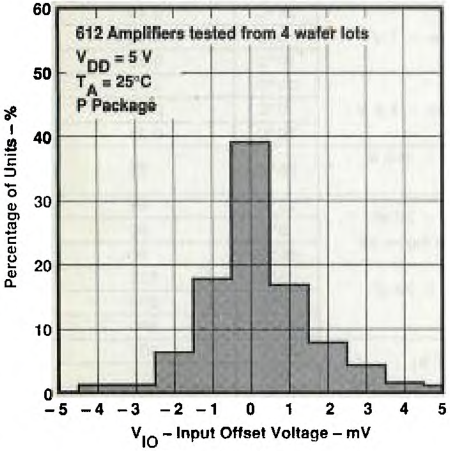

FIGURE 34

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

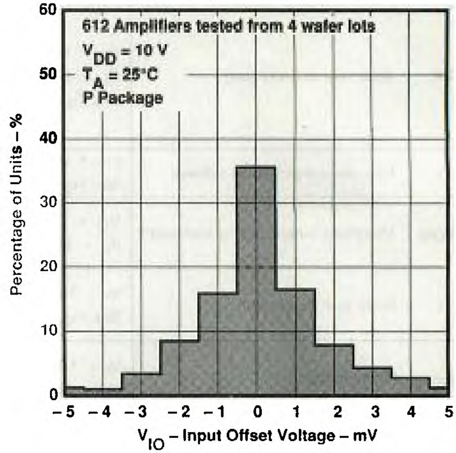

FIGURE 35

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

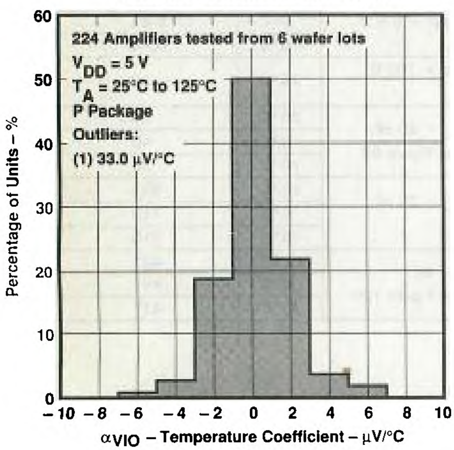

FIGURE 36

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

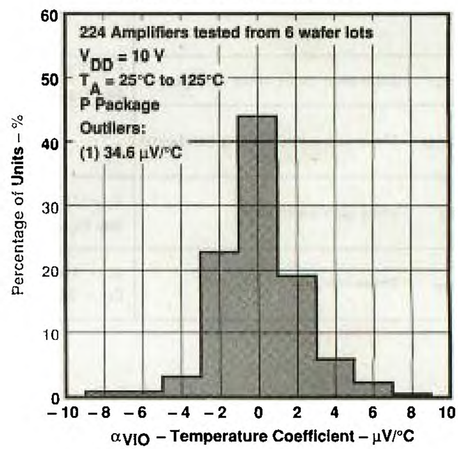

FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

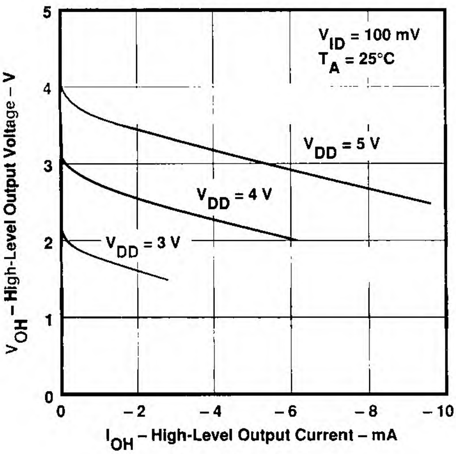

FIGURE 38

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

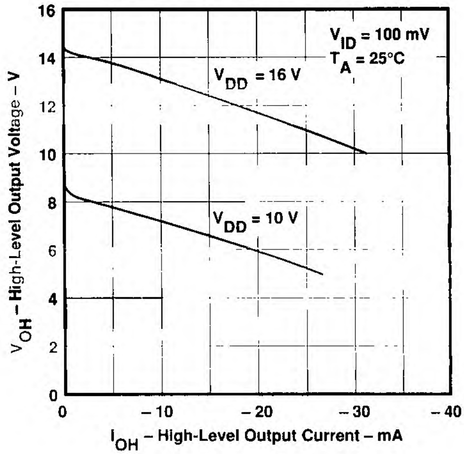

FIGURE 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

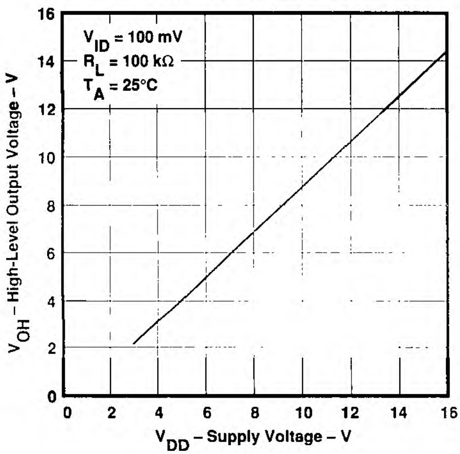

FIGURE 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

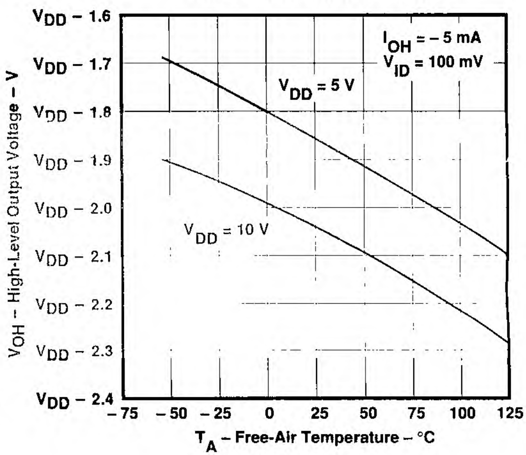

FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

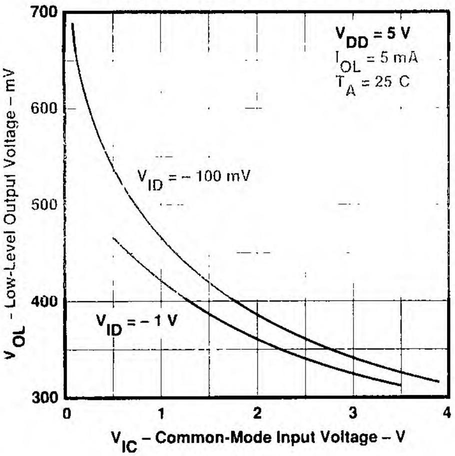

FIGURE 42

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

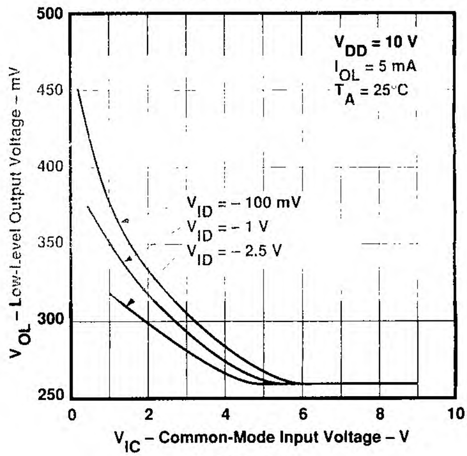

FIGURE 43

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

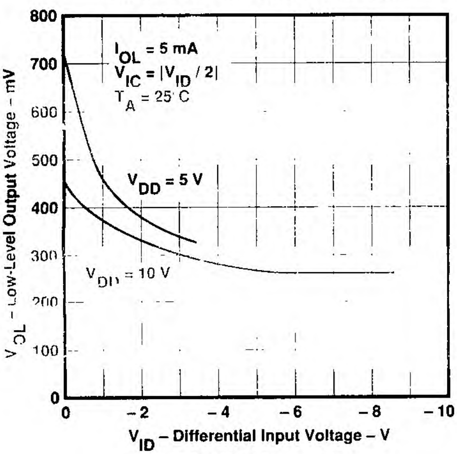

FIGURE 44

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

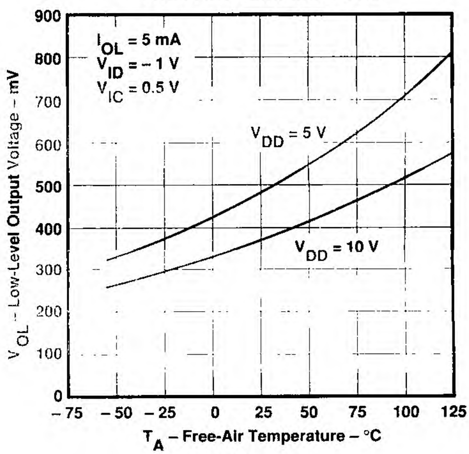

FIGURE 45

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

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TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

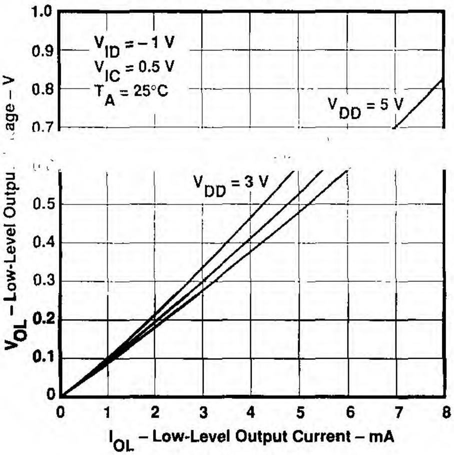

FIGURE 46

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

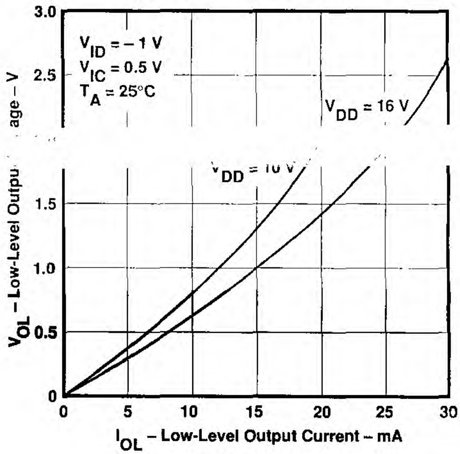

FIGURE 47

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

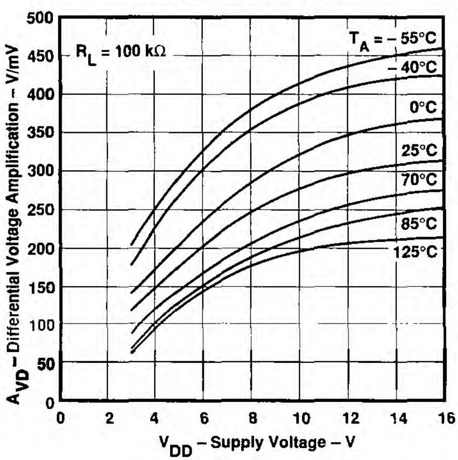

FIGURE 48

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

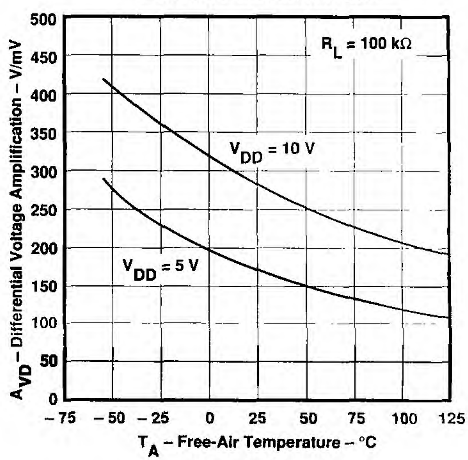

FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

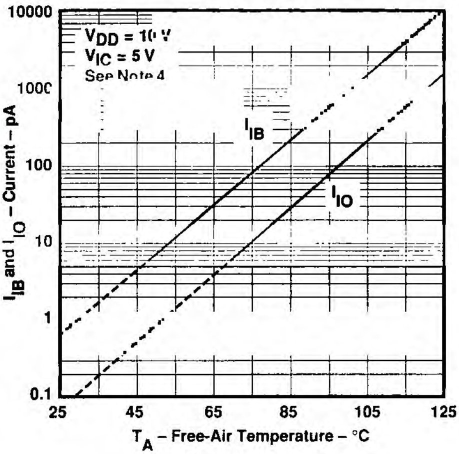

FIGURE 50

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

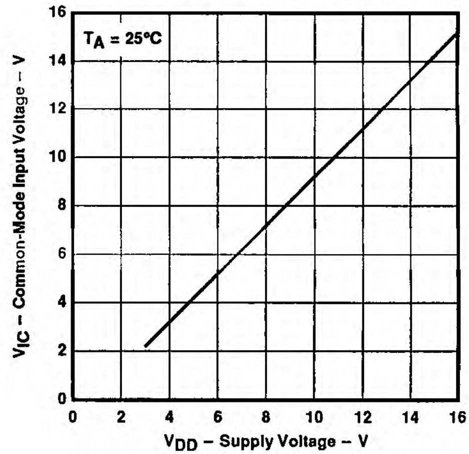

FIGURE 51

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

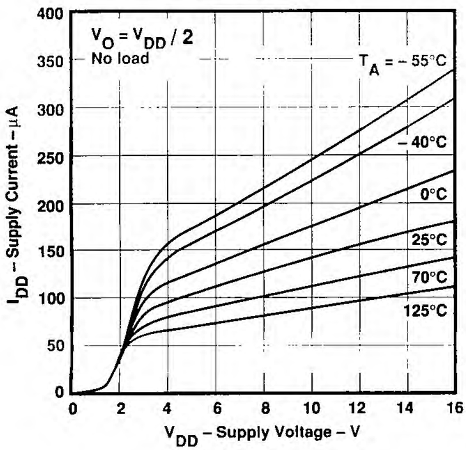

FIGURE 52

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

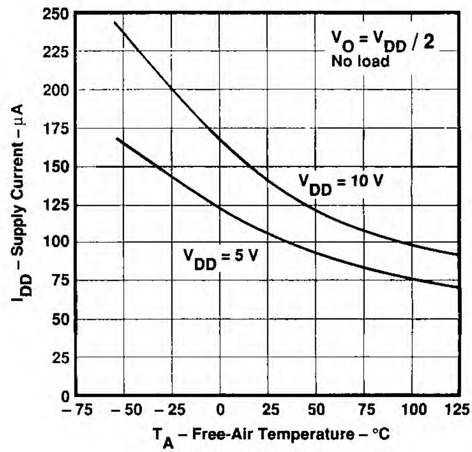

FIGURE 53

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

NOTE 4: The typical values of input bias current and input offset current and input offset current below 5 pA were determined mathematically.

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TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

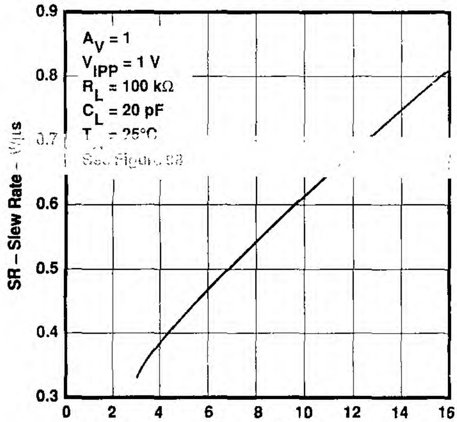

FIGURE 54

SLEW RATE
vs
FREE-AIR TEMPERATURE

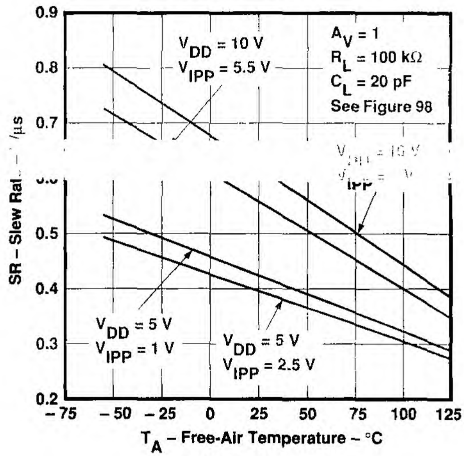

FIGURE 55

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

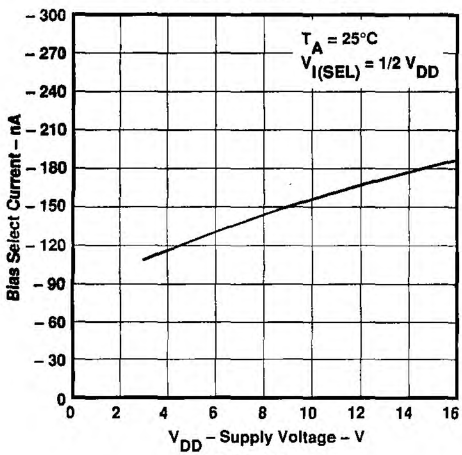

FIGURE 56

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

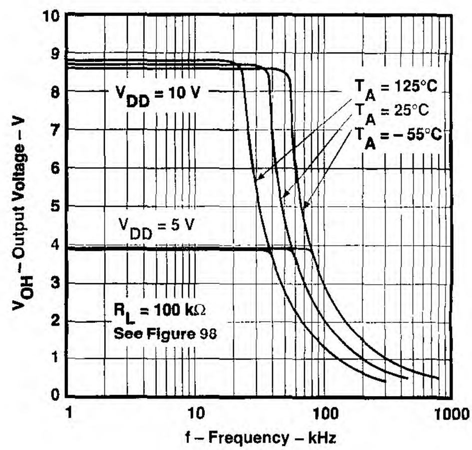

FIGURE 57

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

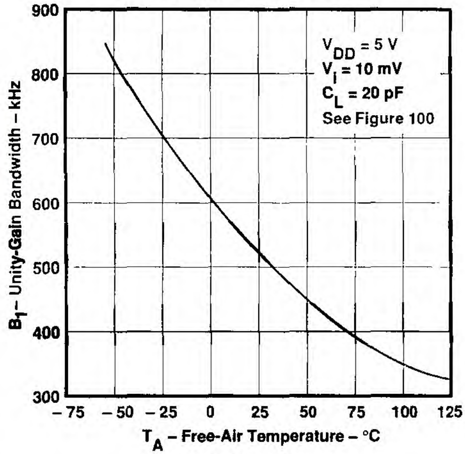

FIGURE 58

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

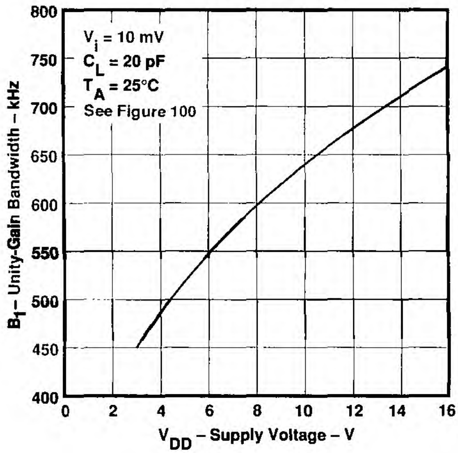

FIGURE 59

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

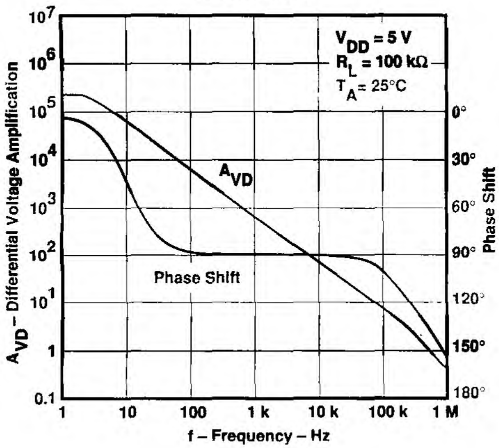

FIGURE 60

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

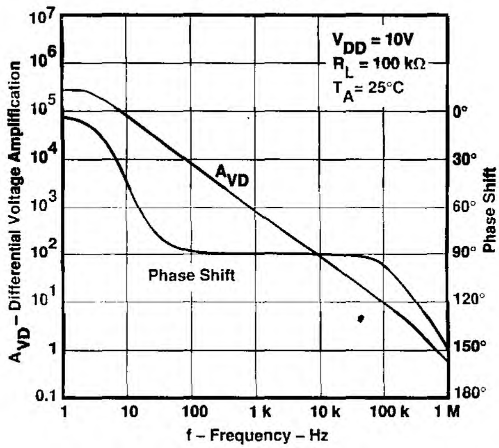

FIGURE 61

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

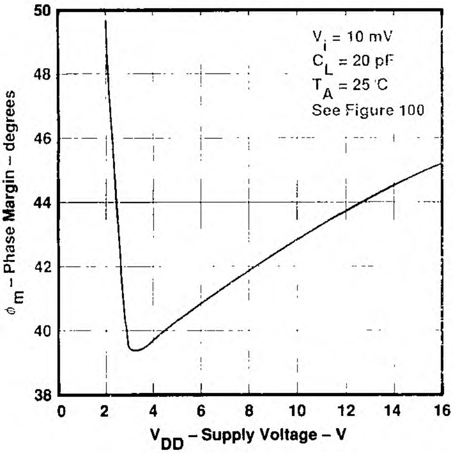

FIGURE 62

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

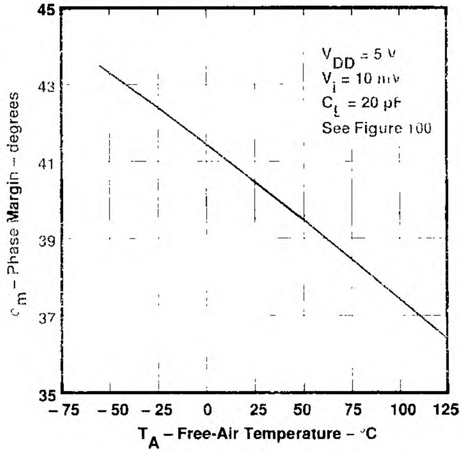

FIGURE 63

PHASE MARGIN
vs
CAPACITIVE LOAD

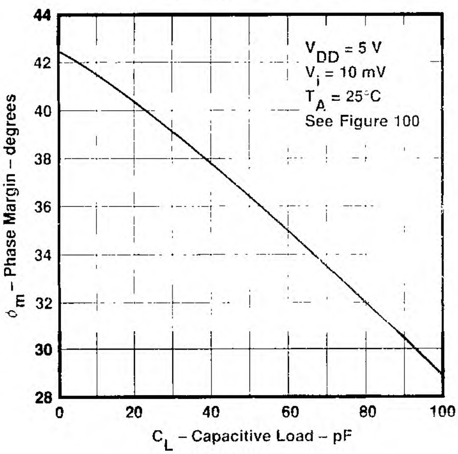

FIGURE 64

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

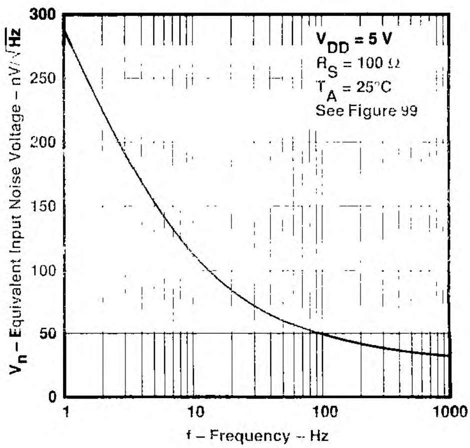

FIGURE 65

2

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			−55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			−55°C	25	[illegible]		25	1775		
			125°C	25	[illegible]		25	[illegible]		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	94		65	[illegible]		dB
			−55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			−55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
			−55°C		17	30		28	48	
			125°C		7	12		9	15	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

TEXAS INSTRUMENTS
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LOW-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full			7			7	
		TLC271BI		[illegible]		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				−40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				−40°C	50	[illegible]		50	[illegible]		
				85°C	50	[illegible]		50	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				−40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				−40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
				−40°C		16	27		25	43	
				85°C		7	13		10	18	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

2

Operational Amplifiers

LOW-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					[illegible]	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	[illegible]		50	870		V/mV
				0°C	50	[illegible]		50	[illegible]		
				70°C	50	380		50	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

TEXAS INSTRUMENTS
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LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				[illegible]C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				−55°C		43°		
				125°C		29°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				−40°C		42°		
				85°C		32°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				0°C		40°		
				70°C		34°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

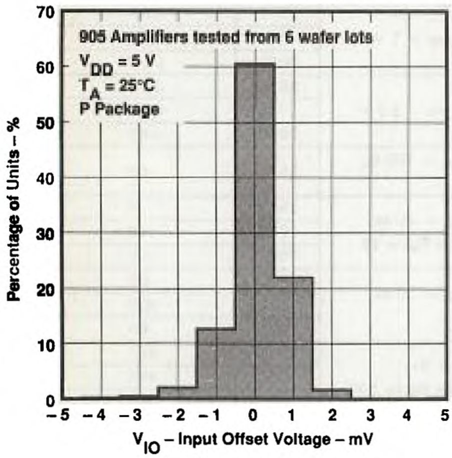

FIGURE 66

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

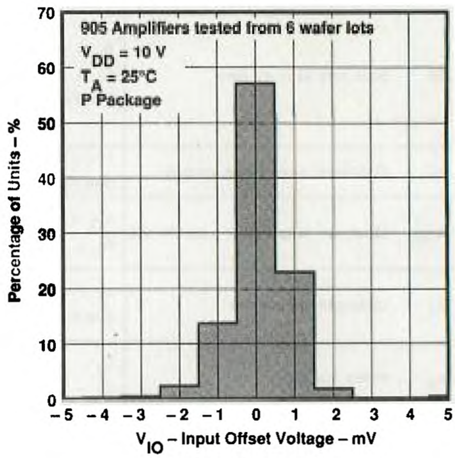

FIGURE 67

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

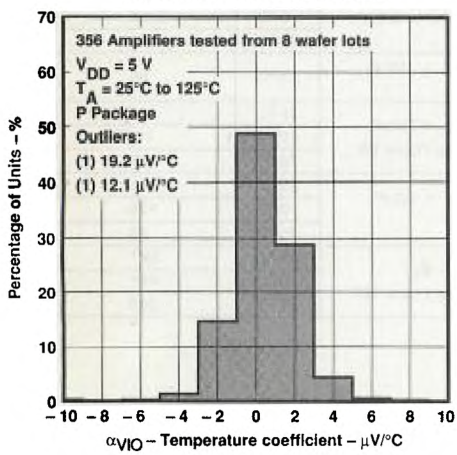

FIGURE 68

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

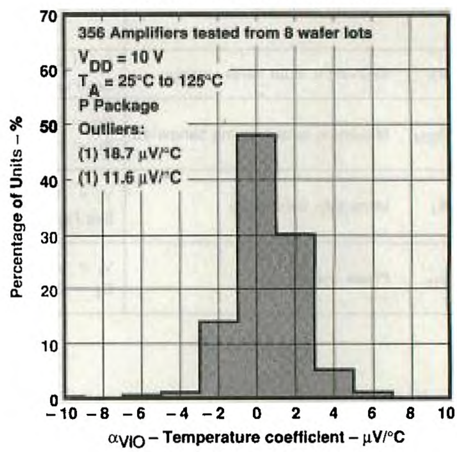

FIGURE 69

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

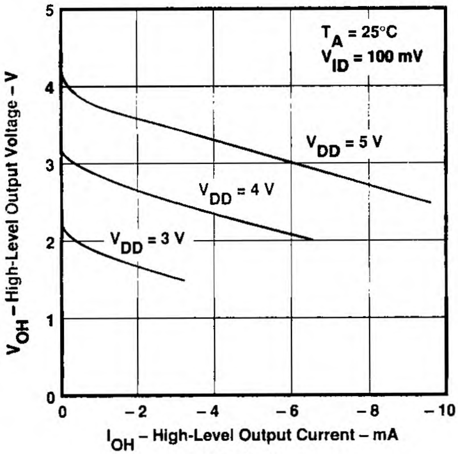

FIGURE 70

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

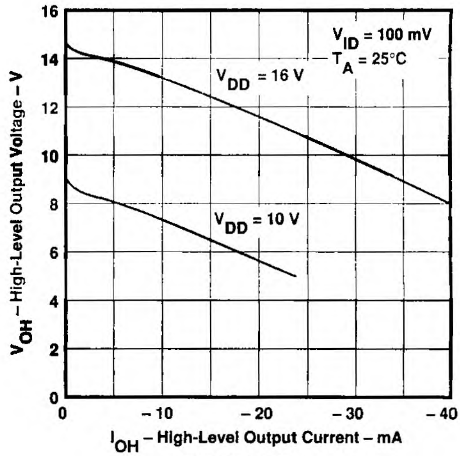

FIGURE 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

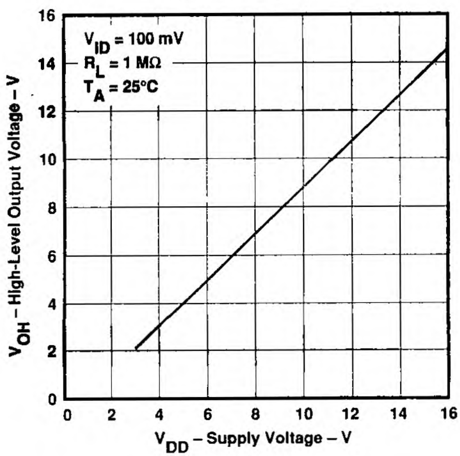

FIGURE 72

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

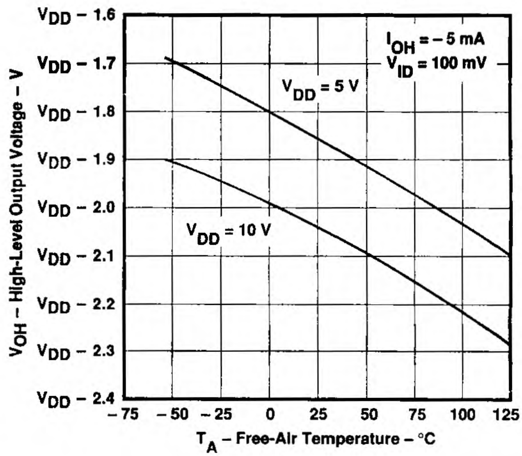

FIGURE 73

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

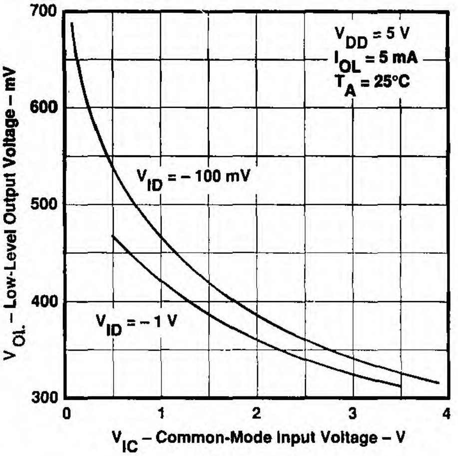

FIGURE 74

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

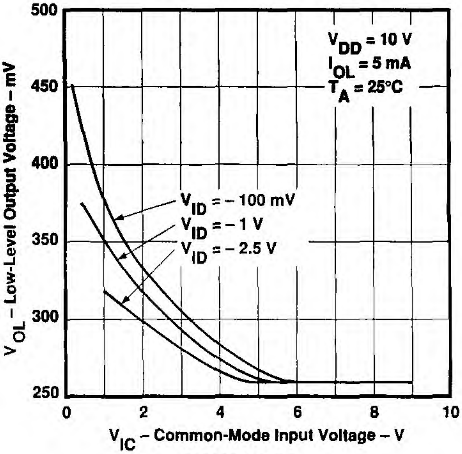

FIGURE 75

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

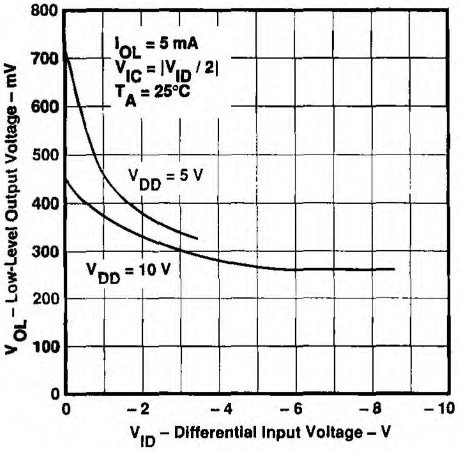

FIGURE 76

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

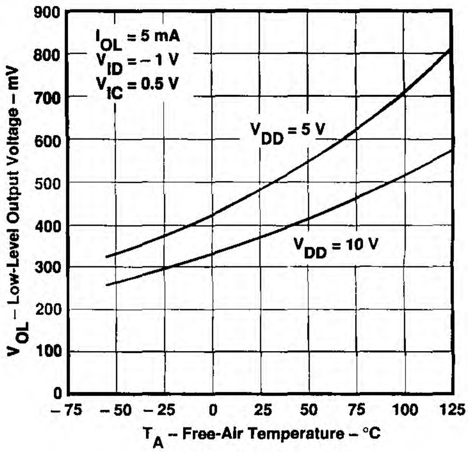

FIGURE 77

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

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TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

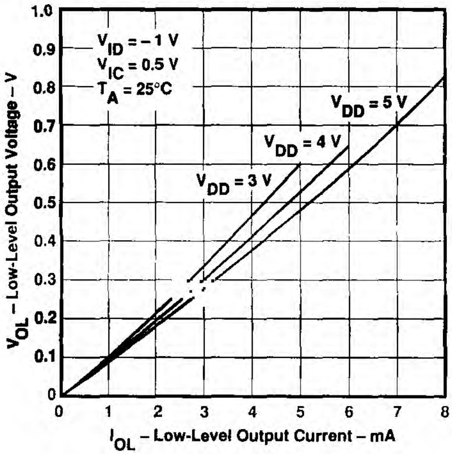


FIGURE 78

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

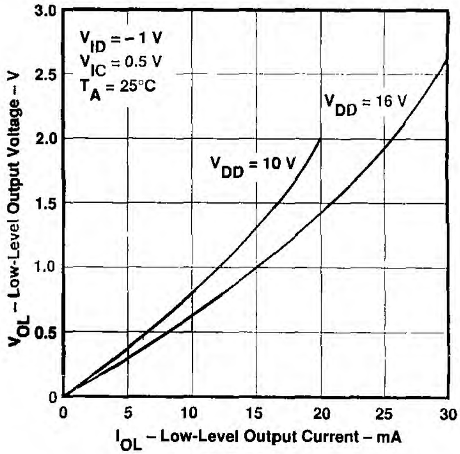


FIGURE 79

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

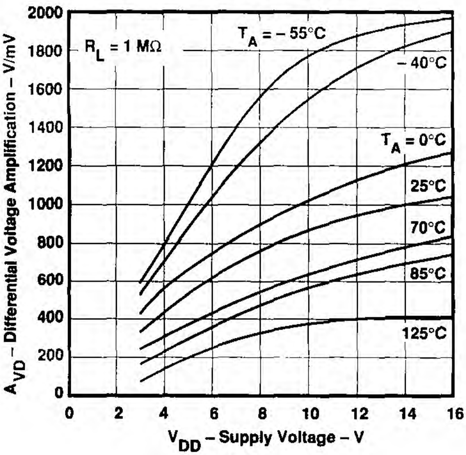


FIGURE 80

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

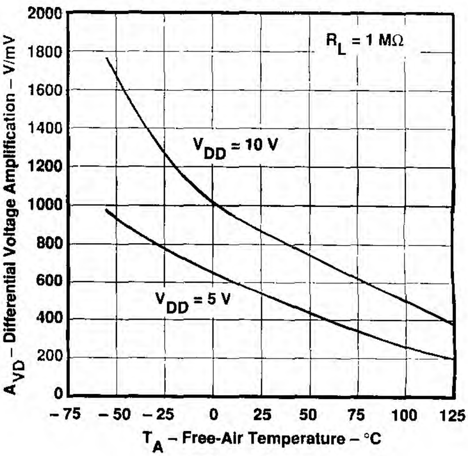


FIGURE 81

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

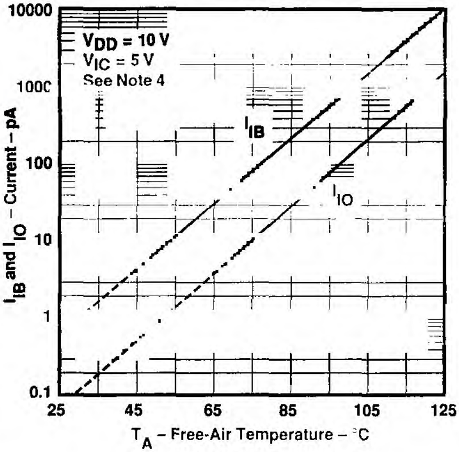


FIGURE 82

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

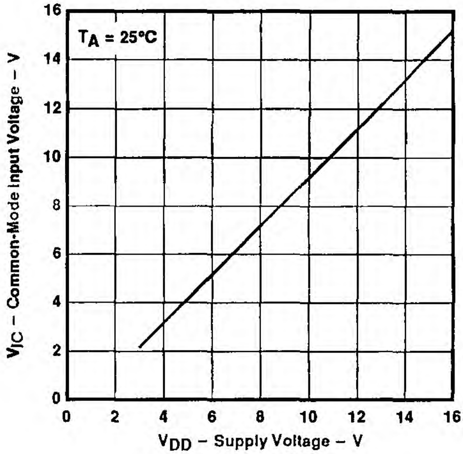


FIGURE 83

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

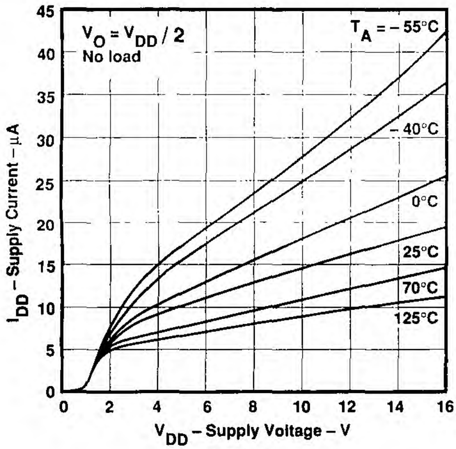


FIGURE 84

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

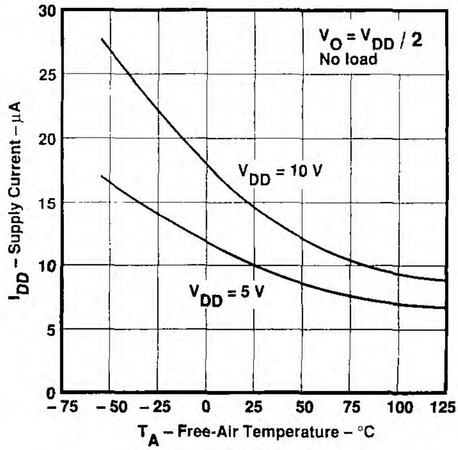


FIGURE 85

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

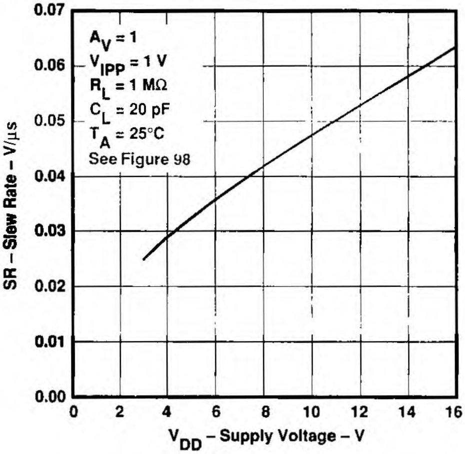


FIGURE 86

SLEW RATE
vs
FREE-AIR TEMPERATURE

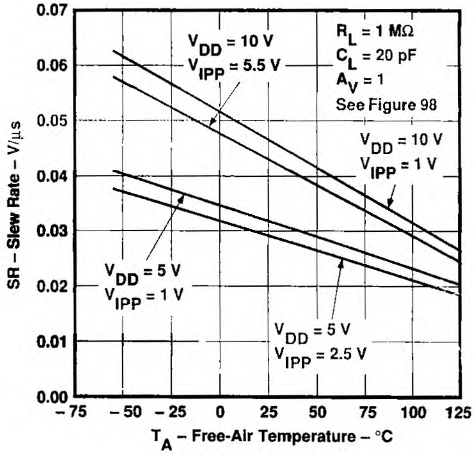


FIGURE 87

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

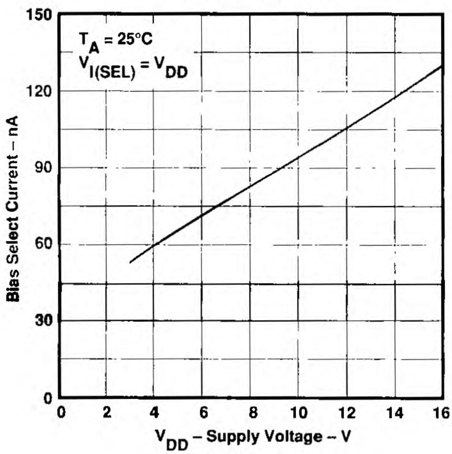


FIGURE 88

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

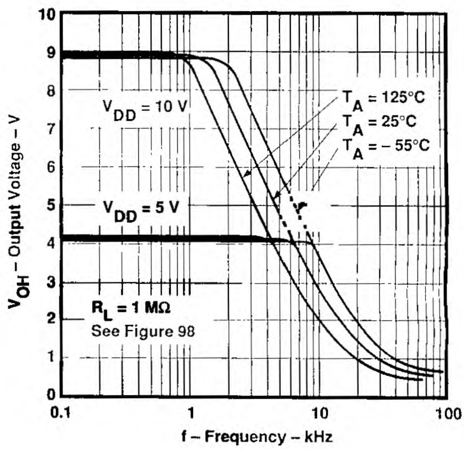


FIGURE 89

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

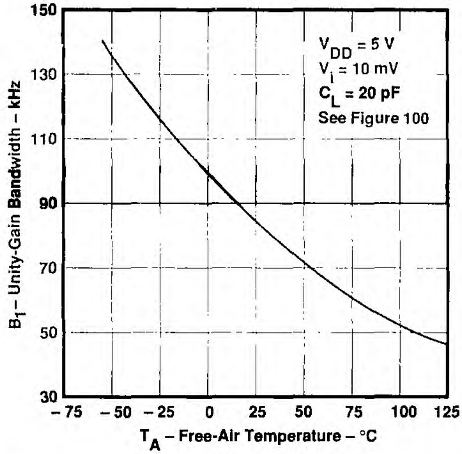


FIGURE 90

UNDITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

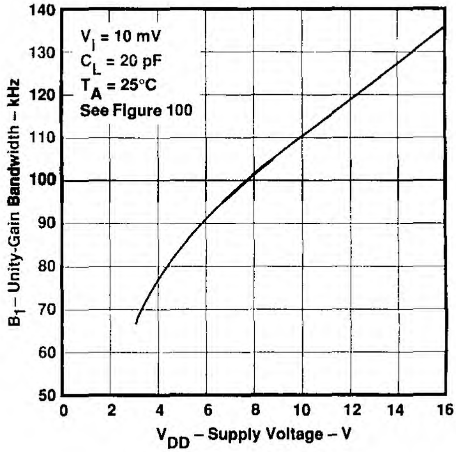


FIGURE 91

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

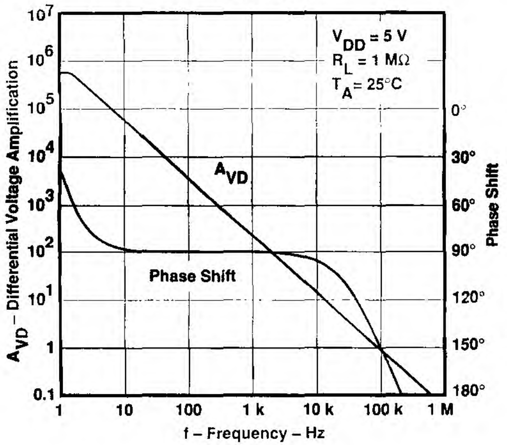


FIGURE 92

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

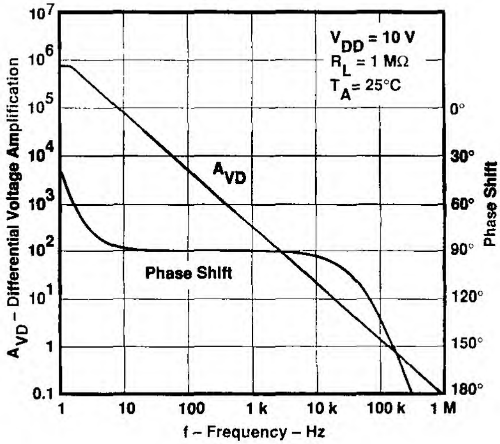


FIGURE 93

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

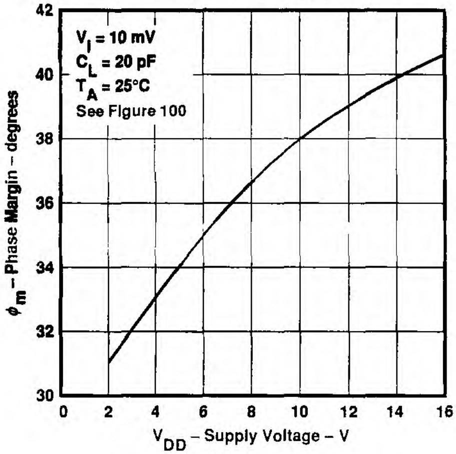


FIGURE 94

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

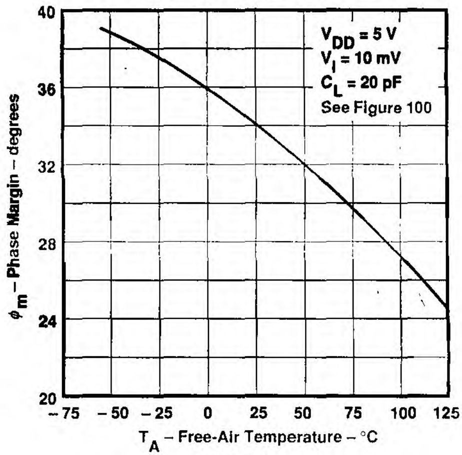


FIGURE 95

PHASE MARGIN
vs
CAPACITIVE LOAD

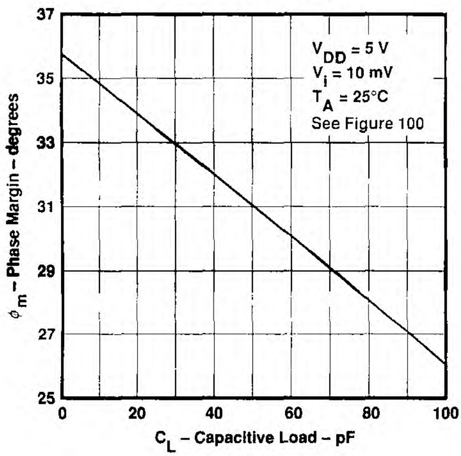


FIGURE 96

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

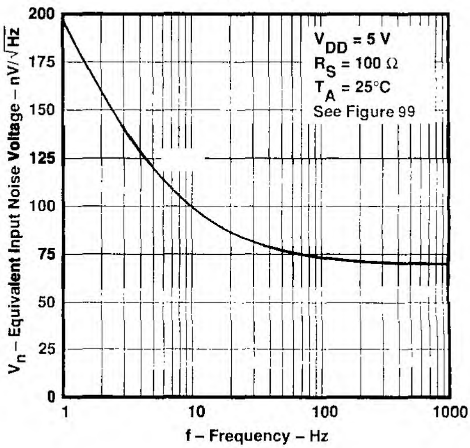


FIGURE 97

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

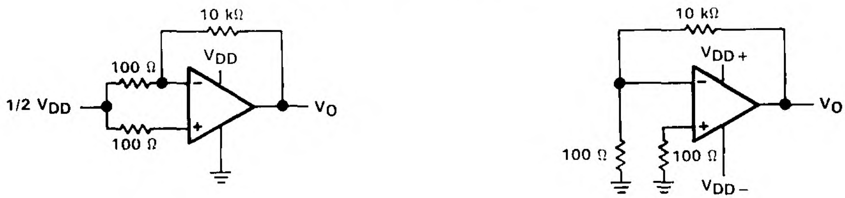
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

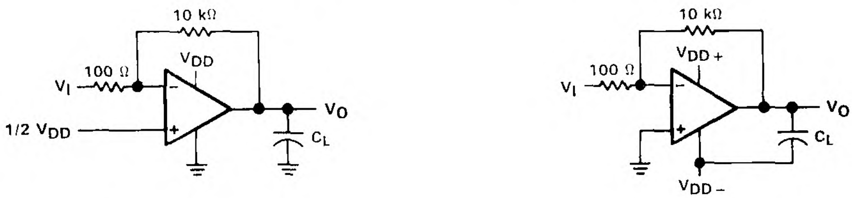
(a) Single-Supply (b) Split-Supply

FIGURE 98. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 99. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 100. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC271 op amp, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 101). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

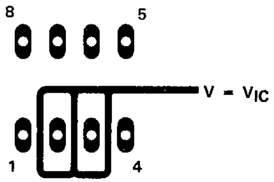


FIGURE 101. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 98. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 102). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

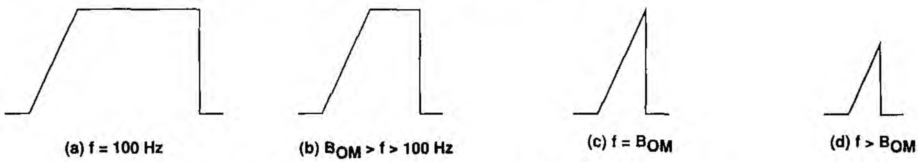


FIGURE 102. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

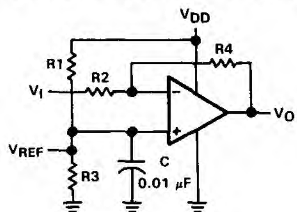
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC271 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 103). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 103. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

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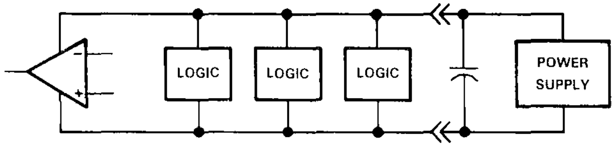
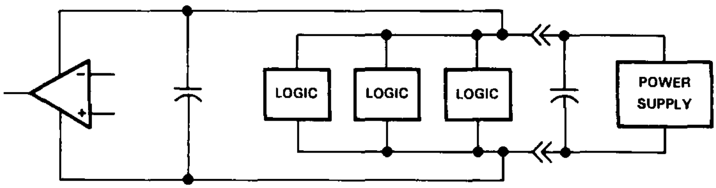
TYPICAL APPLICATION DATA

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 104); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



(a) Common Supply Rails

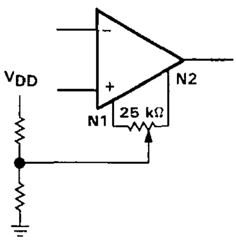


(b) Separate Bypassed Supply Rails (preferred)

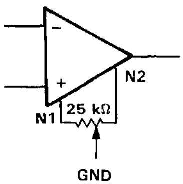
FIGURE 104. COMMON VERSUS SEPARATE SUPPLY RAILS

input offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 105. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.



(a) Single-Supply



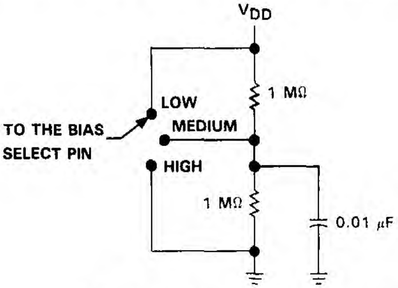
(b) Split-Supply

FIGURE 105. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 106). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
[illegible]	1 V to $V_{DD} - 1$ V
	GND

FIGURE 106. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 101 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 107).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

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TYPICAL APPLICATION DATA

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

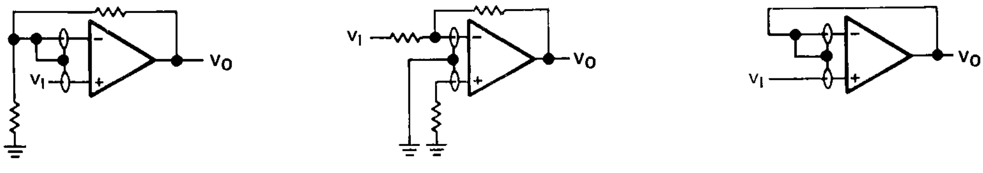


FIGURE 107. GUARD RING SCHEMES

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 108). The value of this capacitor is optimized empirically.

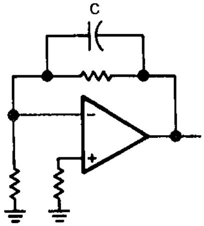


FIGURE 108. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC271 incorporates an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −110-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

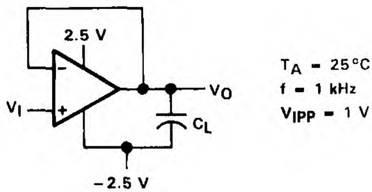
TYPICAL APPLICATION DATA

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

output characteristics

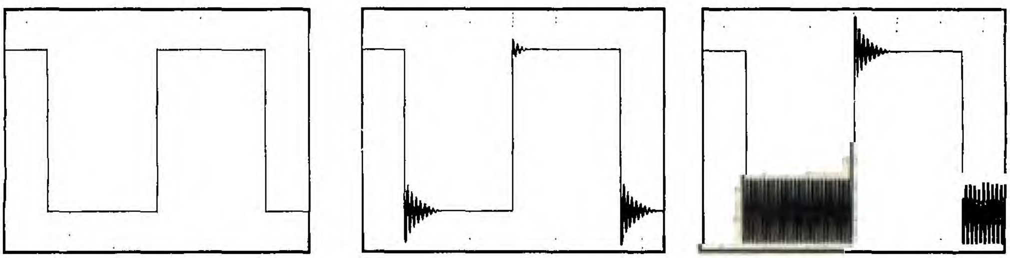
The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 110, 111, and 112). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



(d) Test Circuit

FIGURE 109. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS



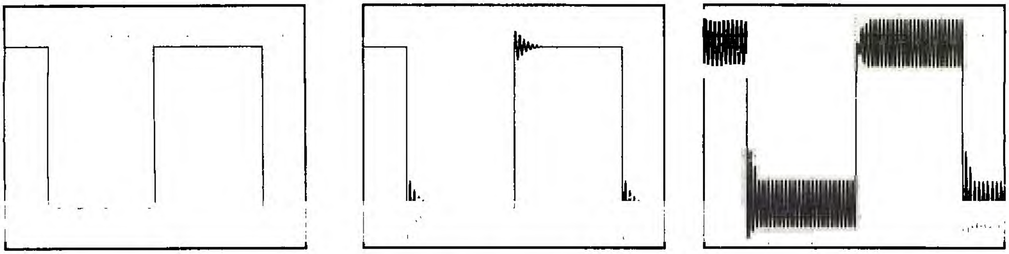
(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

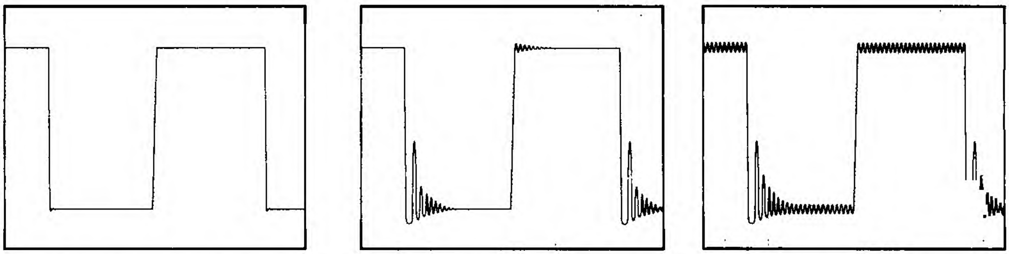
FIGURE 110. EFFECT OF CAPACITIVE LOADS IN HIGH-BIAS MODE

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

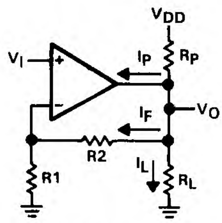
FIGURE 111. EFFECT OF CAPACITIVE LOADS IN MEDIUM-BIAS MODE



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

FIGURE 112. EFFECT OF CAPACITIVE LOADS IN LOW-BIAS MODE

Although the TLC271 possesses excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 113). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of Rp, a voltage offset from 0 V at the output will occur. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

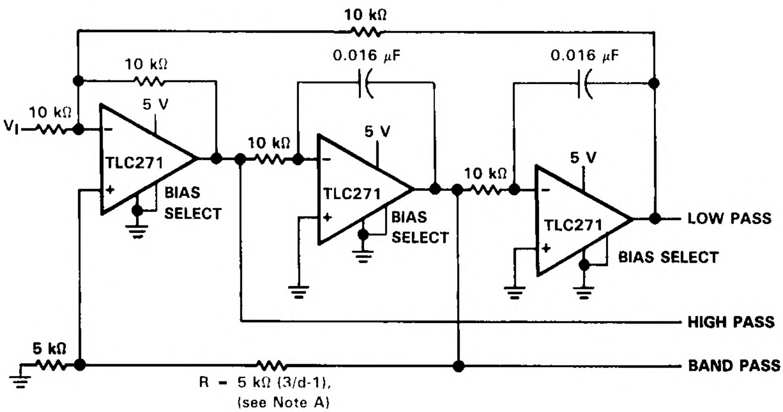


$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

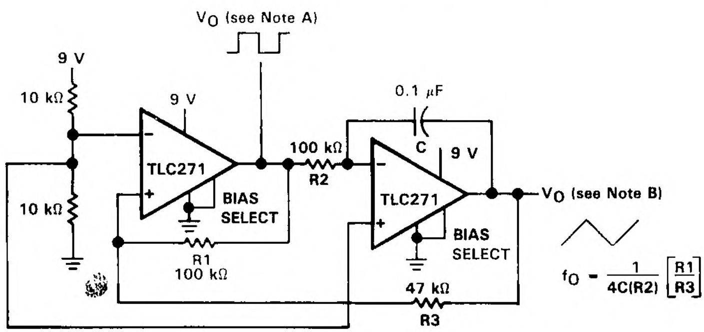
FIGURE 113. RESISTIVE PULLUP TO INCREASE V_{OH}

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 114. STATE VARIABLE FILTER



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 115. SINGLE-SUPPLY FUNCTION GENERATOR

2

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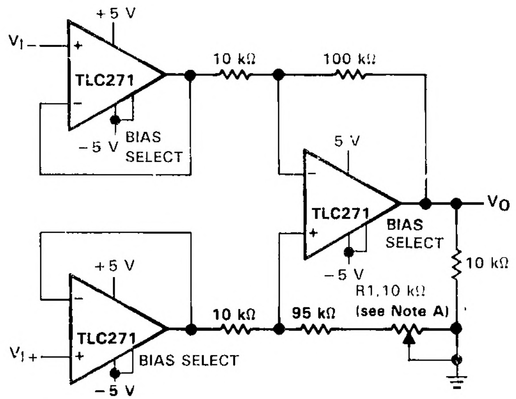
TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 116. LOW-POWER INSTRUMENTATION AMPLIFIER

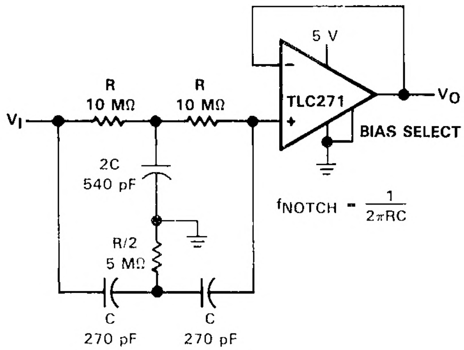
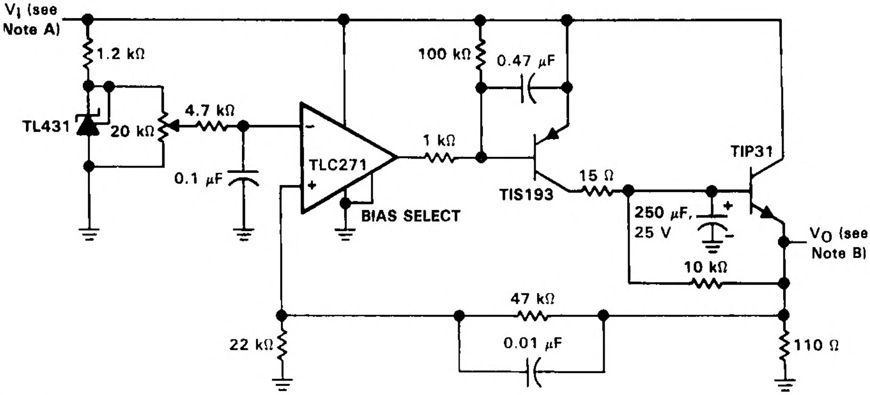


FIGURE 117. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 118. LOGIC-ARRAY POWER SUPPLY

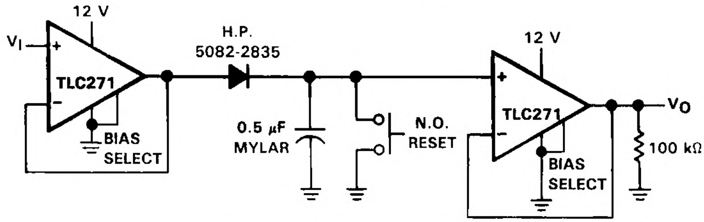
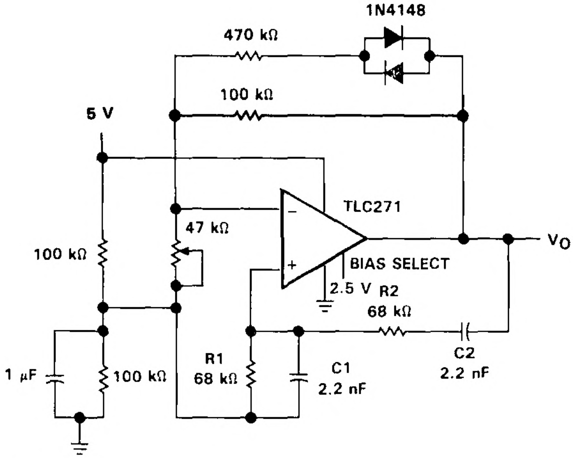


FIGURE 119. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 120. WIEN OSCILLATOR

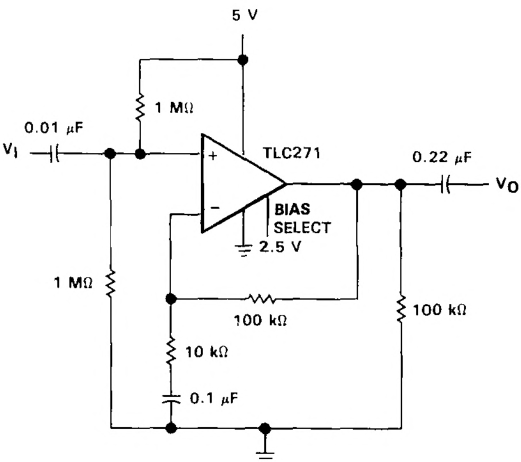
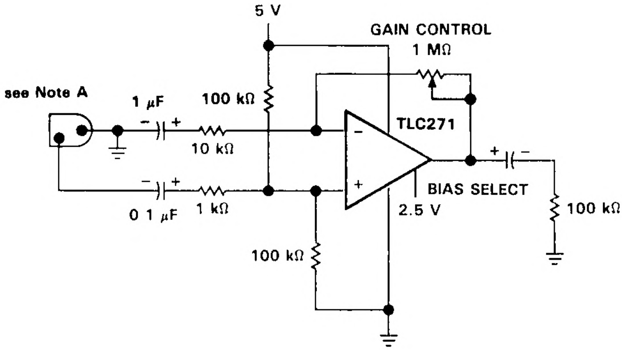


FIGURE 121. SINGLE-SUPPLY AC AMPLIFIER

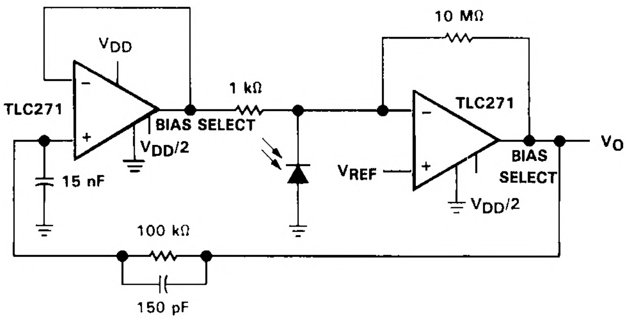
2
Operational Amplifiers

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTE A.: Low to medium impedance dynamic mike

FIGURE 122. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 123. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

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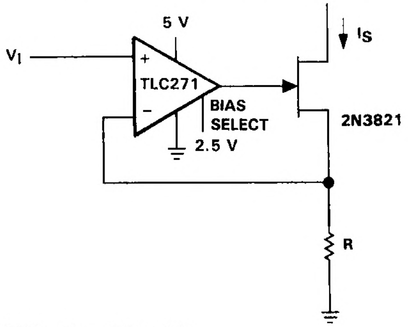
TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



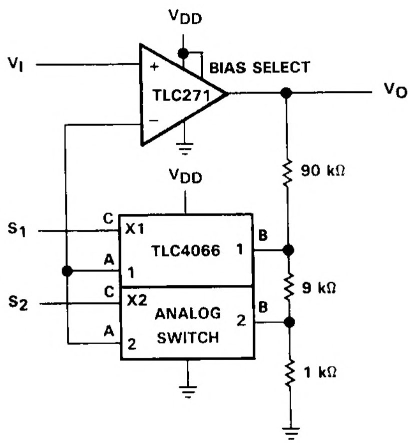
NOTES: V_I = 0 V to 3 V

$$I_S = \frac{V_I}{R}$$

FIGURE 124. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA (LOW-BIAS MODE)

SELECT:	S_1	S_2
A_V	10	100



NOTE. V_{DD} = 5 V to 12 V

FIGURE 125. AMPLIFIER WITH DIGITAL GAIN SELECTION

TYPICAL APPLICATION DATA (LOW-BIAS MODE)

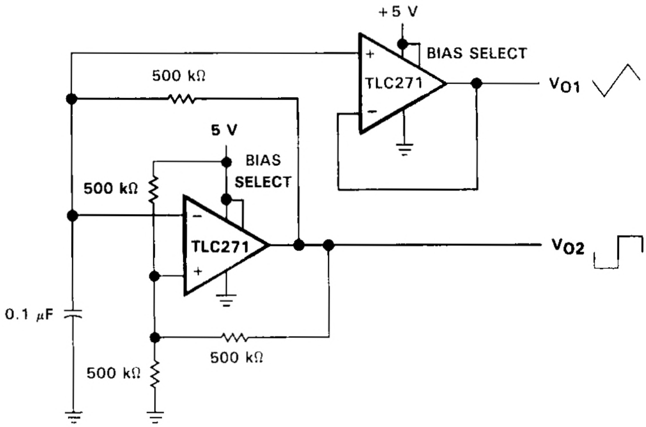
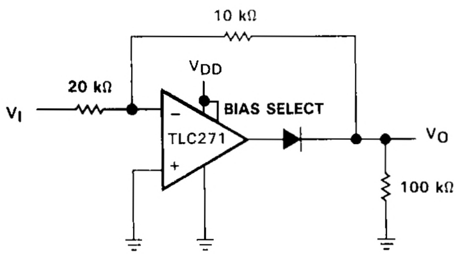


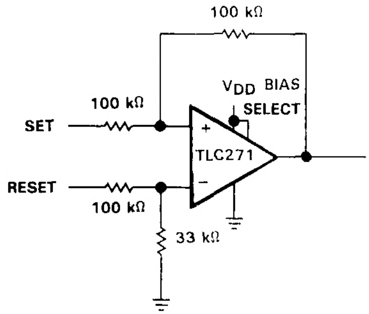
FIGURE 126. MULTIVIBRATOR



NOTE V_{DD} = 5 V to 16 V

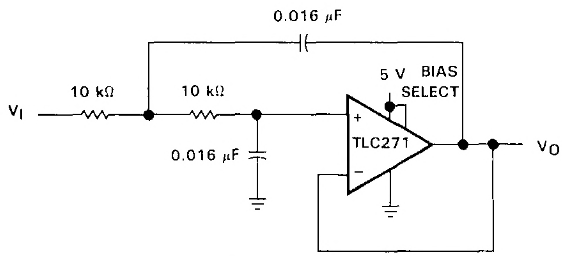
FIGURE 127. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



NOTE. V_{DD} = 5 V to 16 V

FIGURE 128. SET/RESET FLIP-FLOP



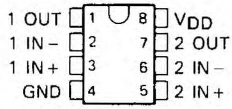
NOTE Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 129. TWO-POLE LOW-PASS BUTTERWORTH FILTER

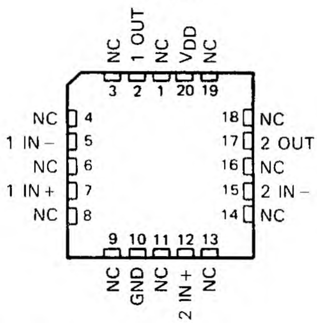
D3138, OCTOBER 1987—REVISED MARCH 1989

- Trimmed Offset Voltage: TLC277 . . . 500 μV Max at 25 °C, V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/$\sqrt{Hz}$ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latchup Immunity

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



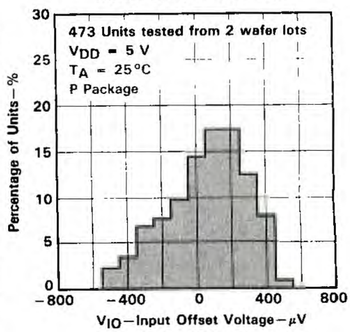
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	[illegible]V	TLC277CD	—	TLC277CJG	TLC277CP
	[illegible] mV	TLC272BCD	—	TLC272BCJG	T[illegible]2BCP
	5 mV	TLC272ACD	—	TLC272ACJG	T[illegible]
	10 mV	TLC2[illegible]	—	T[illegible]2CJG	T[illegible]2CP
−40°C to 85°C	500 μV	TLC2[illegible]	—	T[illegible]	TLC277IP
	2 mV	TLC272BID	—	T[illegible]	TLC272BIP
	5 mV	TLC272AID	—	T[illegible]JG	TLC2[illegible]
	10 mV	TLC272ID	—	TLC272IJG	TLC2[illegible]
−55°C to 125°C	500 μV	—	TLC277MFK	TLC277MJG	—
	10 mV	—	TLC272MFK	TLC272MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC277CDR).

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



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description

The TLC272 and TLC277 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

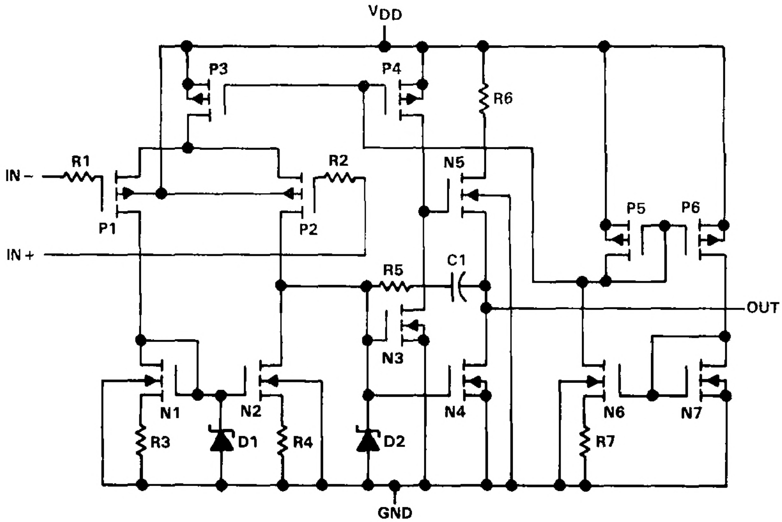
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	−55°C to 125°C
I-suffix	−40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		[illegible]	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				F[illegible]			12	
		TLC277M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	[illegible]		200	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				[illegible]C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		1.4	3.2	mA
				−55°C		2	5	
				125°C		1	2.2	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	mV
		TLC277M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		250	800	μV
					Full range			4300	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		V
					125°C	7.8	8.4		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	mV
					125°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		V/mV
					125°C	7	27		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−55°C	60	87		dB
					125°C	60	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		dB
					125°C	60	97		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−55°C		3	6	mA
					[illegible]C		1.3	2.8	mA

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC272AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC272BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	[illegible]	μV
				Full range			[illegible]	μV
		TLC277I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	[illegible]	μV
				Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−40°C	3	3.8		V
				85°C	3	3.8		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	mV
				85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−40°C	3.5	32		V/mV
				85°C	3.5	19		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				−40°C	60	81		dB
				85°C	60	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−40°C	60	92		dB
				85°C	60	96		dB
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		1.4	3.2	mA
				−40°C		1.9	4.4	mA
				85°C		1.1	2.4	mA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	mV
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	mV
					Full [illegible]			7	mV
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		290	[illegible]	μV
					Full [illegible]			[illegible]	μV
		TLC277I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		250	800	μV
					Full range			2900	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		V
					85°C	7.8	8.5		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	mV
					85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	46		V/mV
					85°C	7	31		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		dB
					85°C	60	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		dB
					85°C	60	96		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−40°C		2.8	5	mA
					85°C		1.5	3.2	mA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full [illegible]			12	mV
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		0.9	5	mV
					Full [illegible]			6.5	mV
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		230	2000	μV
					Full [illegible]			3000	μV
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		200	500	μV
					Full range			1500	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		V
					70°C	3	3.8		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	mV
					70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		V/mV
					70°C	4	20		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					0°C	60	84		dB
					70°C	60	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		dB
					70°C	60	96		dB
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	mA
					70°C		1.2	2.6	mA

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full [illegible]			12	mV
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		0.9	5	mV
					F[illegible]			[illegible]	mV
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		290	[illegible]	μV
					F[illegible]			[illegible]	μV
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		[illegible]	[illegible]	μV
					Full range			1900	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		V
					70°C	7.8	8.4		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	mV
					70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		V/mV
					70°C	7.5	32		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					0°C	60	88		dB
					70°C	60	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		dB
					70°C	60	96		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					0°C		2.3	4.4	mA
					70°C		1.6	3.4	mA

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				[illegible]		3.1		
			V_{IPP} = 5.5 V	[illegible]		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				[illegible]		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	[illegible]		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		[illegible]		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		[illegible]		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		[illegible]		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		[illegible]		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

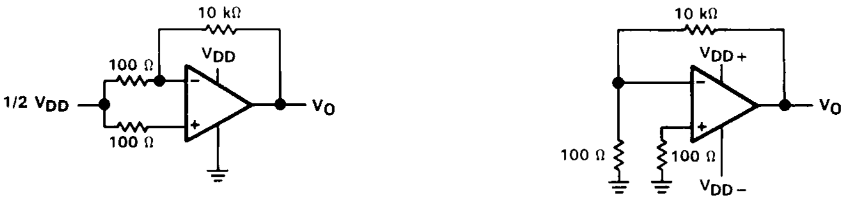
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

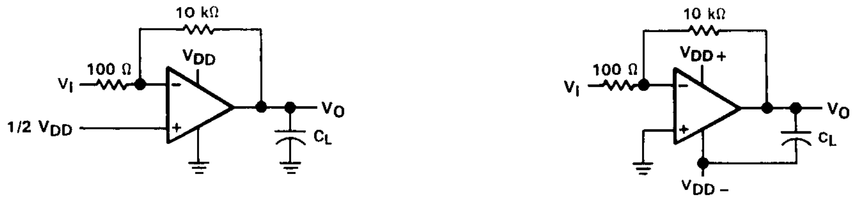
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

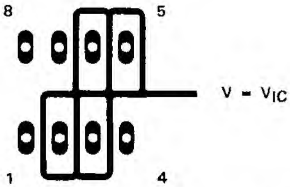


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

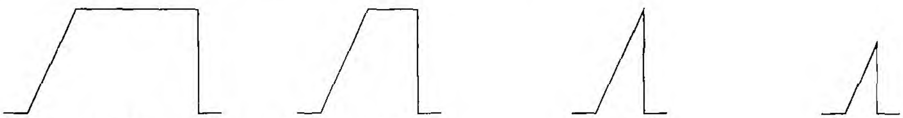
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) $f = 1$ kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

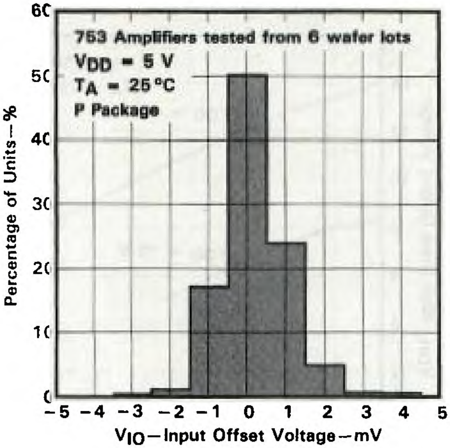


FIGURE 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

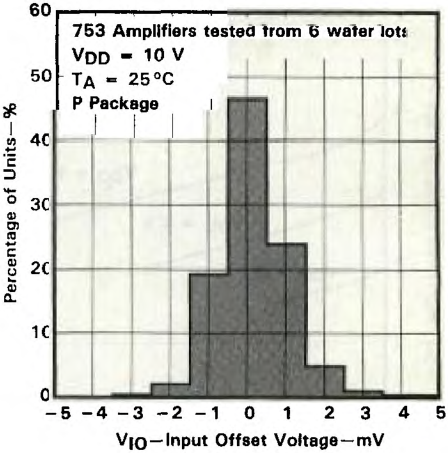


FIGURE 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

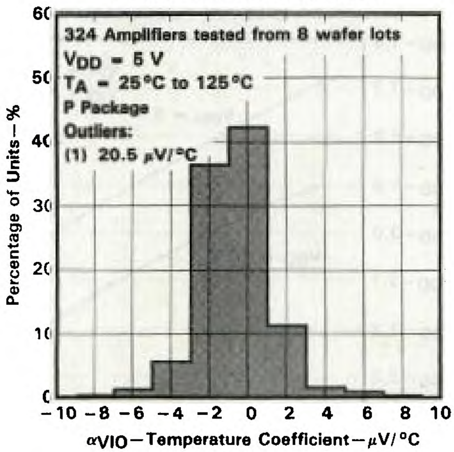


FIGURE 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

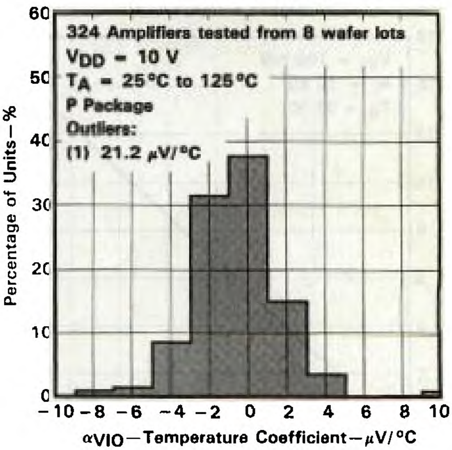


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

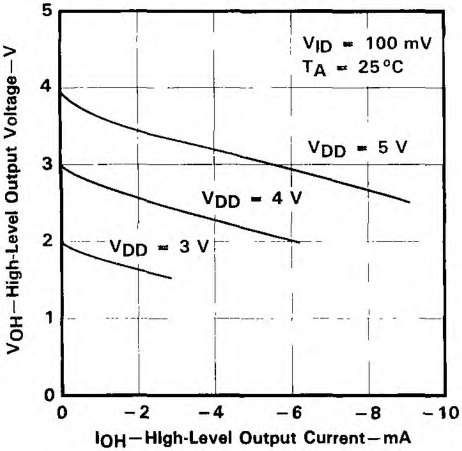


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

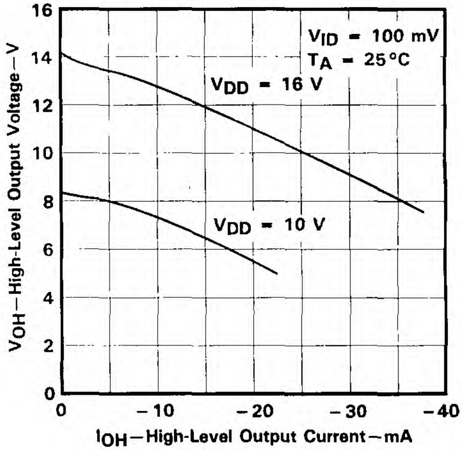


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

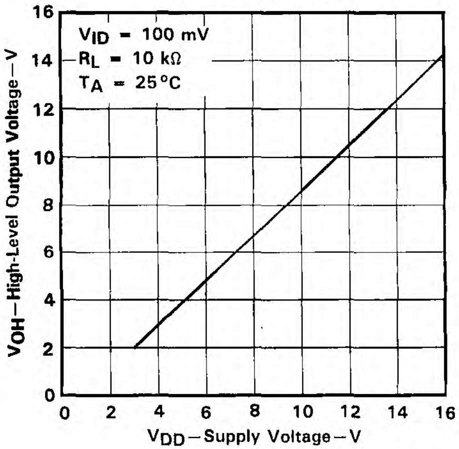


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

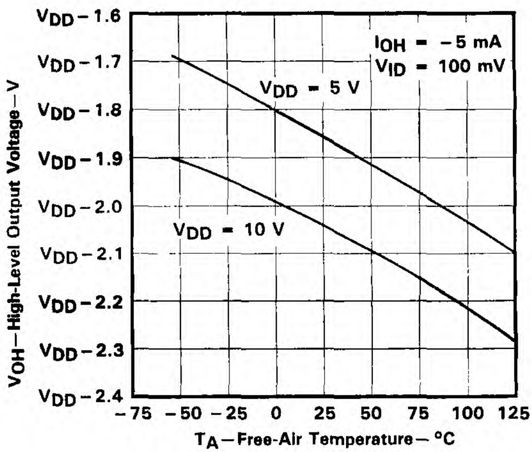


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

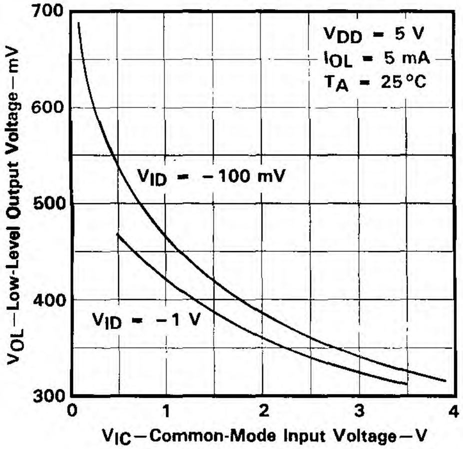


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

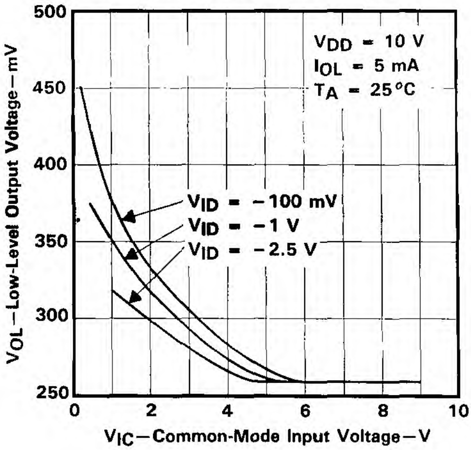


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

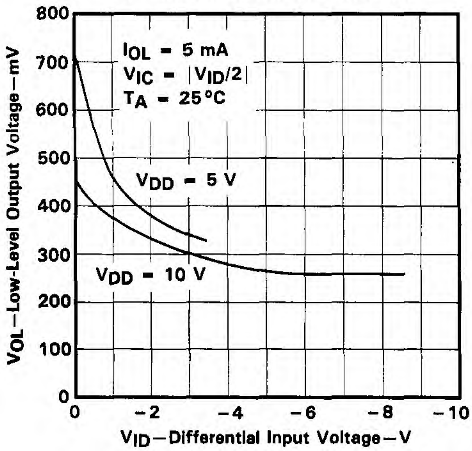


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

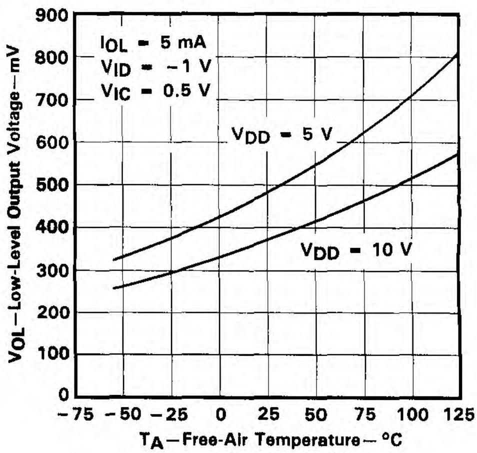


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

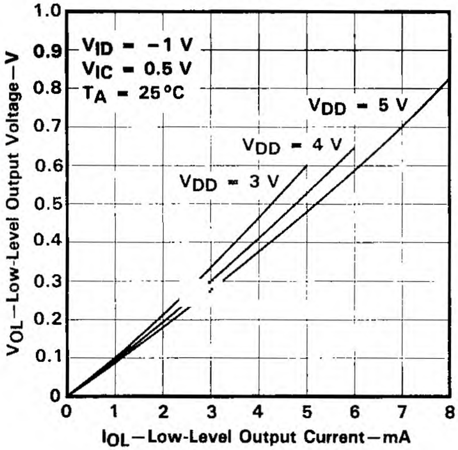


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

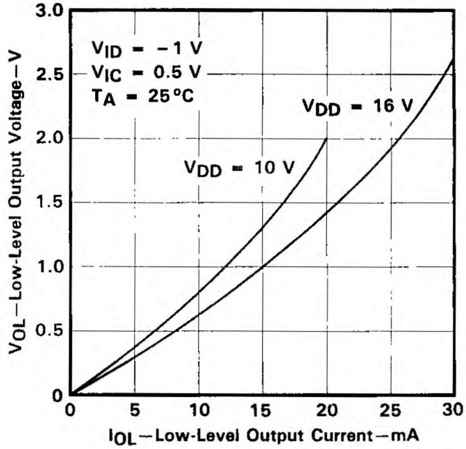


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

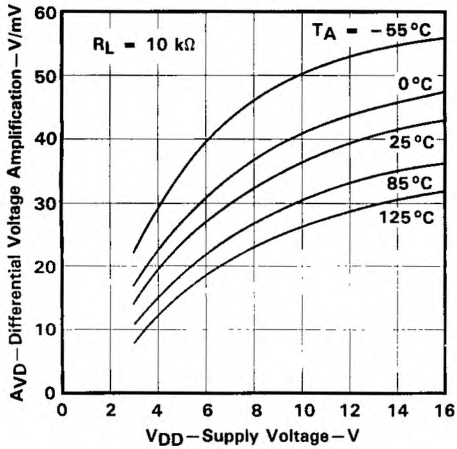


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

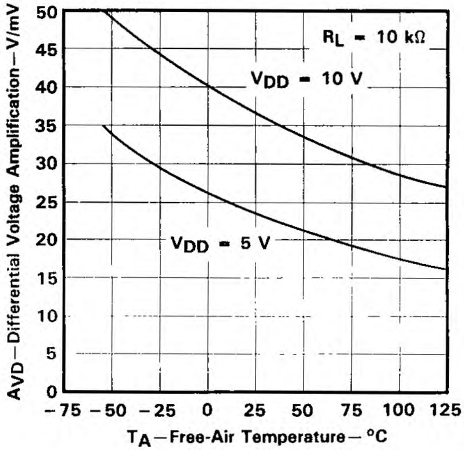


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

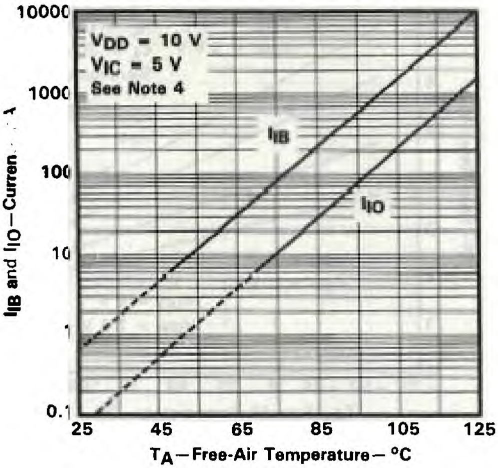


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

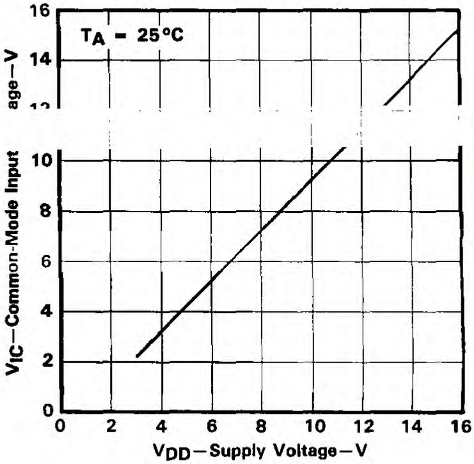


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

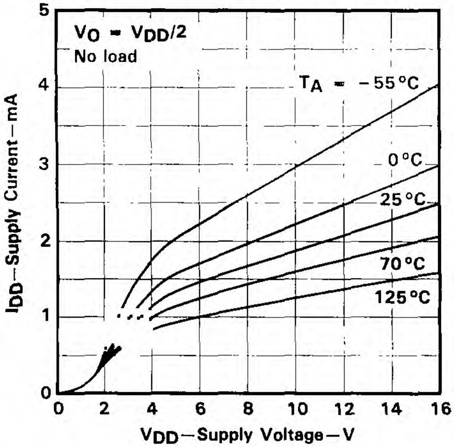


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

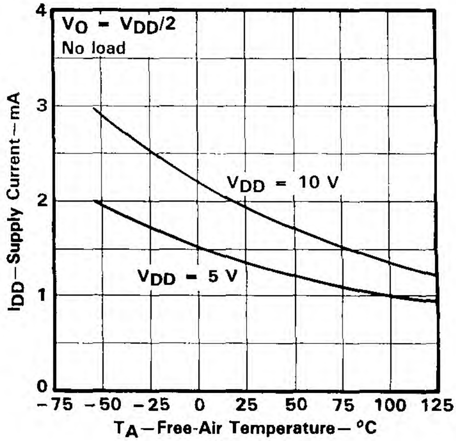


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

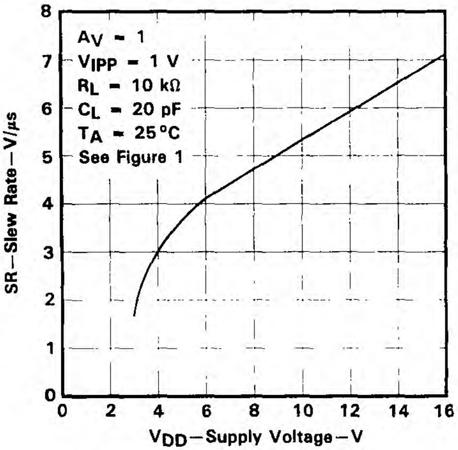


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

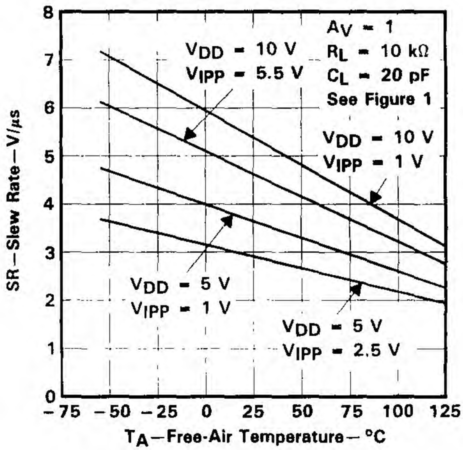


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

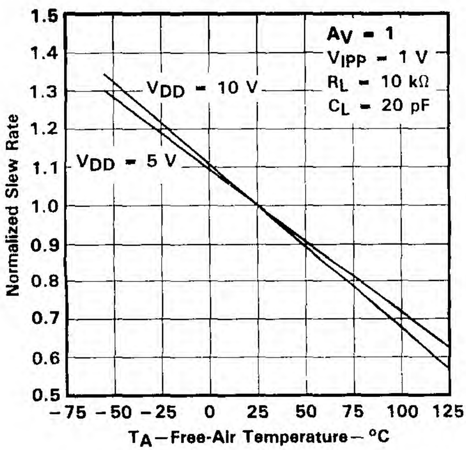


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

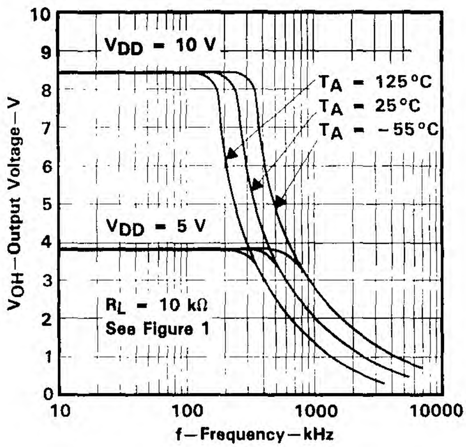


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

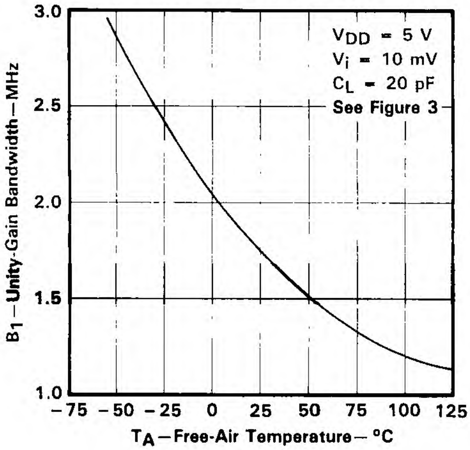


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

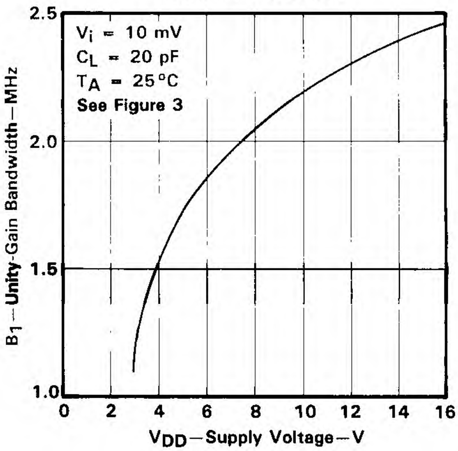


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

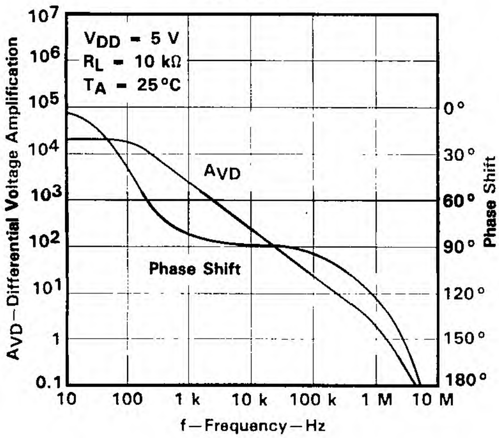


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

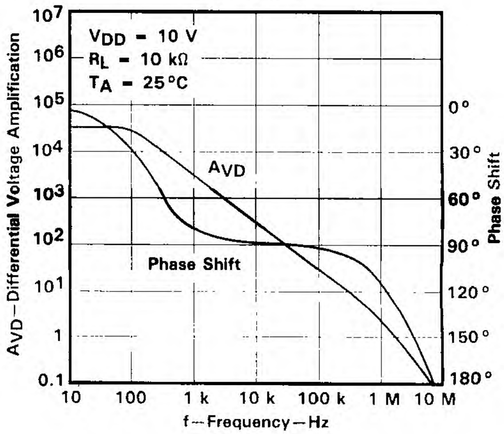


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

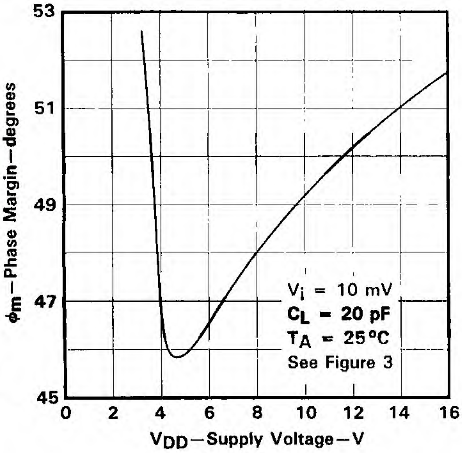


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

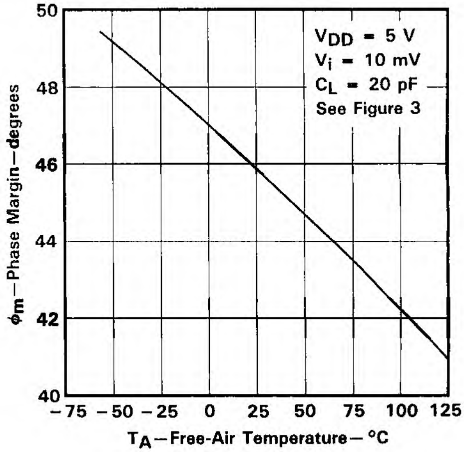


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

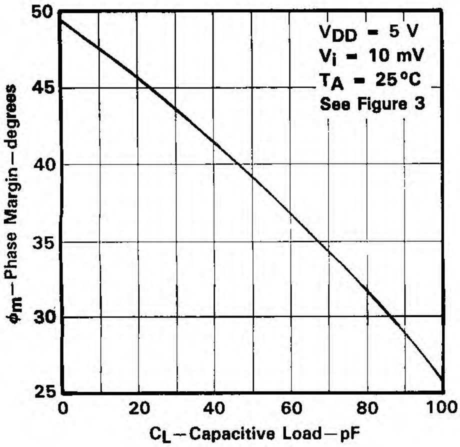


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

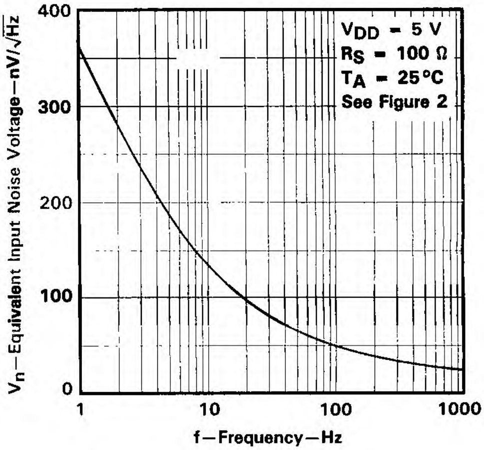


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL APPLICATION DATA

single-supply operation

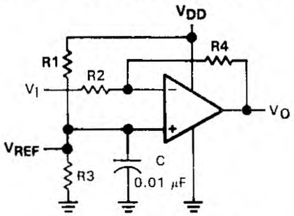
While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.

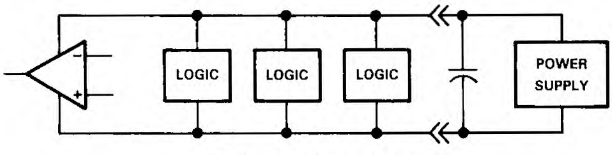
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



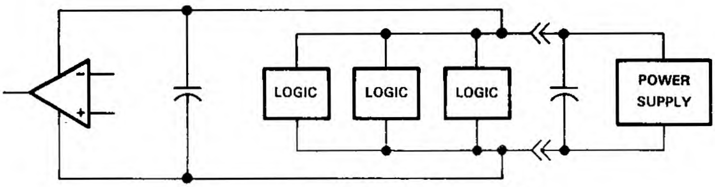
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25$°C and at $V_{DD} - 1.5$ V at all other temperatures.

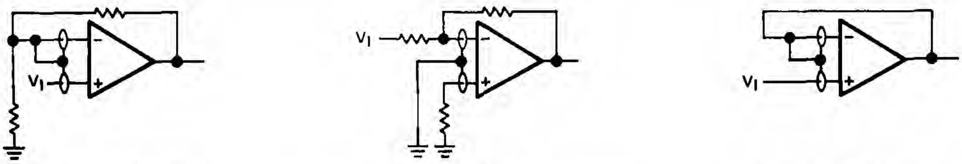
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

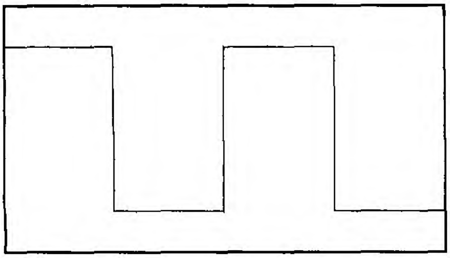
FIGURE 40. GUARD-RING SCHEMES

output characteristics

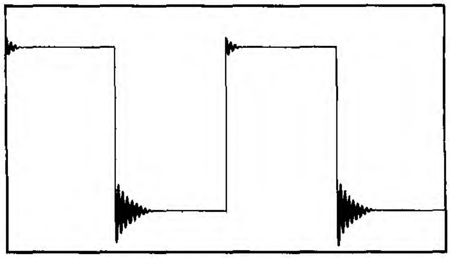
The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

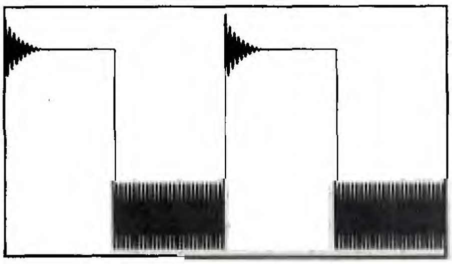
TYPICAL APPLICATION DATA



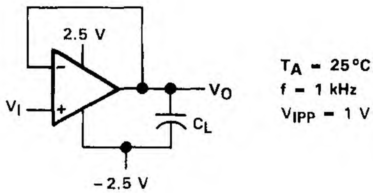
(a) C_L = 20 pF, R_L = No load



(b) C_L = 130 pF, R_L = No load



(c) C_L = 150 pF, R_L = No load



(d) Test Circuit

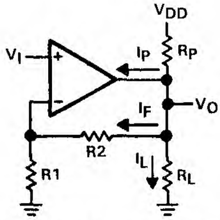
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

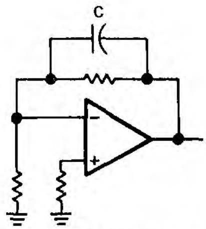


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

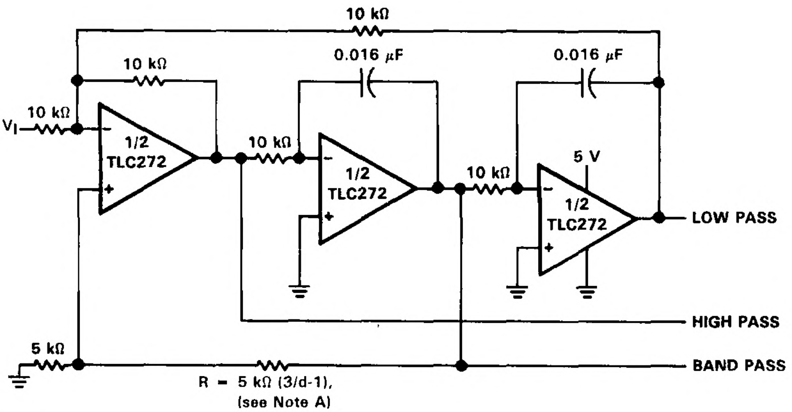
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

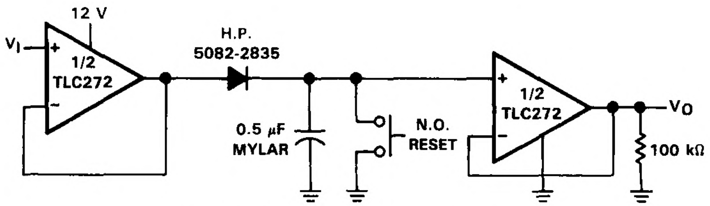
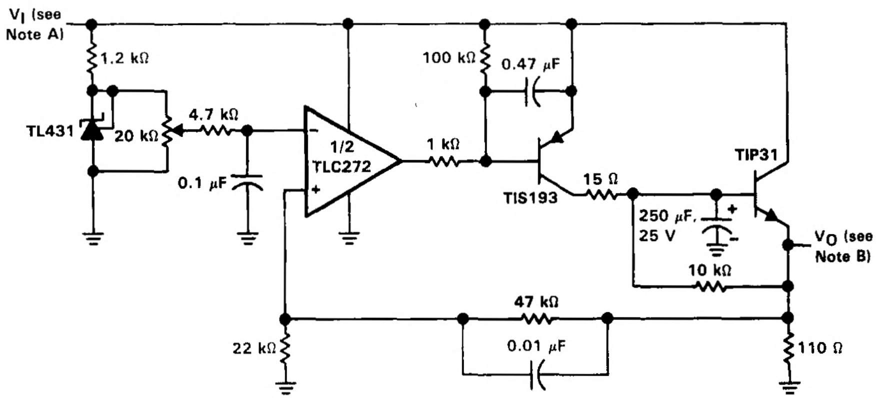


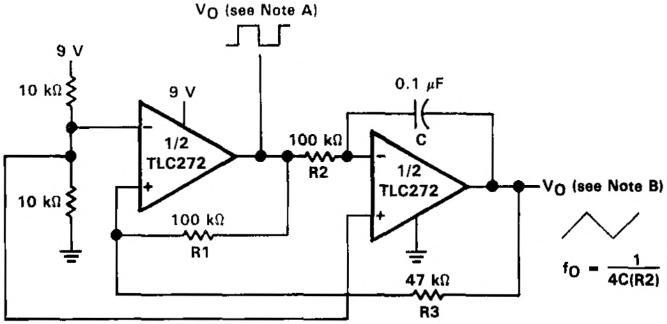
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 46. LOGIC ARRAY POWER SUPPLY



$$f_O = \frac{1}{4C(R2)}\left[\frac{R1}{R3}\right]$$

NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

2 Operational Amplifiers

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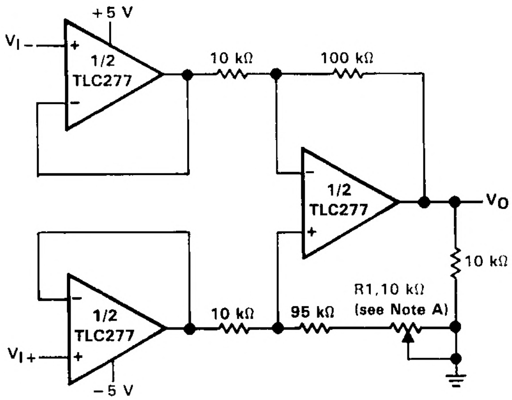
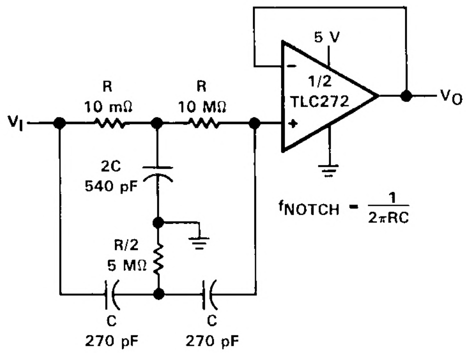
TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER



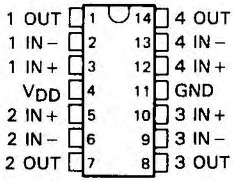
$$f_{NOTCH} = \frac{1}{2\pi RC}$$

FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

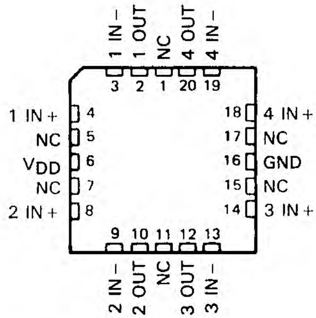
D3141, SEPTEMBER 1987—REVISED AUGUST 1988

- Trimmed Offset Voltage:
  TLC279 . . . 900 μV Max at 25 °C,
  V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  −55 °C to 125 °C . . . 4 V to 16 V
  −40 °C to 85 °C . . . 4 V to 16 V
  0 °C to 70 °C . . . 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latchup Immunity

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



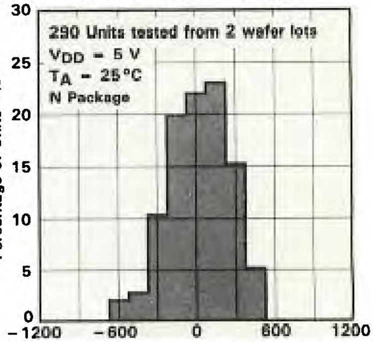
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25 °C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0 °C to 70 °C	900 μV	TLC279CD	—	[illegible]	[illegible]
	2 mV	[illegible]	—	[illegible]	[illegible]
	5 mV	[illegible]	—	[illegible]	[illegible]
	10 mV	[illegible]	—	[illegible]	[illegible]
−40 °C to 85 °C	900 μV	[illegible]	—	TLC279IJ	[illegible]
	2 mV	[illegible]	—	[illegible]	[illegible]
	5 mV	[illegible]	—	[illegible]	[illegible]
	10 mV	[illegible]	—	TLC274IJ	TLC274IN
−55 °C to 125 °C	900 μV	—	TLC279MFK	TLC279MJ	—
	10 mV	—	TLC274MFK	TLC274MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC279CDR).

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



2
Operational Amplifiers

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description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

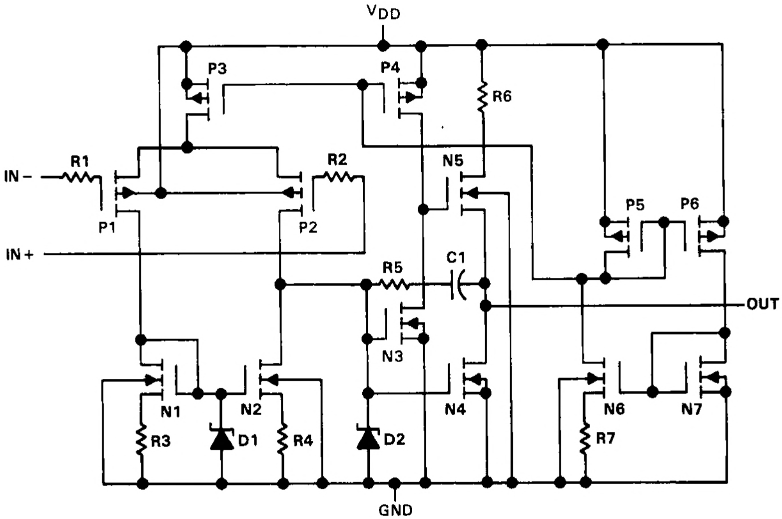
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	−55°C to 125°C
I-suffix	−40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		[illegible]	
Operating free-air temperature, T_A		−55		125	−40		85	0		[illegible]	°C

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	[illegible]	μV
				Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				[illegible]	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	[illegible]		2.7	6.4	mA
				−55°C		4	10	
				[illegible]		1.9	4.4	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	[illegible]		370	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				−55°C	7.8	8.5		
				125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				−55°C	7	50		
				125°C	7	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				−55°C	60	87		
				125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				−55°C		6.0	12	
				125°C		2.5	5.6	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		340	[illegible]	μV
					Full [illegible]			[illegible]	
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		[illegible]	[illegible]	
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		[illegible]	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	[illegible] to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					−40°C		3.8	8.8	
					85°C		2.1	4.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	mV
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	mV
					Full range			7	mV
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		390	2000	µV
					Full range			[illegible]	µV
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		370	[illegible]	µV
					Full range			[illegible]	µV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		V
					85°C	7.8	8.5		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	mV
					85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	47		V/mV
					85°C	7	31		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		dB
					85°C	60	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		dB
					85°C	60	96		dB
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					−40°C		5.5	10	mA
					85°C		2.9	6.4	mA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full [illegible]			12	mV
		TLC274AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		0.9	5	mV
					Full [illegible]			6.5	mV
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		340	2000	μV
					Full [illegible]			3000	μV
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	[illegible]		[illegible]	[illegible]	μV
					Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7		pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		V
					70°C	3	3.8		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	mV
					70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		V/mV
					70°C	4	20		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					0°C	60	84		dB
					70°C	60	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		dB
					70°C	60	96		dB
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					0°C		3.1	7.2	mA
					70°C		2.3	5.2	mA

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC274AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		390	[illegible]	μV
					Full range			[illegible]	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		370	1200	
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					0°C		4.5	8.8	
					70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				[illegible] C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				[illegible] C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, $V_{DD} = 5$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10$ kΩ, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			$V_{IPP} = 2.5$ V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 100$ Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, $R_L = 10$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		[illegible]		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	$V_i = 10$ mV, $C_L = 20$ pF,	$f = B_1$, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, $V_{DD} = 10$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10$ kΩ, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		5.3		V/μs
				−40°C		6.7		
				85°C		4		
			$V_{IPP} = 5.5$ V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 100$ Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, $R_L = 10$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	$V_i = 10$ mV, $C_L = 20$ pF,	$f = B_1$, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

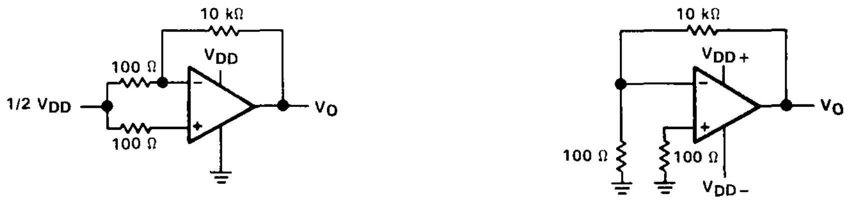
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

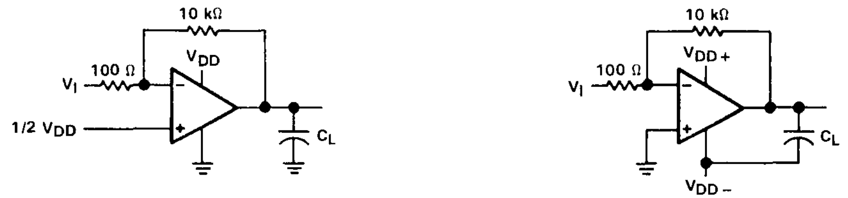
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

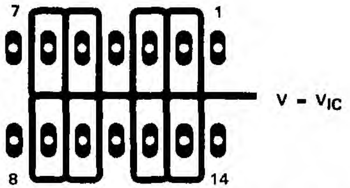

FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

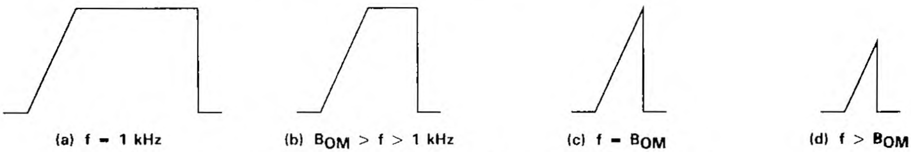

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

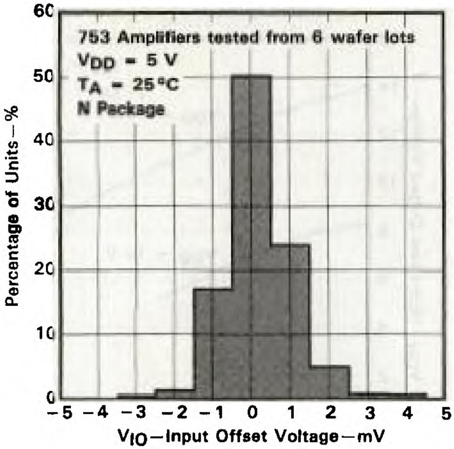

FIGURE 6

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

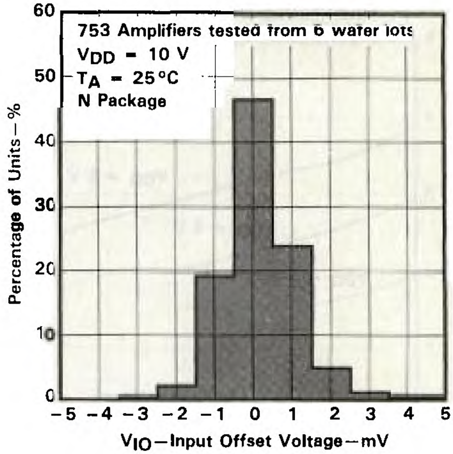

FIGURE 7

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

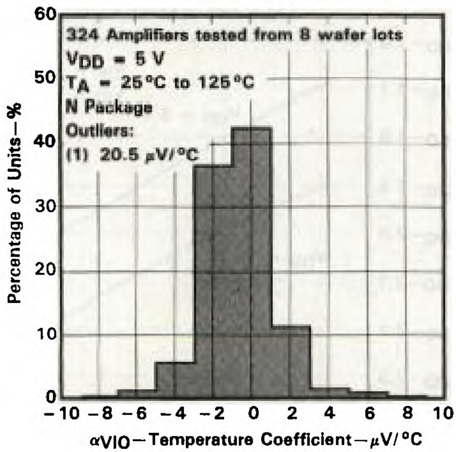

FIGURE 8

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

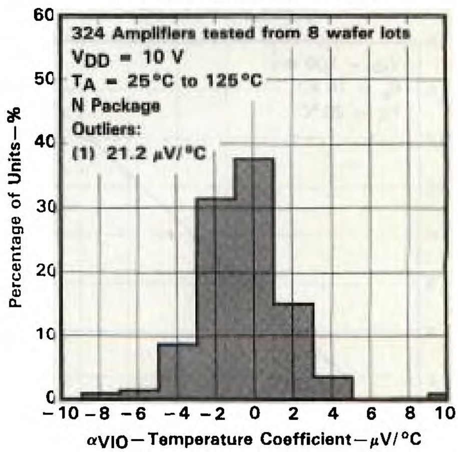

FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

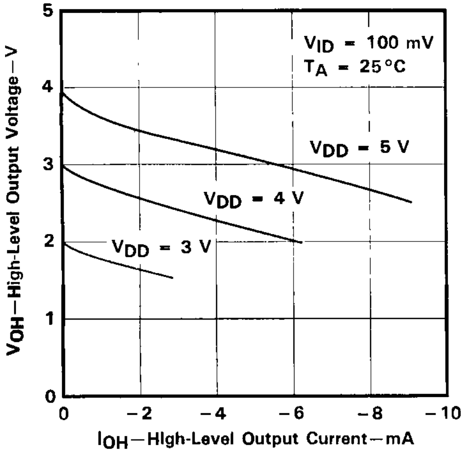

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

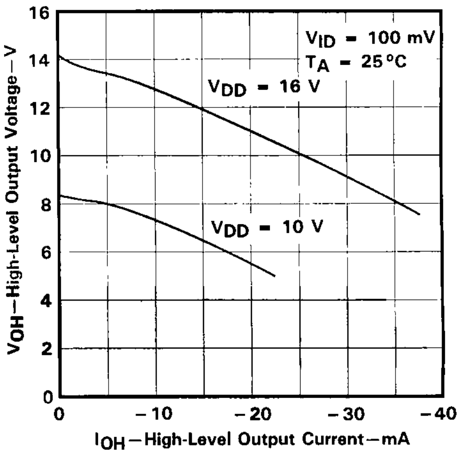

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

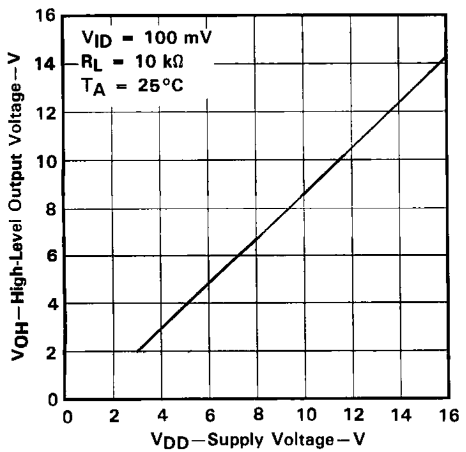

FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

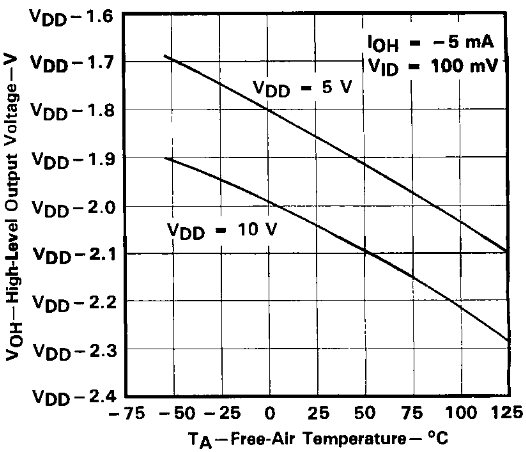

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

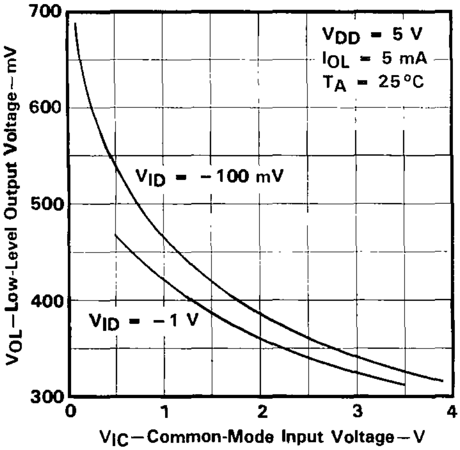

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

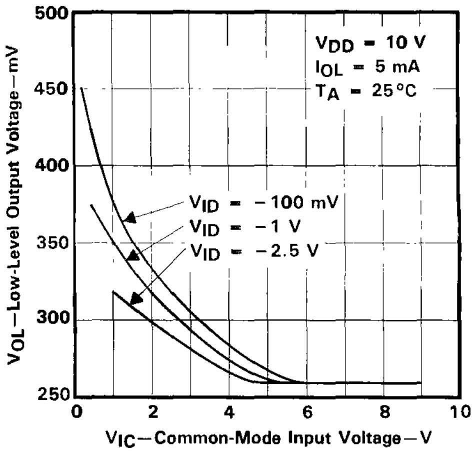

FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

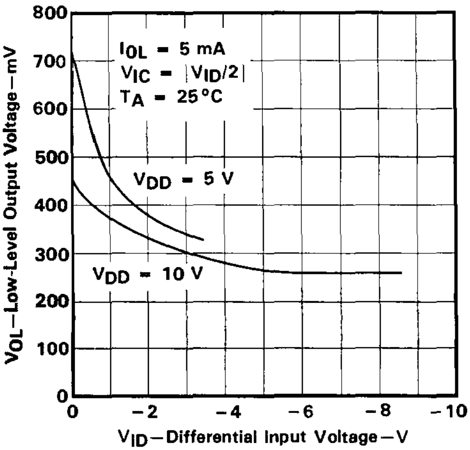

FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

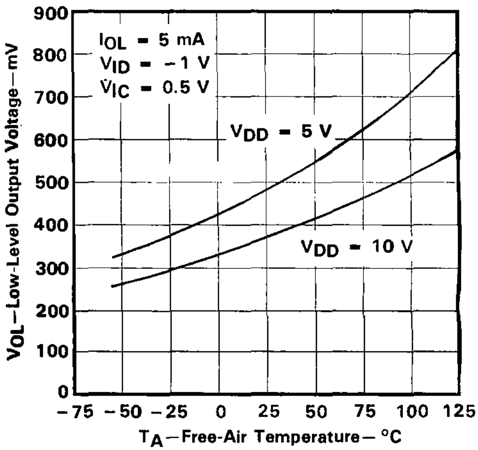

FIGURE 17

2 Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

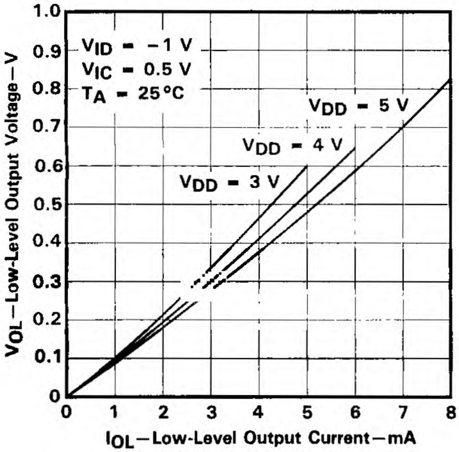

FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

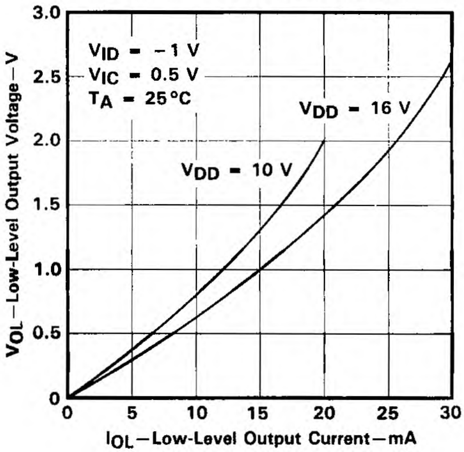

FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

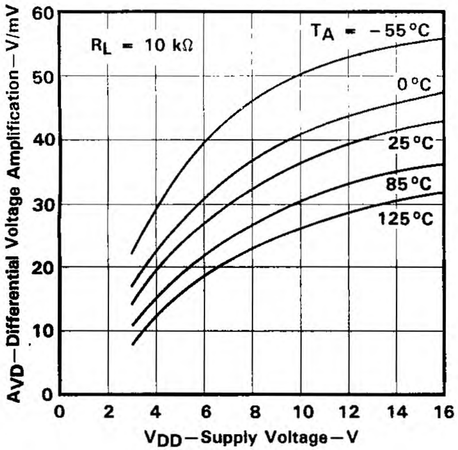

FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

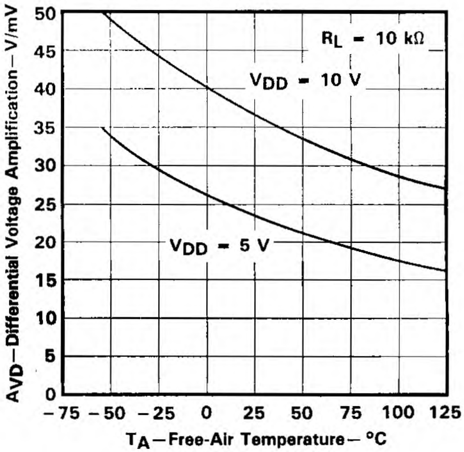

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

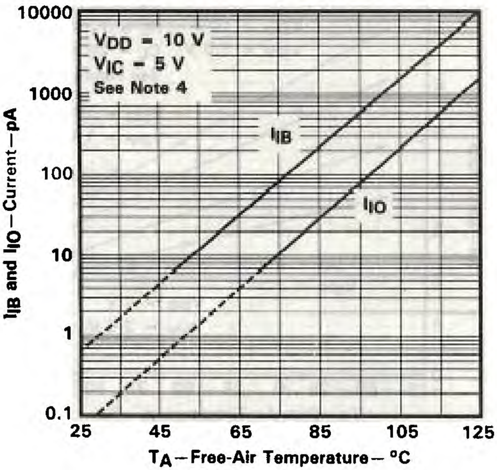

FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

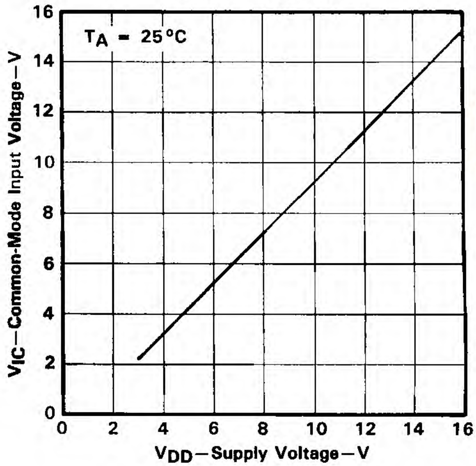

FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

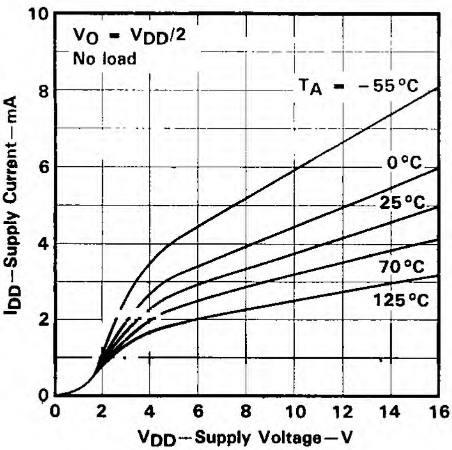

FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

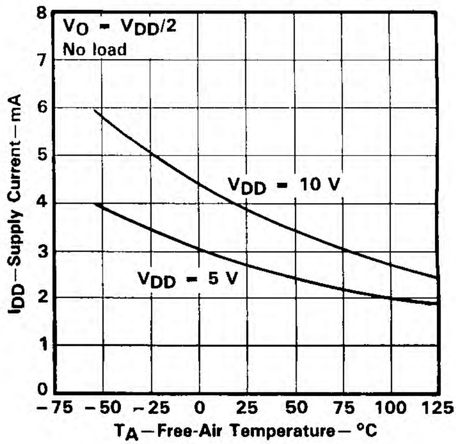

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

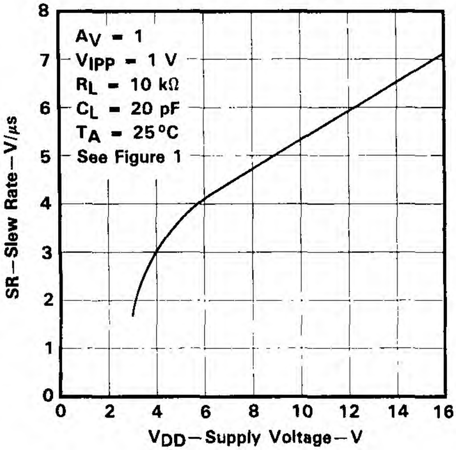

FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

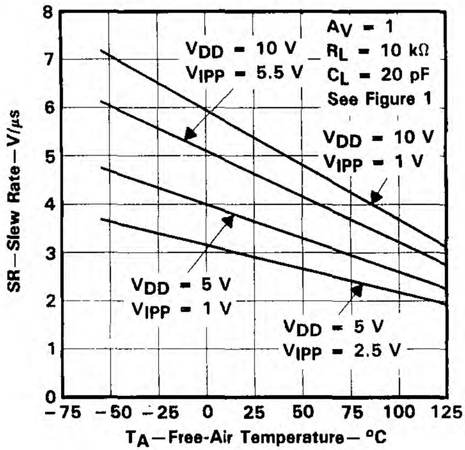

FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

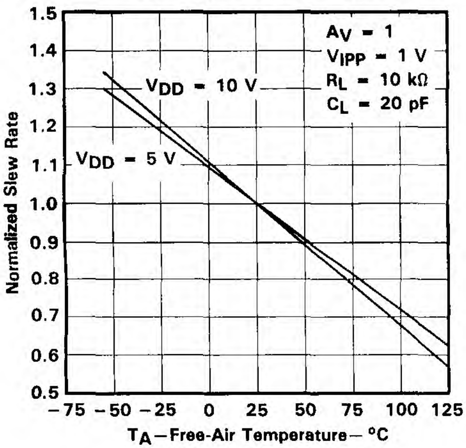

FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

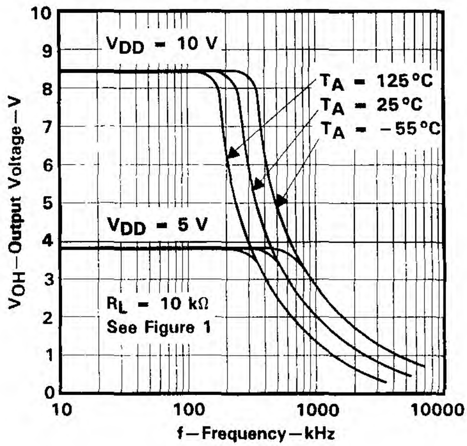

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

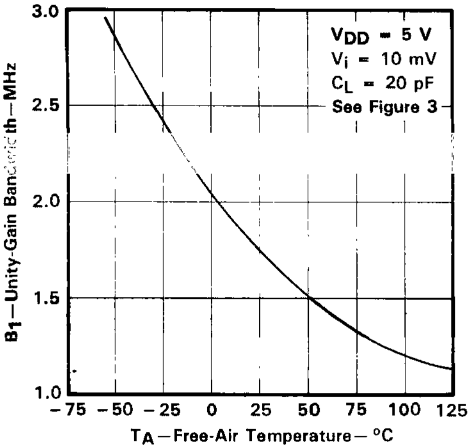


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

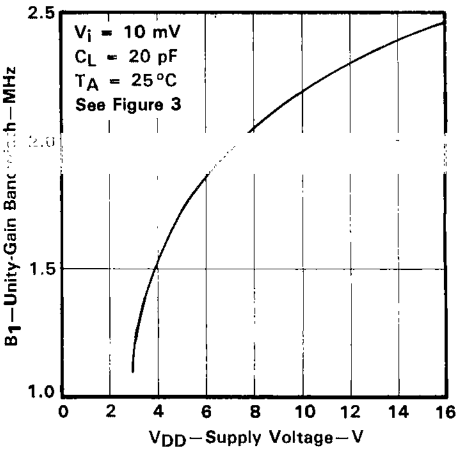


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

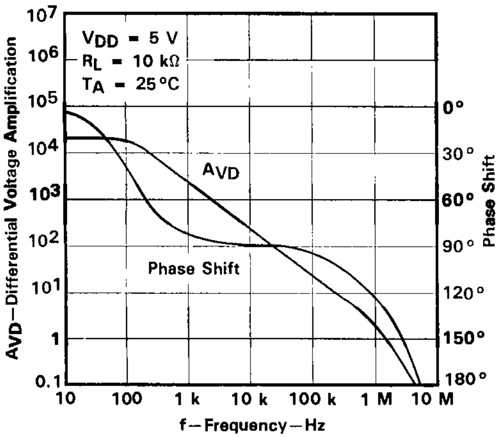


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

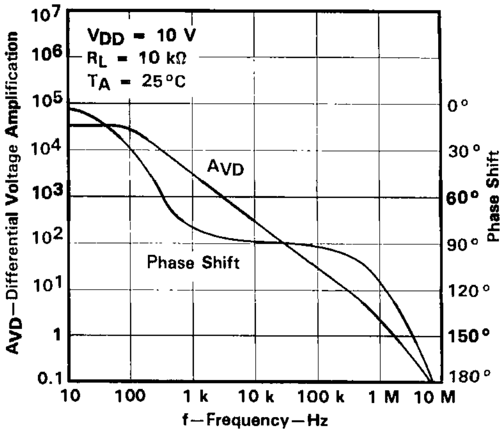


FIGURE 33

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

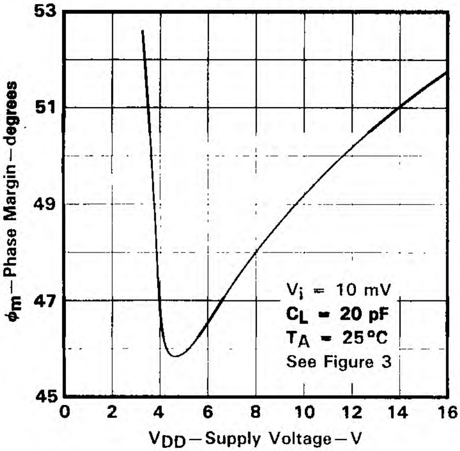


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

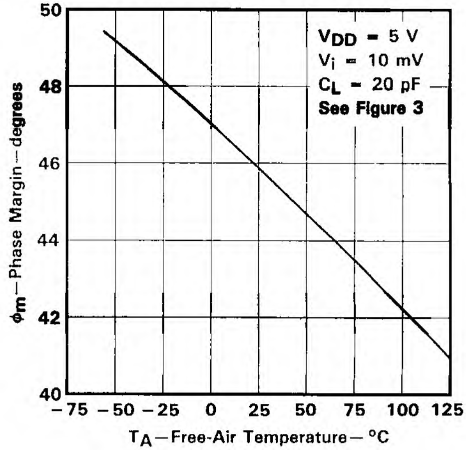


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

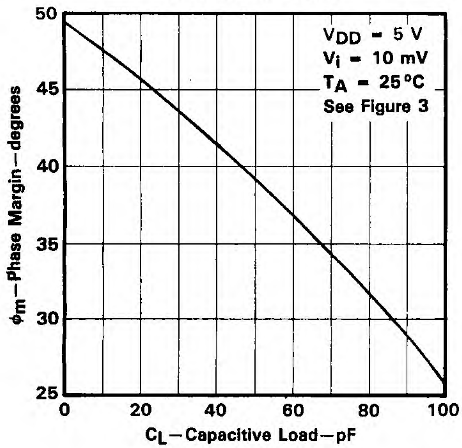


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

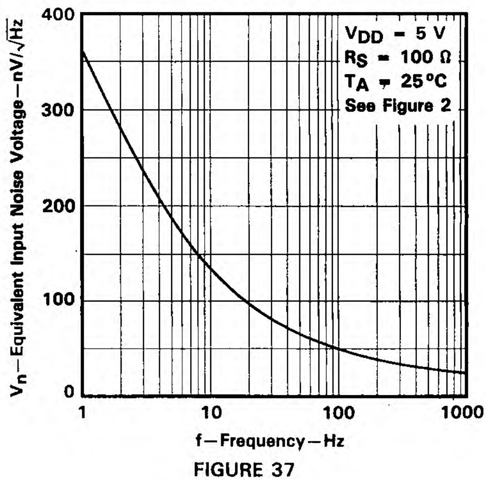


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

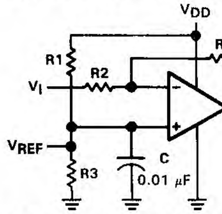
single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

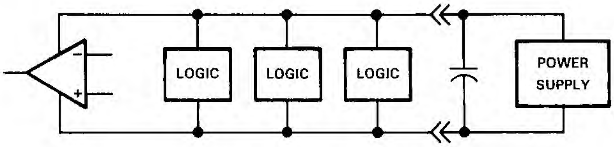
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



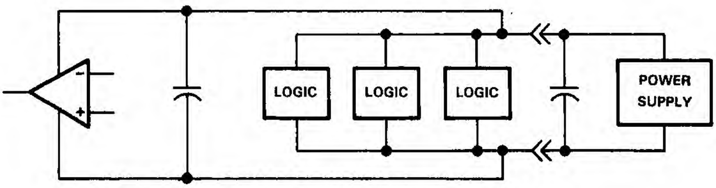
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

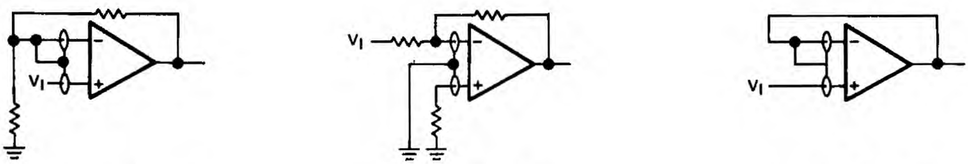
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

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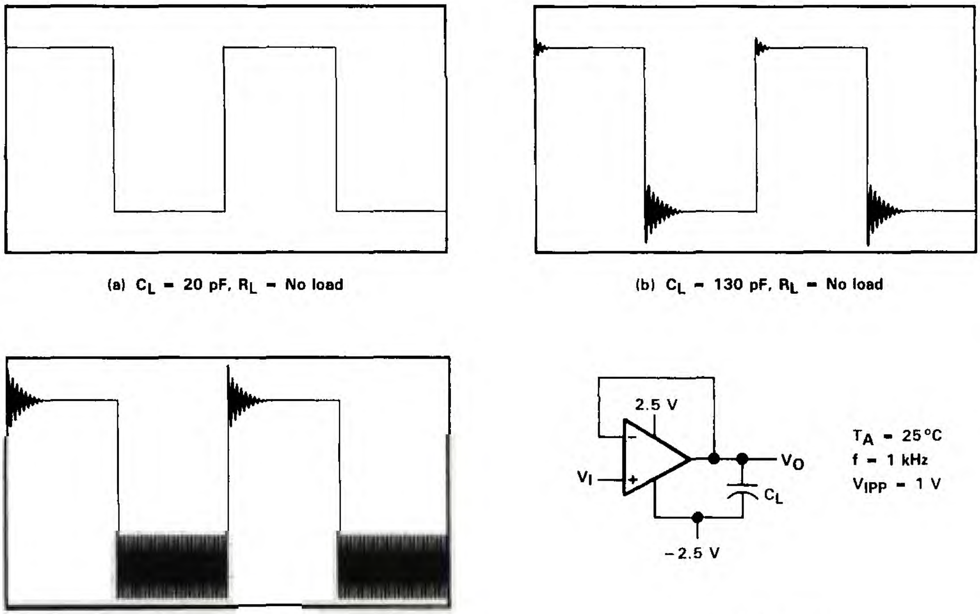
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 130 pF, R_L = No load

(c) C_L = 150 pF, R_L = No load

(d) Test Circuit

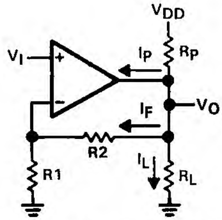
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

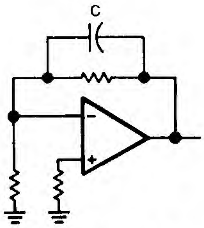


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand – 100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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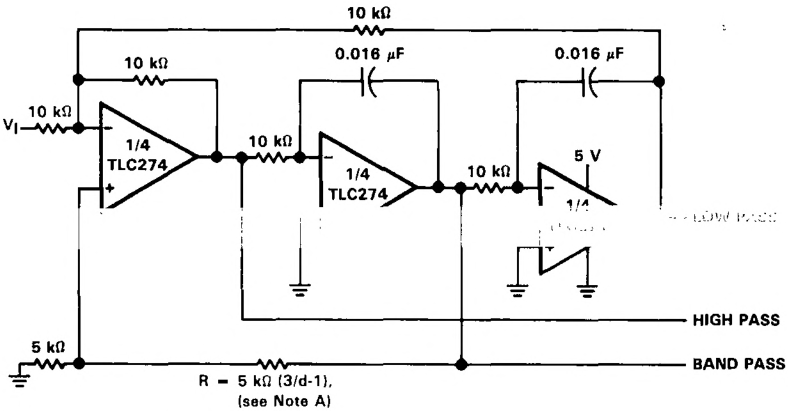
TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

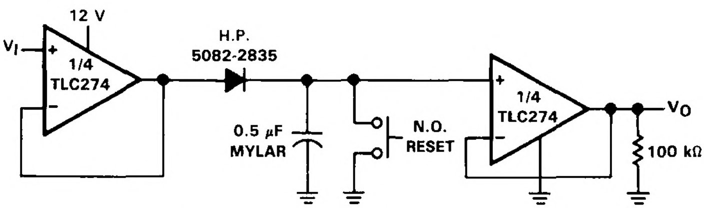
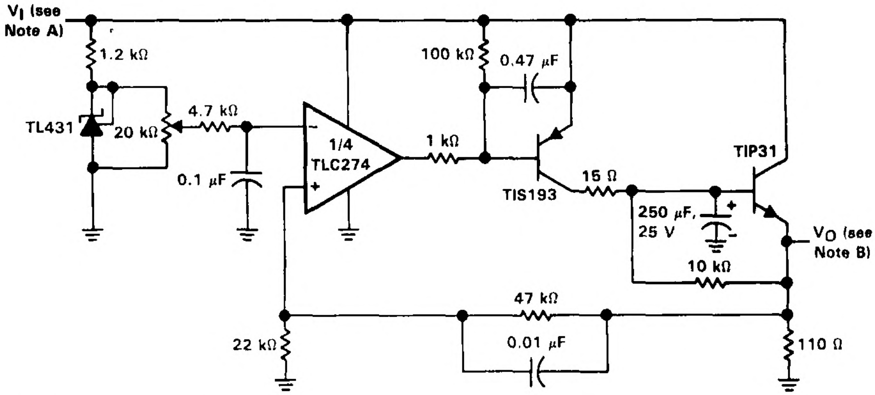


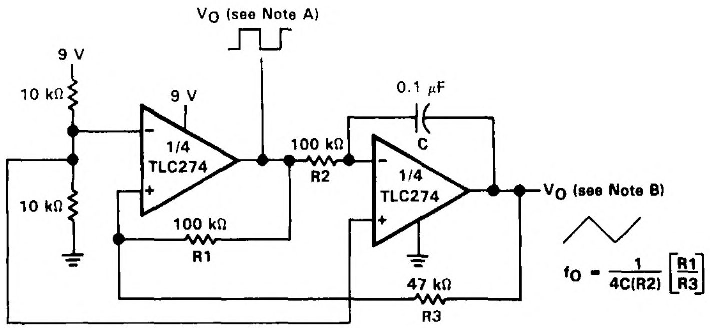
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

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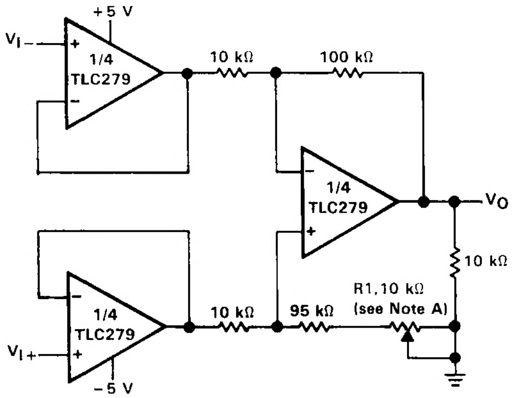
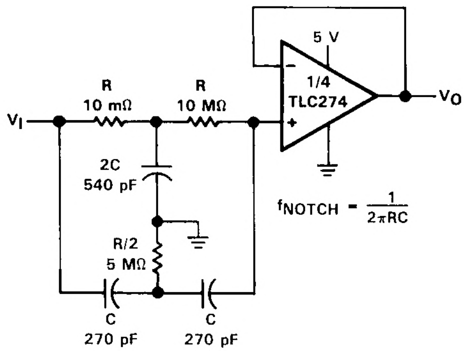
TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER



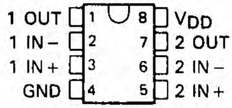
$$f_{NOTCH} = \frac{1}{2\pi RC}$$

FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

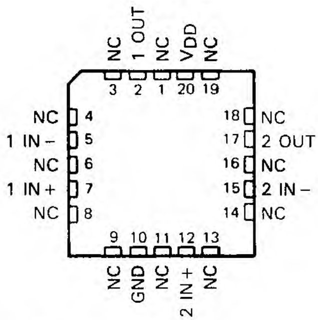
D3139, OCTOBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25 °C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55 °C to 125 °C . . . 4 V to 16 V
  −40 °C to 85 °C . . . 4 V to 16 V
  0 °C to 70 °C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultralow Power . . . Typically 95 μW at 25 °C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



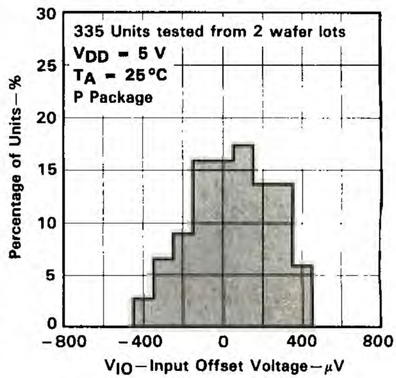
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25 °C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0 °C to 70 °C	[illegible] μV	TLC27L7CD	—	TLC27L7CJG	TLC27L7CP
	[illegible] mV	TLC27L2BCD	—	TLC27L2BCJG	TLC27L2BCP
	5 mV	TLC27L2ACD	—	TLC27L2A[illegible]	TLC27[illegible]
	10 mV	TLC27[illegible]	—	TLC27[illegible]	TL[illegible]
−40 °C to 85 °C	500 μV	TLC27[illegible]	—	TLC27[illegible]	TL[illegible]IP
	2 mV	T[illegible]	—	T[illegible]G	TL[illegible]BIP
	5 mV	T[illegible]AID	—	T[illegible]AIJG	TL[illegible]AIP
	10 mV	TLC27L2ID	—	TLC27L2IJG	TLC27L2IP
−55 °C to 125 °C	500 μV	—	TLC27L7MFK	TLC27L7MJG	—
	10 mV	—	TLC27L2MFK	TLC27L2MJG	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



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description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

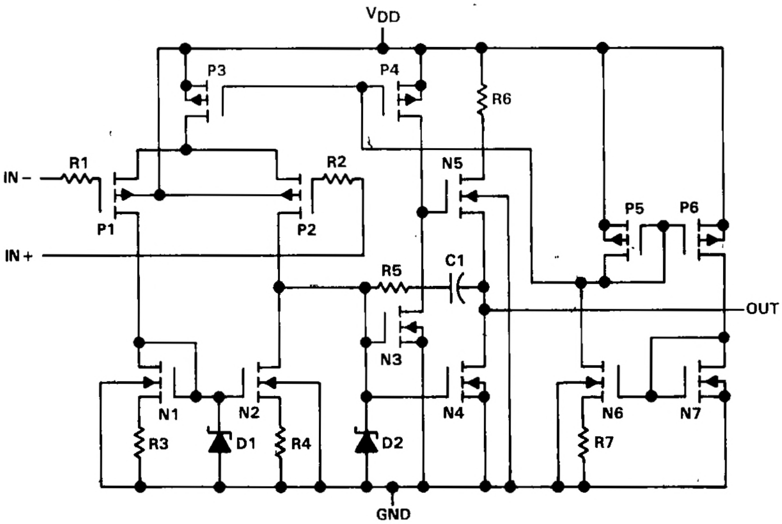
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55 °C to 125 °C. I-suffix devices are characterized for operation from −40 °C to 85 °C, and C-suffix devices are characterized for operation from 0 °C to 70 °C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) .... 18 V
Differential input voltage (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... -0.3 V to V_{DD}
Input current, I_I .... ±5 mA
Output current, I_O (each output) .... ±30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... −55°C to 125°C
I-suffix .... −40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	[illegible] mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		[illegible]	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Fu[illegible]		[illegible]	12	mV
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		170	500	μV
				Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−55°C	3	4.1		V
				125°C	3	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	mV
				125°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	500		V/mV
				−55°C	25	1[illegible]		V/mV
				125°C	25	[illegible]		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−55°C	60	95		dB
				125°C	60	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		dB
				125°C	60	98		dB
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				−55°C		35	60	μA
				[illegible]		14	24	μA

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		190	800	μV
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−55°C	25	1750		
					125°C	25	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	[illegible]		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					[illegible] C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	[illegible] C		29	46	μA
					−55°C		56	96	
					125°C		18	30	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	[illegible]	μV
				Full range			[illegible]	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	[illegible]	
				Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		[illegible]	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				−40°C	50	[illegible]		
				85°C	50	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				−40°C	60	97		
				85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	μA
				−40°C		49	86	
				85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		0.9	5	mV
				Full range			7	mV
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		[illegible]	[illegible]	μV
				Full range			[illegible]	μV
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	[illegible]	μV
				Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		[illegible]	[illegible]	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		V
				85°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	mV
				85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				−40°C	50	[illegible]		V/mV
				85°C	50	[illegible]		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				−40°C	60	97		dB
				85°C	60	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		dB
				85°C	60	98		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	μA
				−40°C		49	86	μA
				85°C		20	36	μA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full [illegible]			12	
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		0.9	5	
				Full [illegible]			6.5	
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		204	[illegible]	μV
				Full range			[illegible]	
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		170	[illegible]	
				Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	500		V/mV
				0°C	50	700		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				0°C		24	42	
				70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				[illegible]			[illegible]	μV
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		190	[illegible]	μV
				Full range			1900	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		8	300	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		V
				70°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	mV
				70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	[illegible]		V/mV
				0°C	50	[illegible]		V/mV
				70°C	50	660		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				0°C	60	97		dB
				70°C	60	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		dB
				70°C	60	98		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	μA
				0°C		36	66	μA
				70°C		22	40	μA

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

TEXAS INSTRUMENTS
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operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				[illegible]		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				[illegible]		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

2

Operational Amplifiers

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

TEXAS INSTRUMENTS
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operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

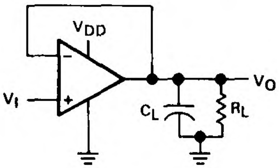
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

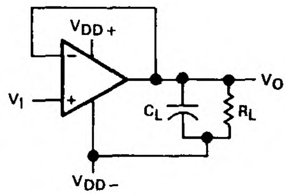
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

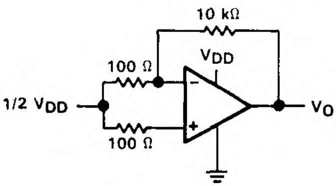


(a) Single-Supply

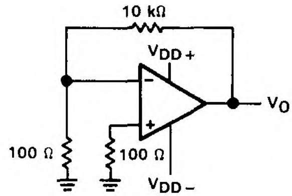


(b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER

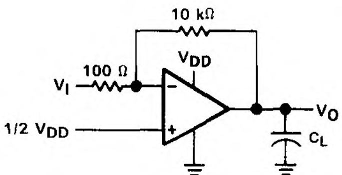


(a) Single-Supply

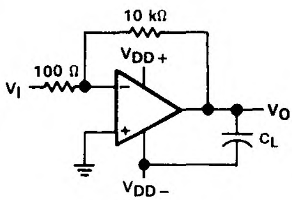


(b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply



(b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

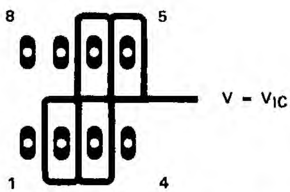


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

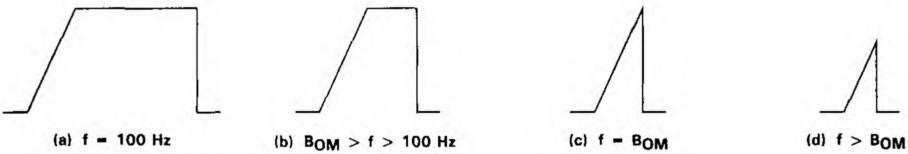


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

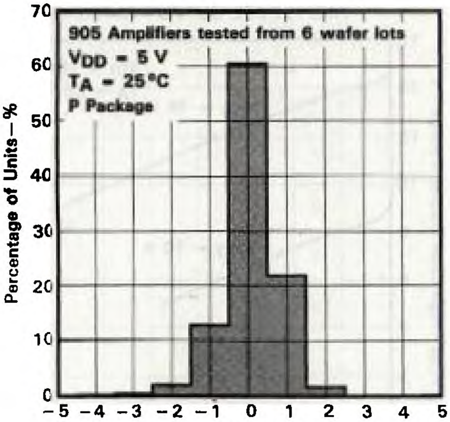


FIGURE 6

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

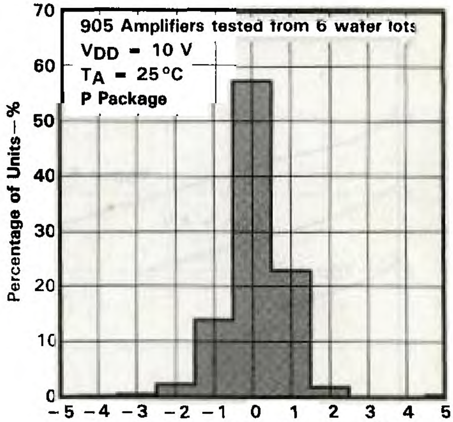


FIGURE 7

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

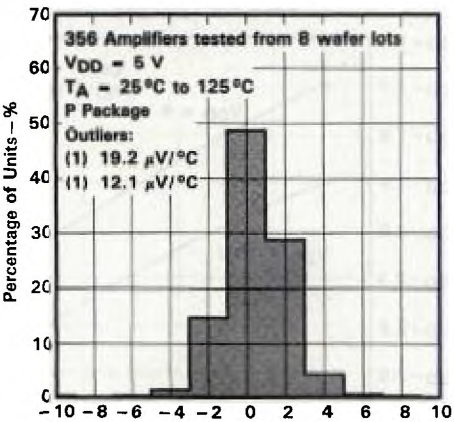


FIGURE 8

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

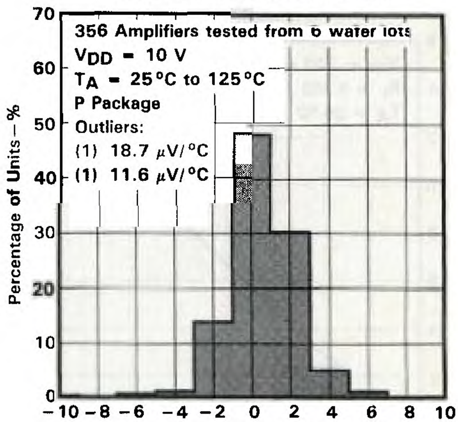


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

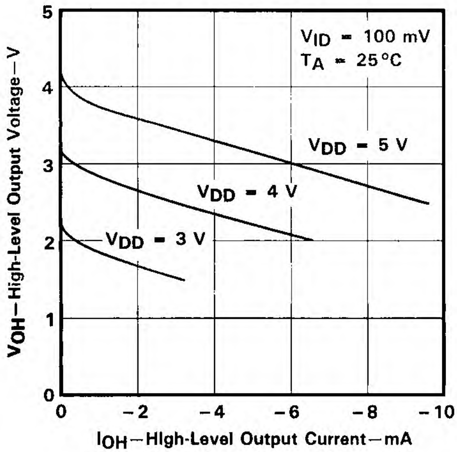


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

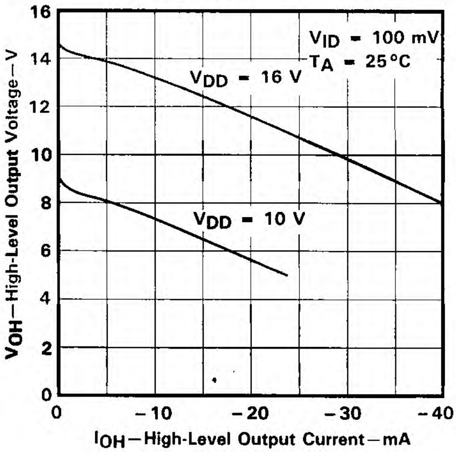


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

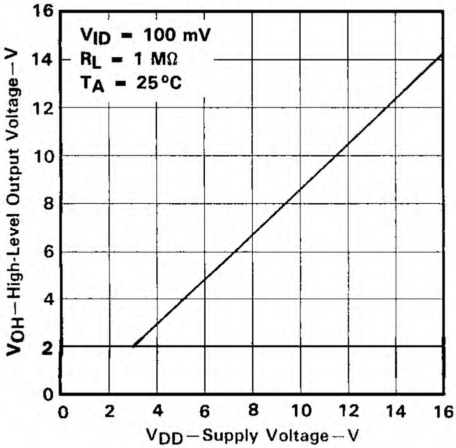


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

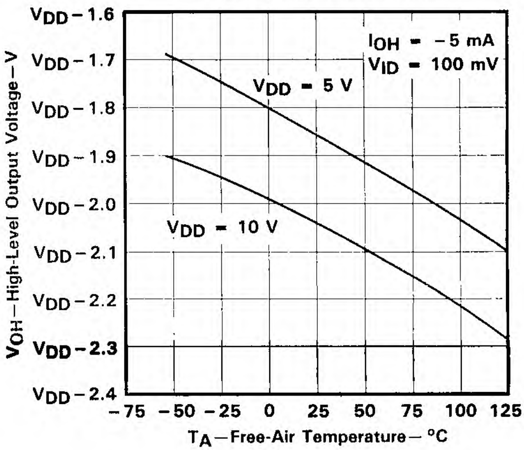


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

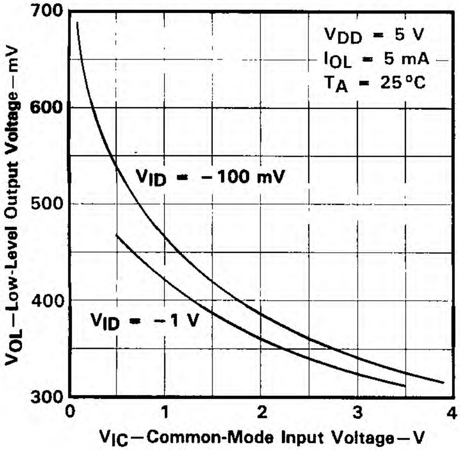


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

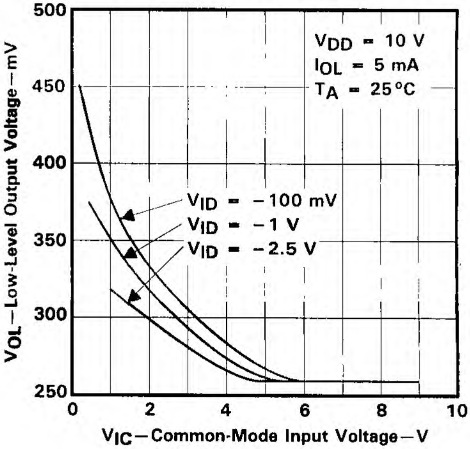


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

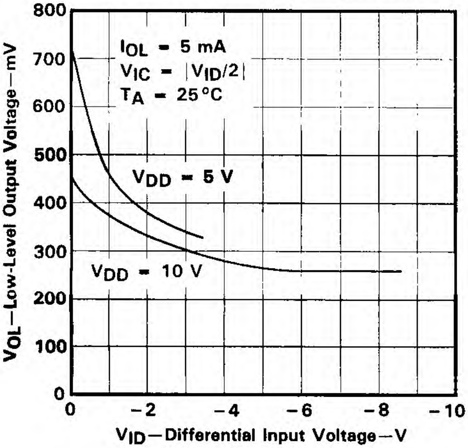


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

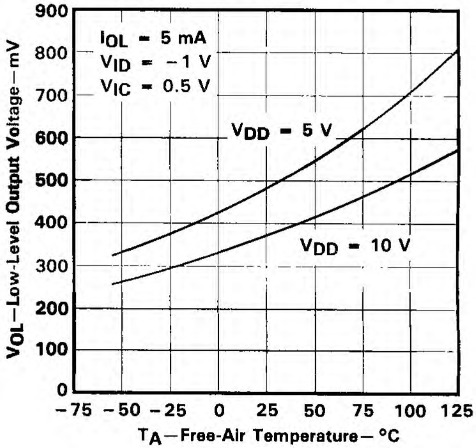


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

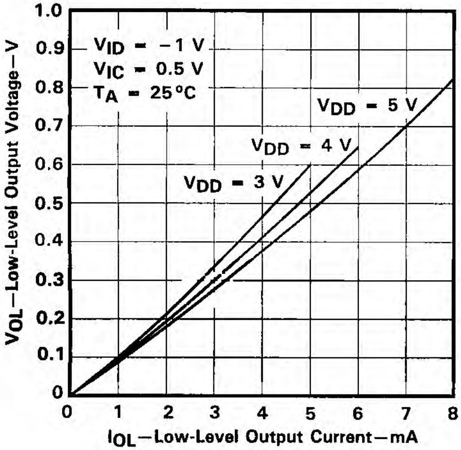


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

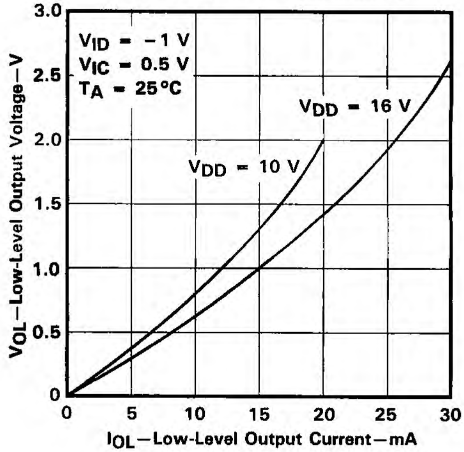


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

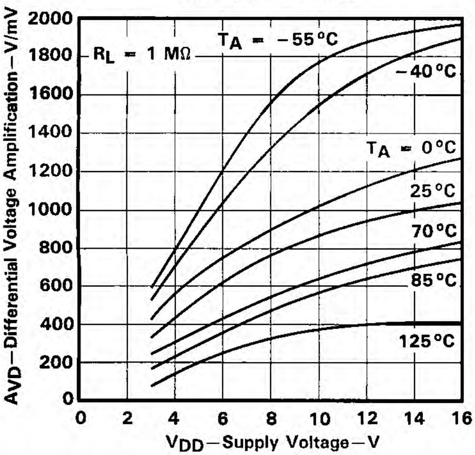


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

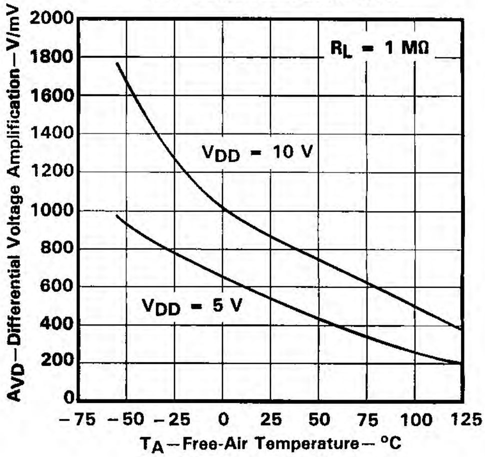


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

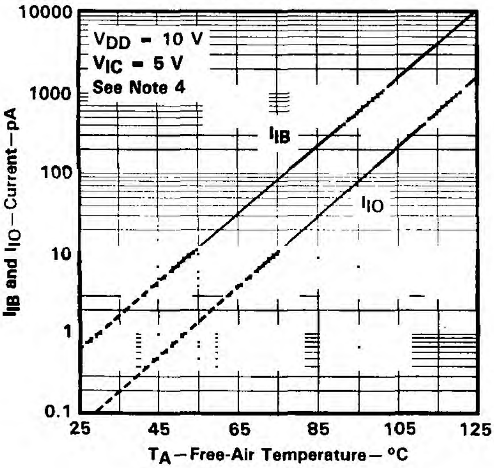


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

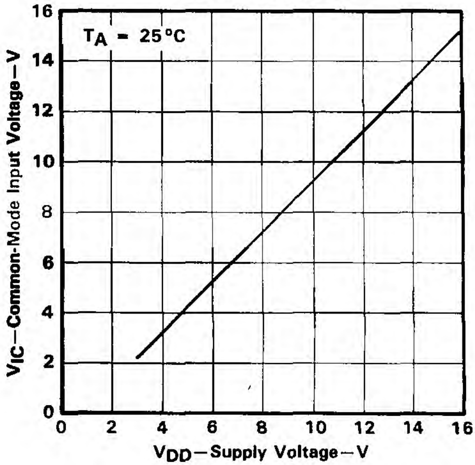


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

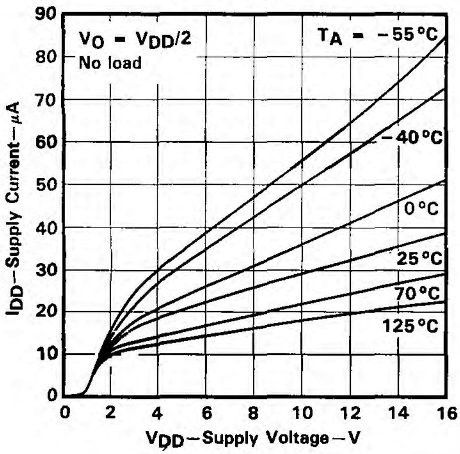


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

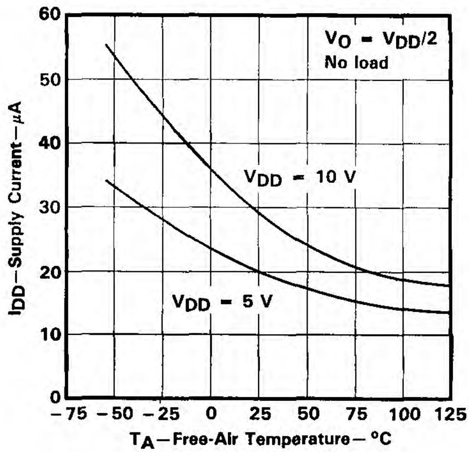


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

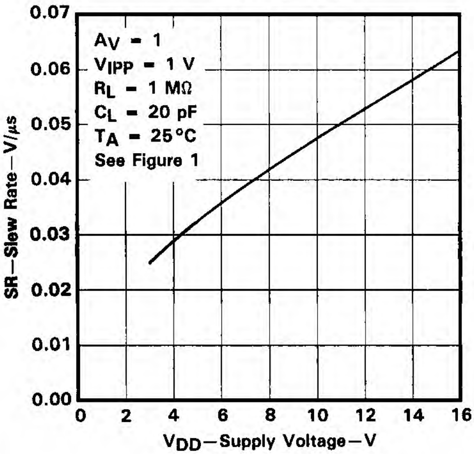


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

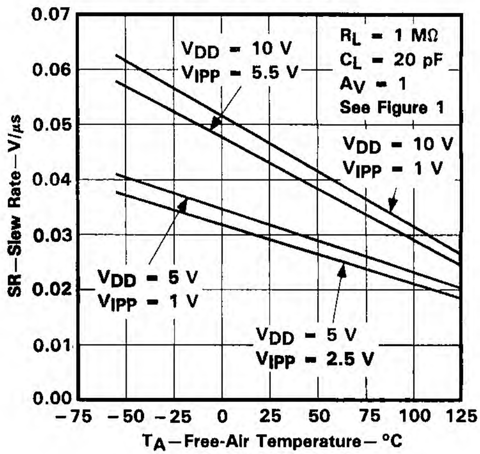


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

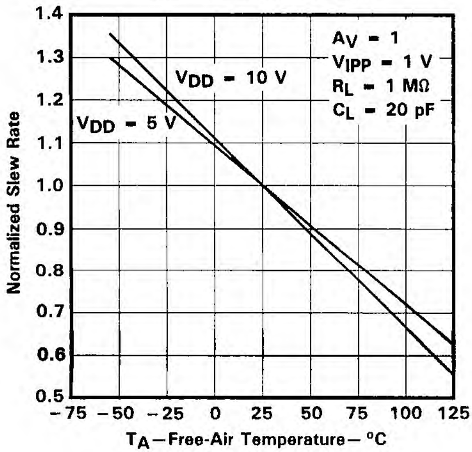


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

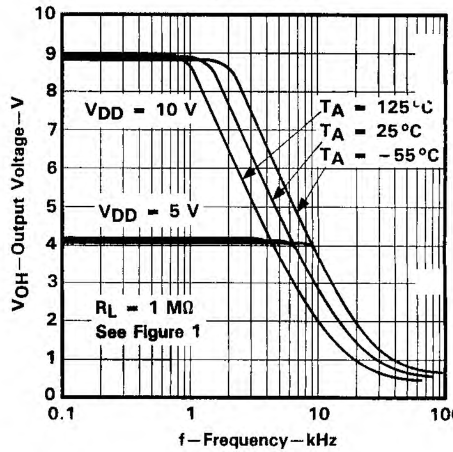


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

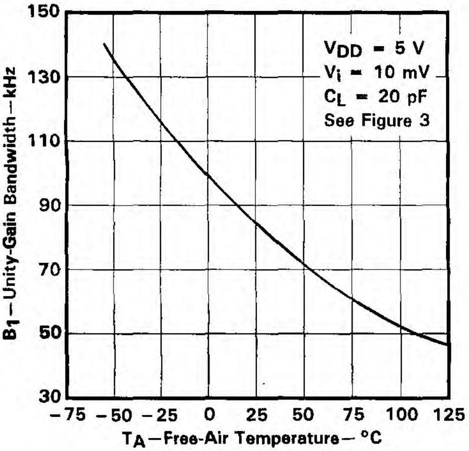


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

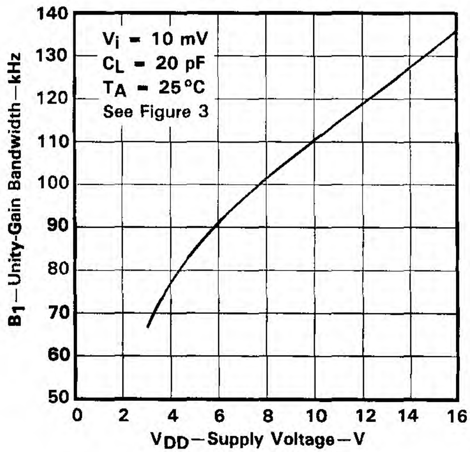


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

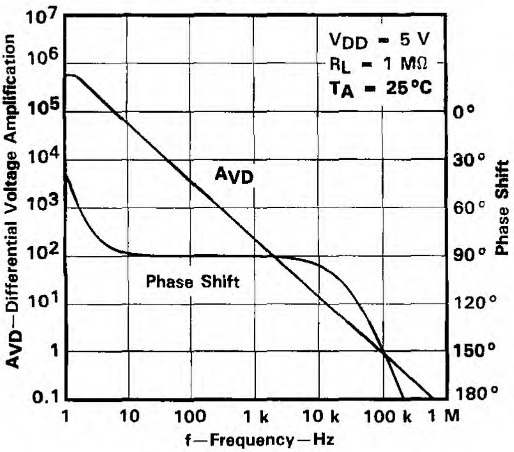


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

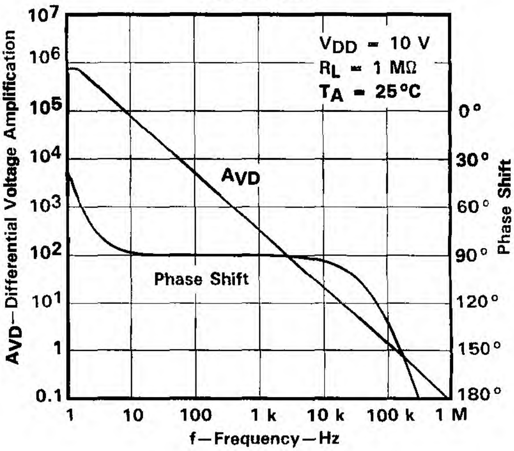


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

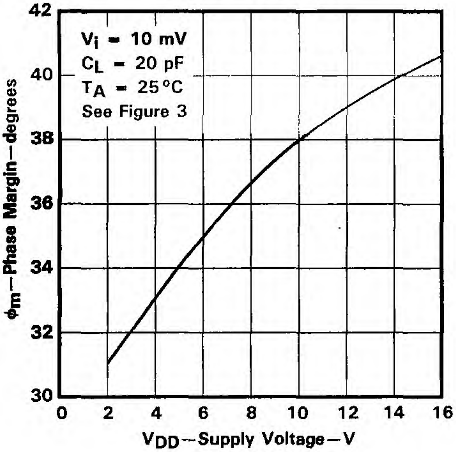


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

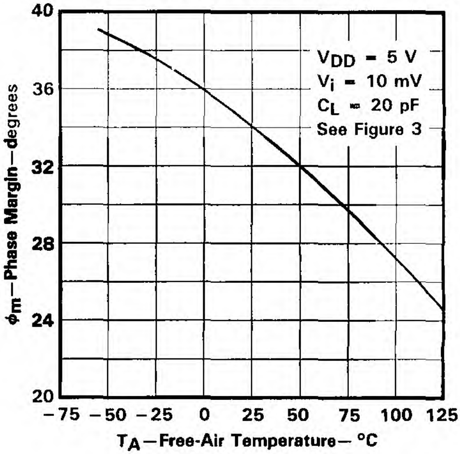


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

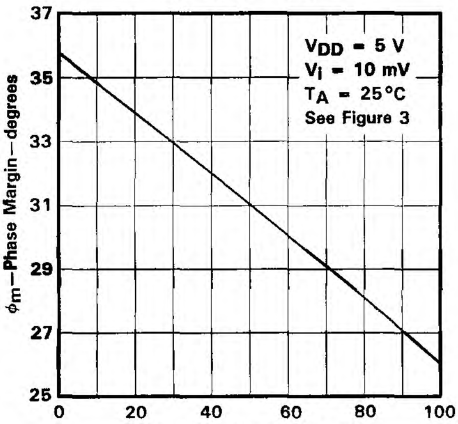


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

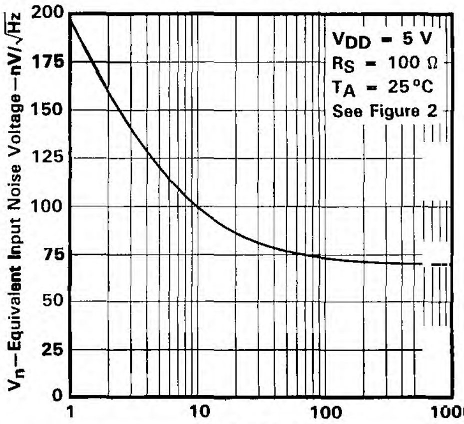


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

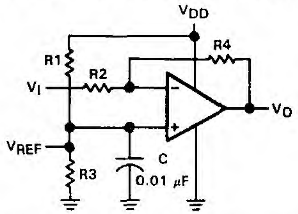
single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

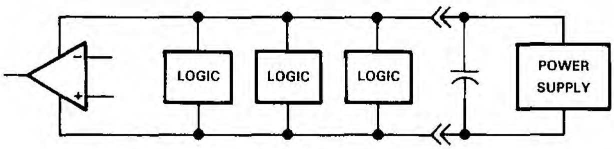
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



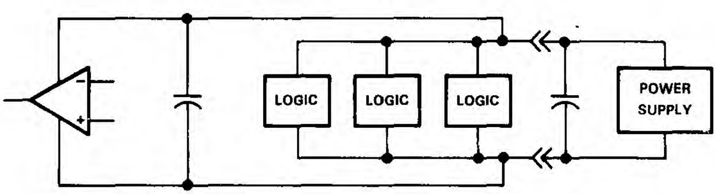
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

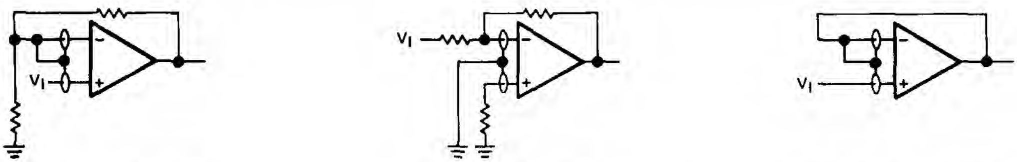
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

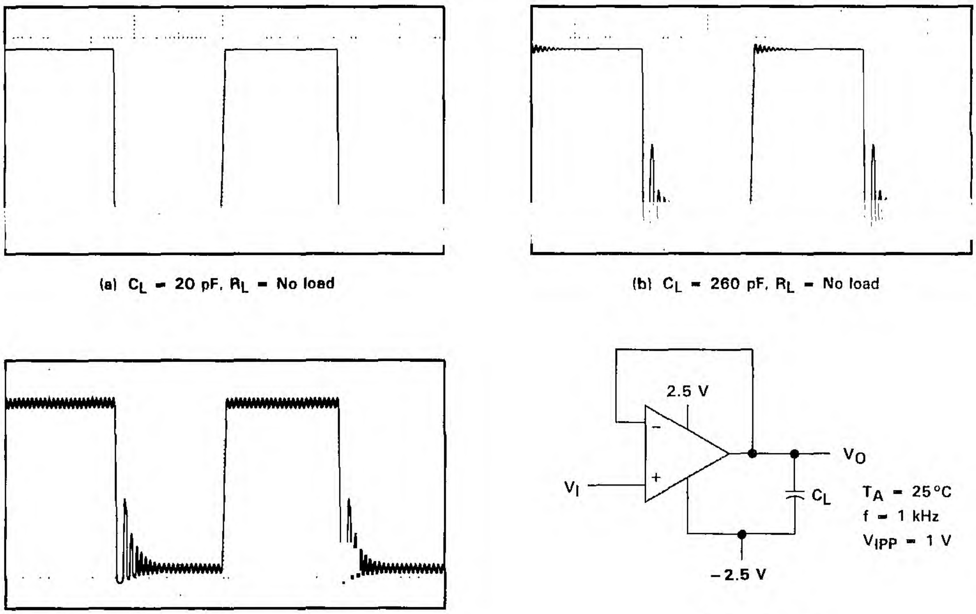
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 260 pF, R_L = No load

(c) C_L = 310 pF, R_L = No load

(d) Test Circuit

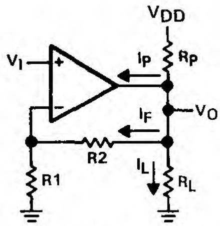
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

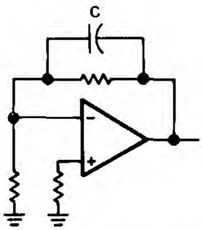


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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TYPICAL APPLICATION DATA

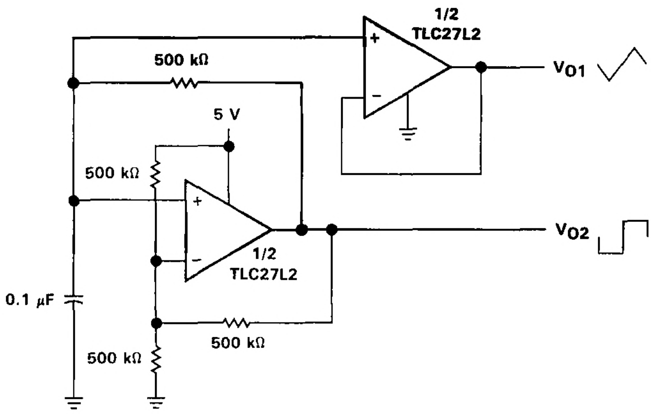
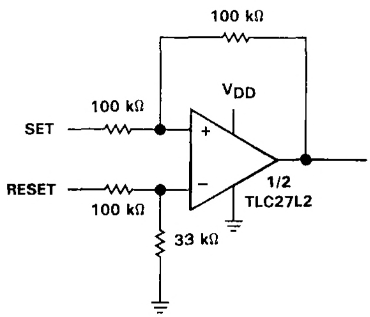


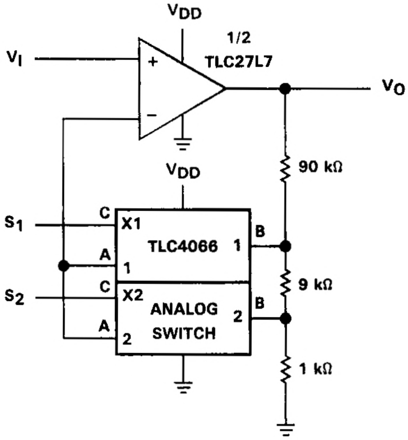
FIGURE 44. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

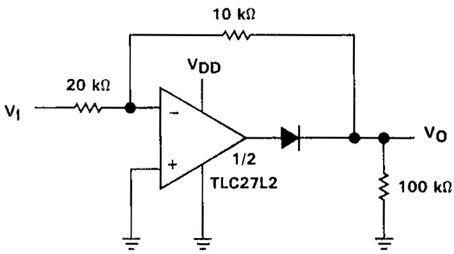
TYPICAL APPLICATION DATA



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

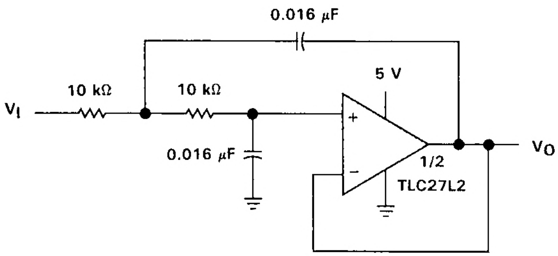
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

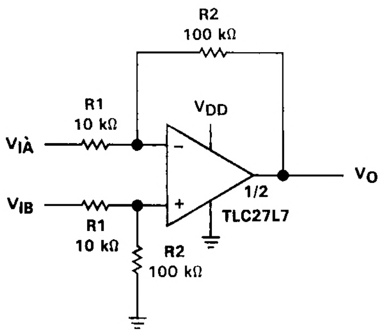
FIGURE 47. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

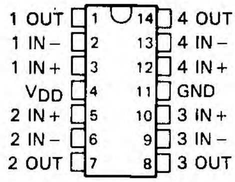
$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER

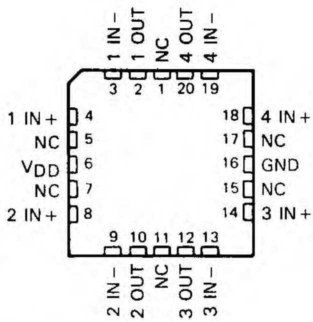
D3142, OCTOBER 1987—REVISED AUGUST 1988

- Trimmed Offset Voltage: TLC27L9 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Ultra-Low Power . . . Typically 195 μW at 25°C, V_{DD} = 5 V
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latchup Immunity

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

2

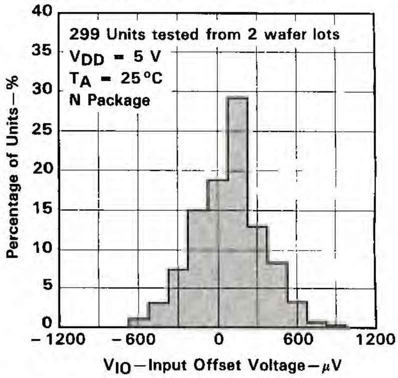
Operational Amplifiers

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE: SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC27L9CD	—	TLC27L9CJ	TLC27L9CN
	2 mV	TLC27L4BCD	—	TLC27[illegible]	TLC27L4BCN
	5 mV	TLC27L4ACD	—	TLC27L4ACJ	TLC27L4A[illegible]
	10 mV	TLC27L4CD	—	TLC27L4CJ	TLC27L4CN
−40°C to 85°C	900 μV	TLC27L9ID	—	TLC27L9IJ	TLC27L9IN
	2 mV	TLC27L[illegible]	—	TLC27L4BIJ	TLC27L4BIN
	5 mV	TLC27L[illegible]	—	TLC27L4AIJ	TLC27L4AIN
	10 mV	TLC27L4ID	—	TLC27L4IJ	TLC27L4IN
−55°C to 125°C	900 μV	—	TLC27L9MFK	TLC27L9MJ	—
	10 mV	—	TLC27L4MFK	TLC27L4MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27L9CDR).

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



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description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading exisitng designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power comsumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

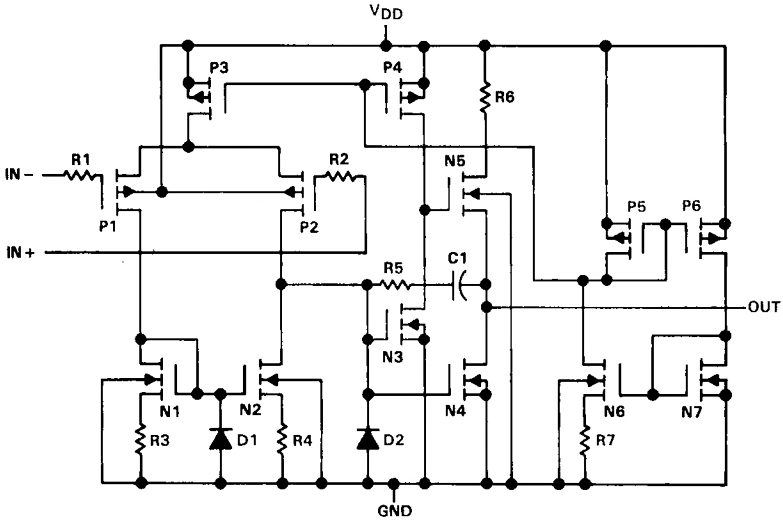
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . −0.3 V to V_{DD}
Input current, I_I . . . . ±5 mA
Output current, I_O (each output) . . . . ±30 mA
Total current into V_{DD} terminal . . . . 45 mA
Total current out of ground terminal . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . −55°C to 125°C
I-suffix . . . . −40°C to 85°C
C-suffix . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−55°C	3	4.1		
				125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−55°C	25	950		
				125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−55°C	60	95		
				125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				[illegible]	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	[illegible]		39	68	µA
				−55°C		69	120	
				[illegible]		27	48	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			[illegible]	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		210	[illegible]	μV
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	[illegible]		V/mV
					−55°C	25	[illegible]		
					125°C	25	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	[illegible]		dB
					−55°C	60	97		
					[illegible]	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	[illegible]	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	[illegible]	μA
					−55°C		111	[illegible]	
					125°C		35	[illegible]	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	[illegible]	µV
				Full range			[illegible]	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	[illegible]	
				Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	[illegible]	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	[illegible]	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−40°C	60	95		
				85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		39	68	µA
				−40°C		62	108	
				85°C		29	52	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full [illegible]			13	mV
		TLC27L4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	[illegible]		0.9	5	mV
					Full [illegible]			7	mV
		TLC27L4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	[illegible]		260	2000	μV
					Full [illegible]			[illegible]	μV
		TLC27L9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	[illegible]		210	[illegible]	μV
					Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		[illegible]	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		V
					85°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	mV
					85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−40°C	50	[illegible]		V/mV
					85°C	50	[illegible]		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		dB
					85°C	60	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		dB
					85°C	60	98		dB
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					−40°C		98	172	μA
					85°C		40	72	μA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full			6.5	
		TLC27L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	[illegible]		240	2000	µV
					Full range			3000	
		TLC27L9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		200	[illegible]	
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7		
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	[illegible]		V/mV
					0°C	50	[illegible]		
					70°C	50	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		40	68	µA
					0°C		48	84	
					70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		[illegible]	[illegible]	μV
				Full range			[illegible]	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	[illegible]		210	[illegible]	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	870		V/mV
				0°C	50	1020		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	μA
				0°C		72	[illegible]	
				70°C		44	[illegible]	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				[illegible] C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		[illegible]		
				125°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

TEXAS INSTRUMENTS
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operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

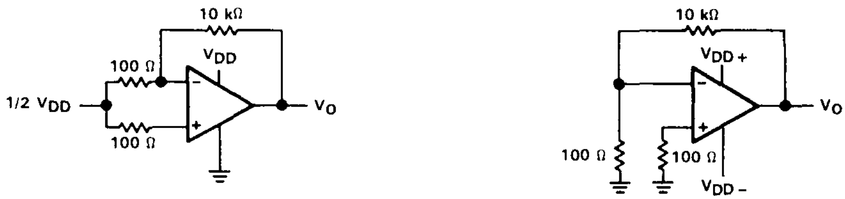
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

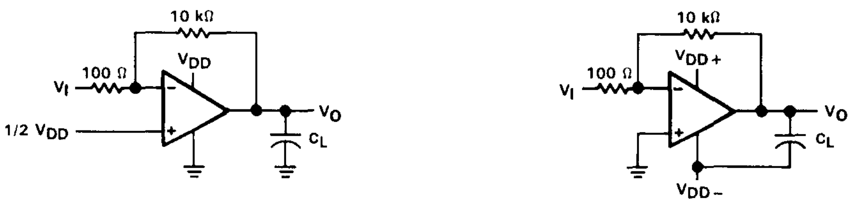
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 2. NOISE TEST CIRCUIT



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

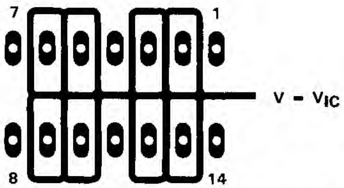


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

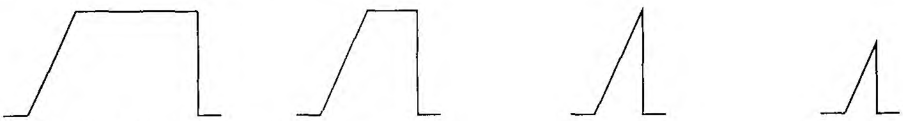
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) $B_{OM} > f > 100$ Hz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

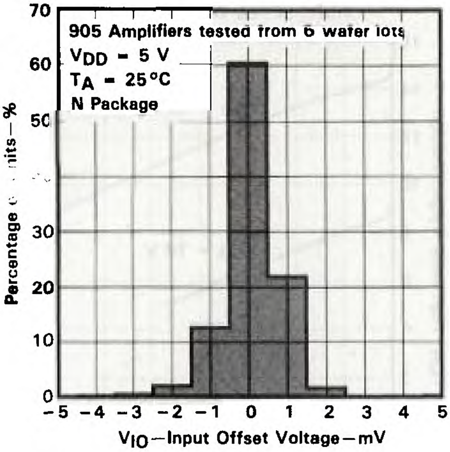


FIGURE 6

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

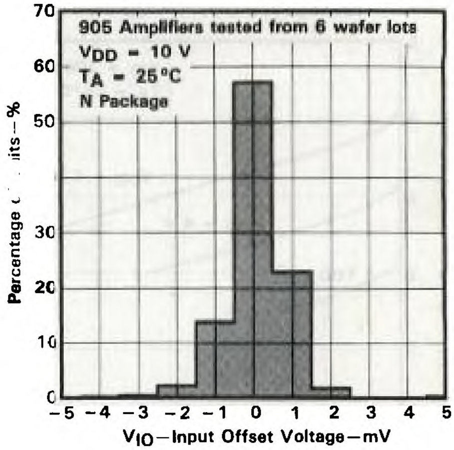


FIGURE 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

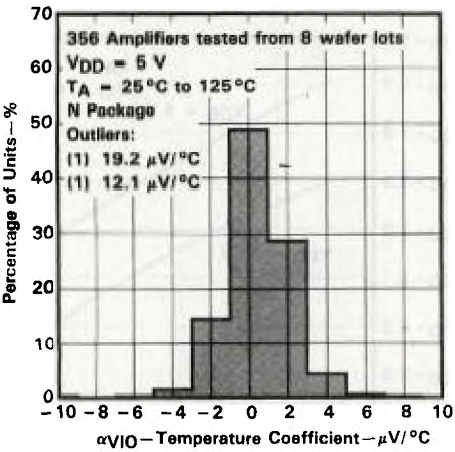


FIGURE 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

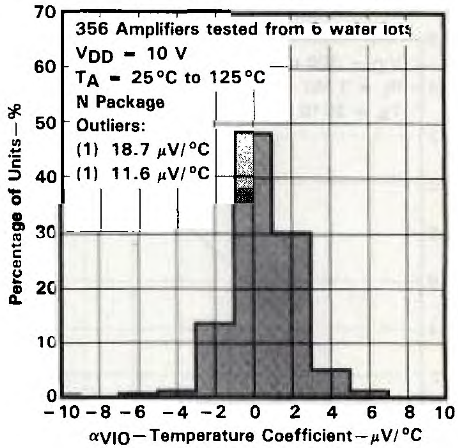


FIGURE 9

Operational Amplifiers

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

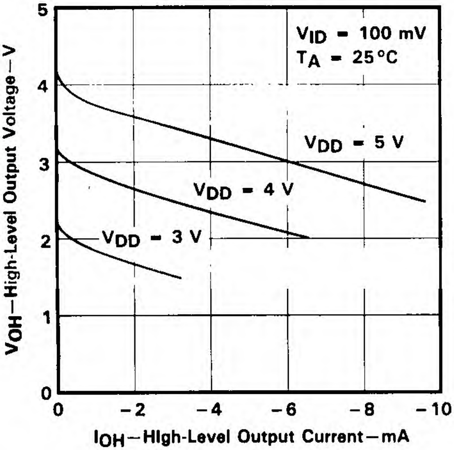


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

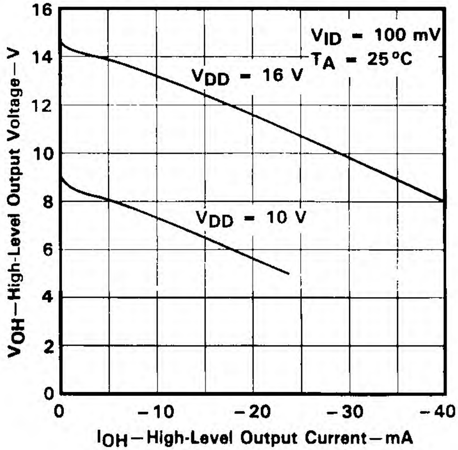


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

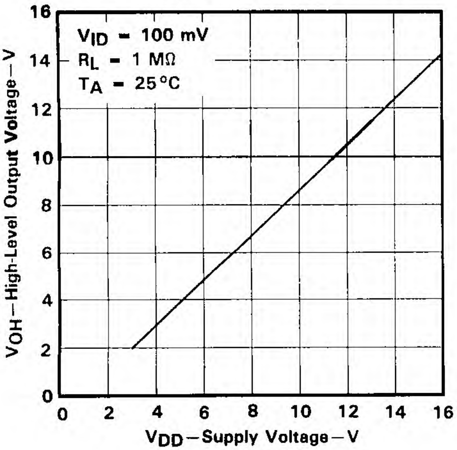


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

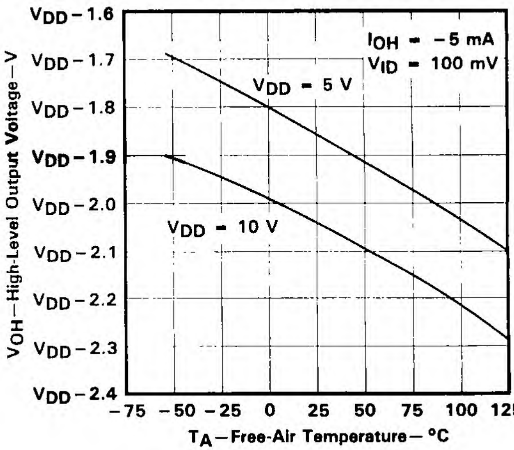


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

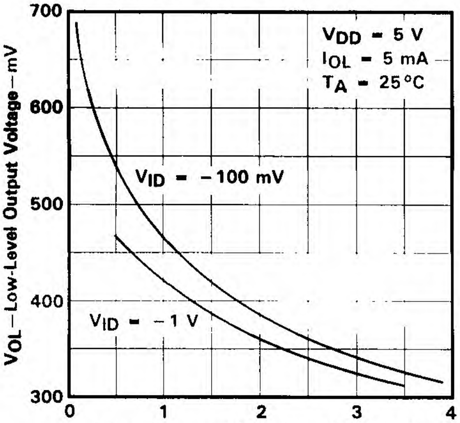


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

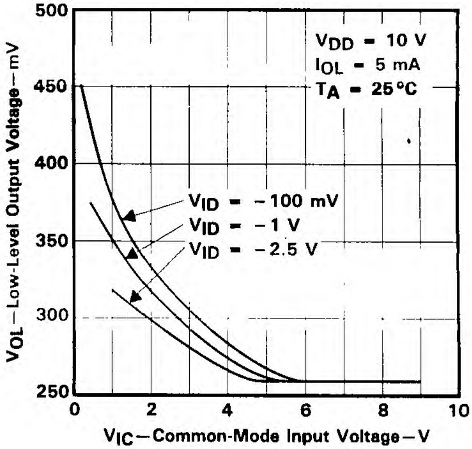


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

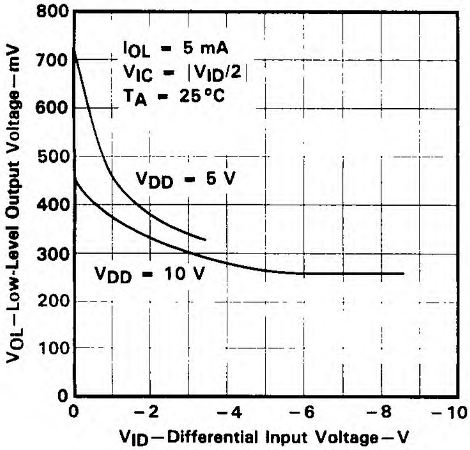


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

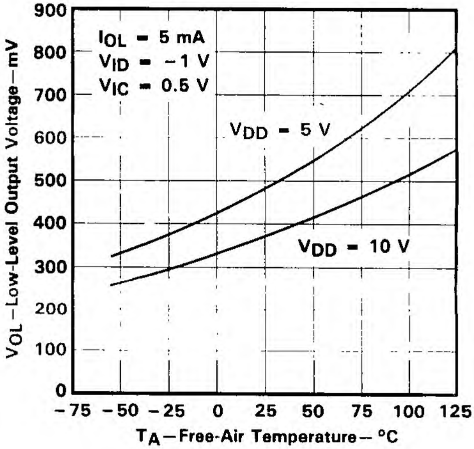


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

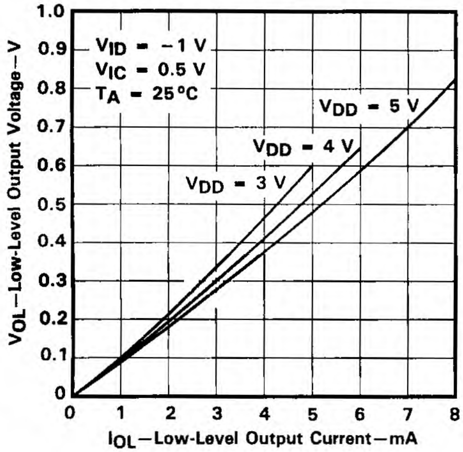


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

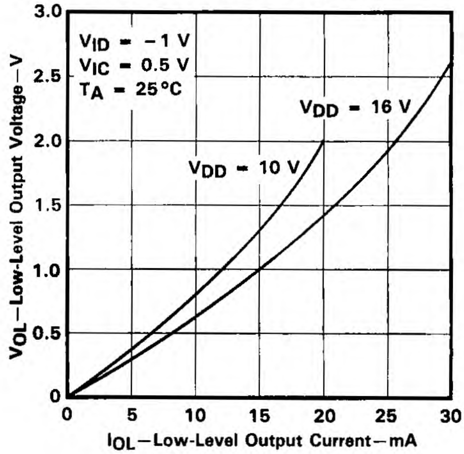


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

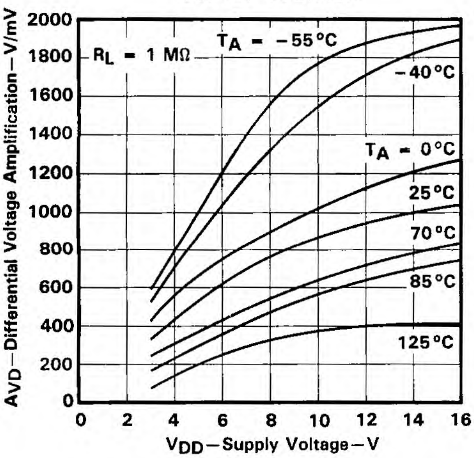


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

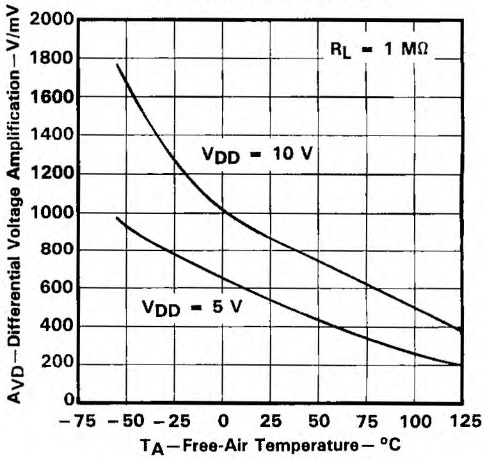


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

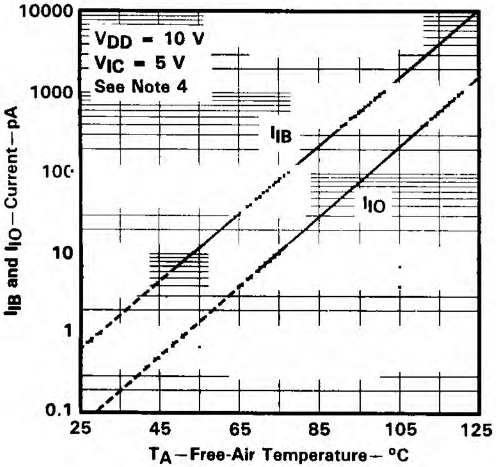


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

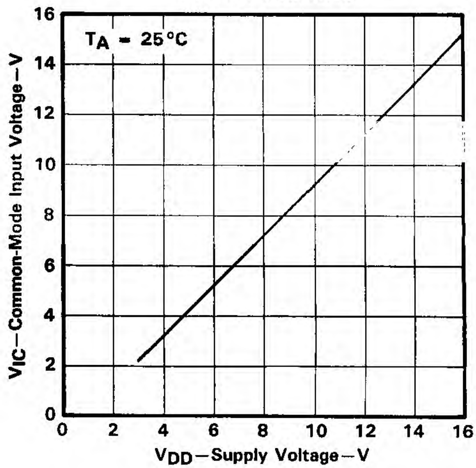


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

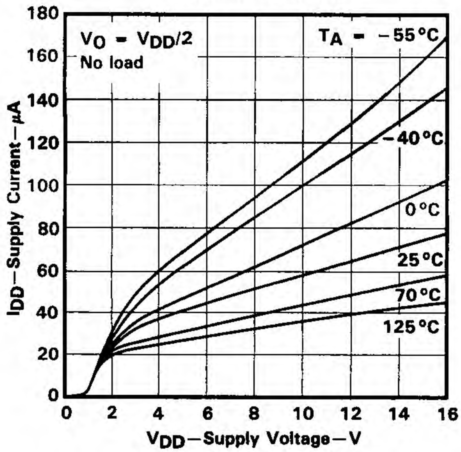


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

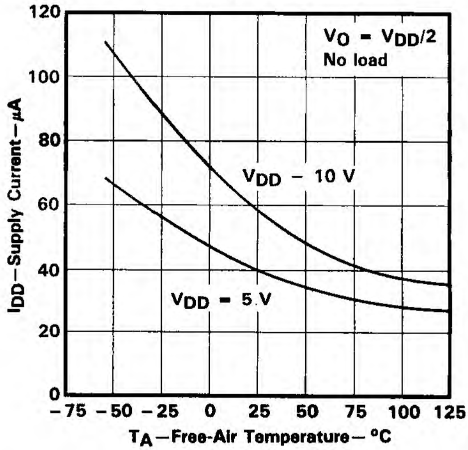


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

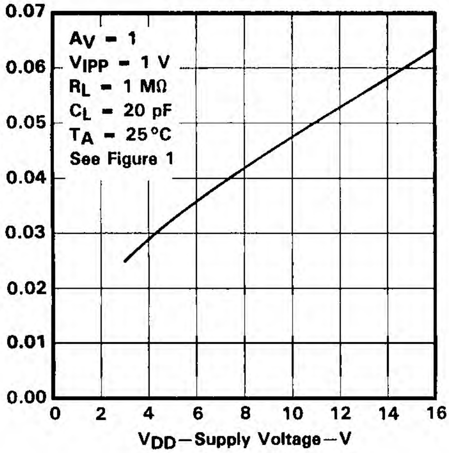


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

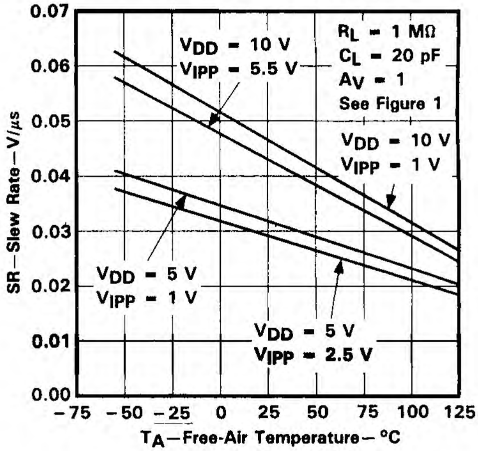


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

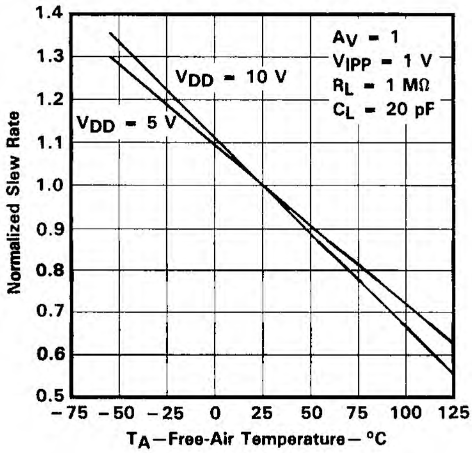


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

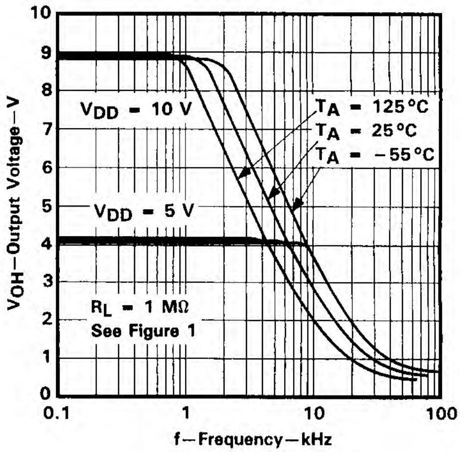


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

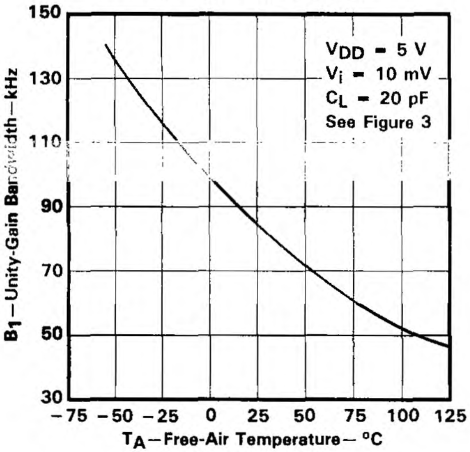


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

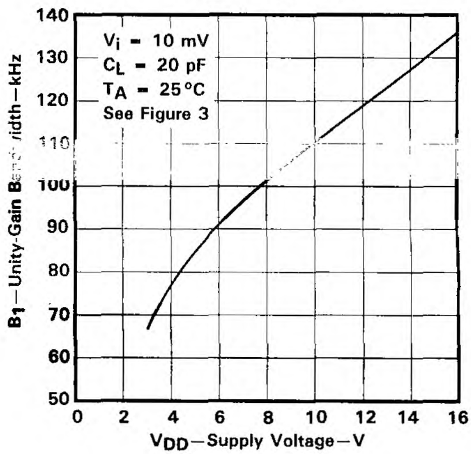


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

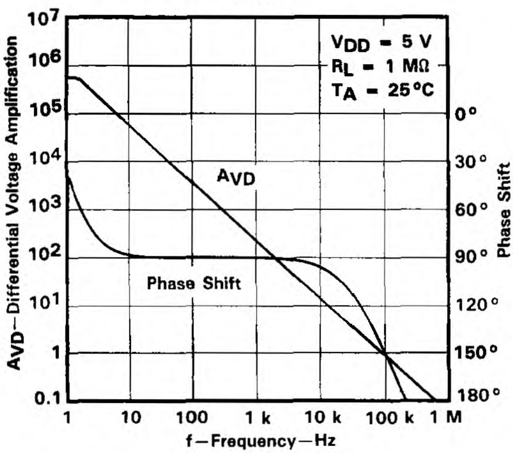


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

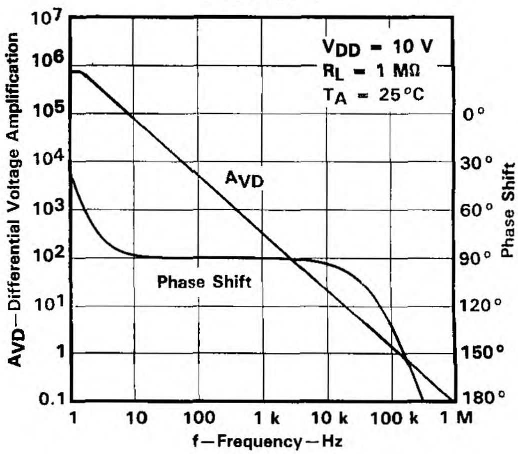


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

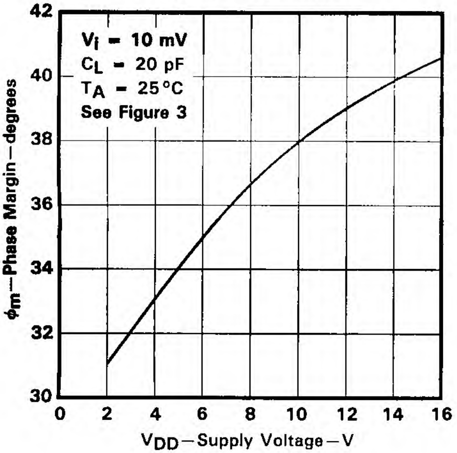


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

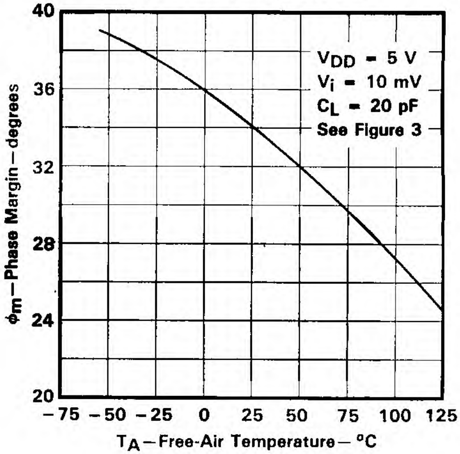


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

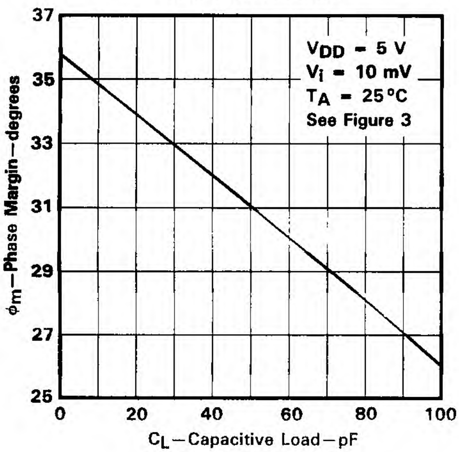


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

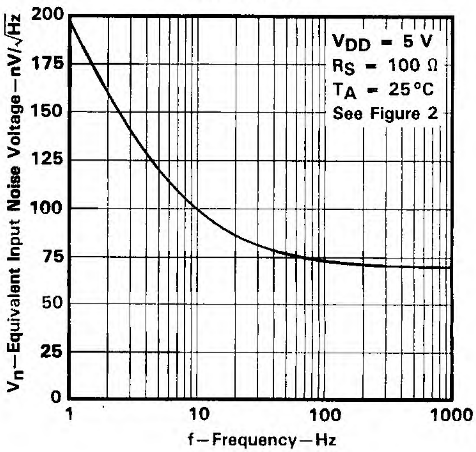


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

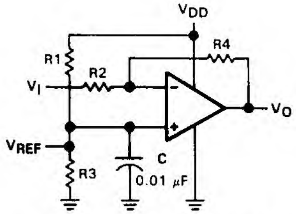
single-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

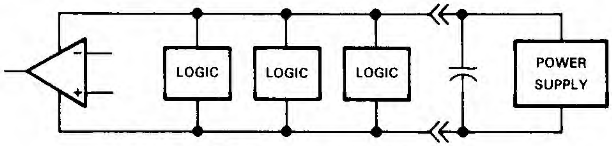
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



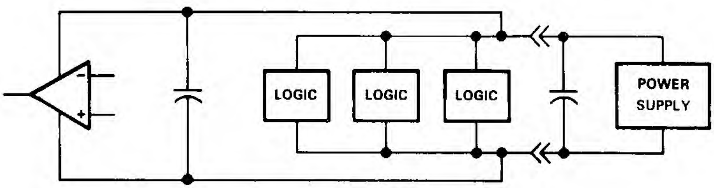
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

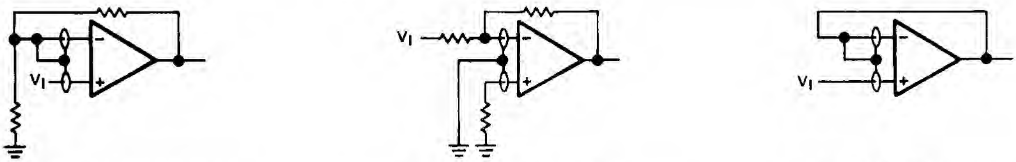
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER　(b) INVERTING AMPLIFIER　(c) UNITY-GAIN AMPLIFIER

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

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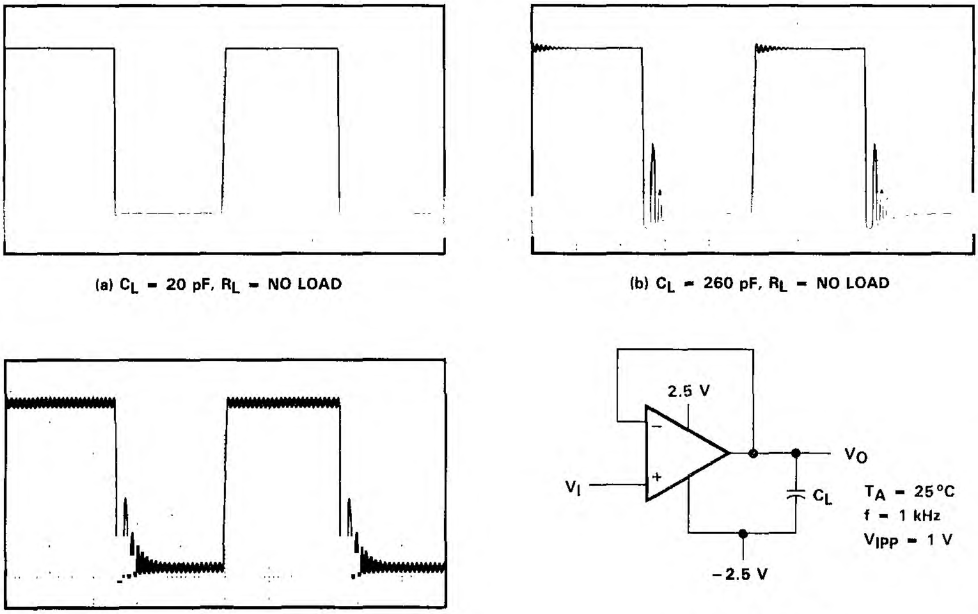
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

(d) TEST CIRCUIT

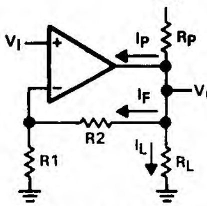
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of Rp, a voltage offset from 0 V at the output will occur. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

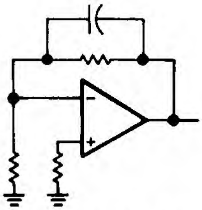


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

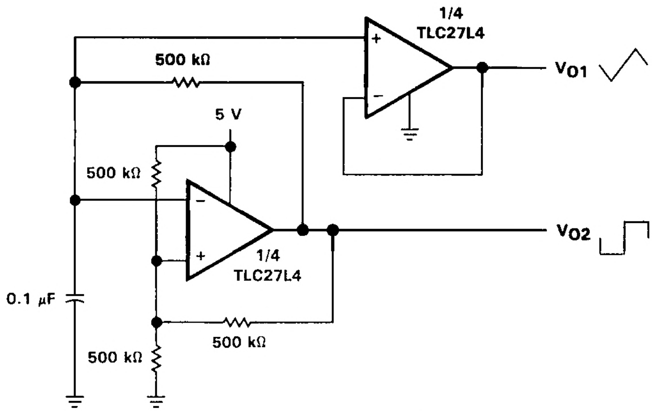
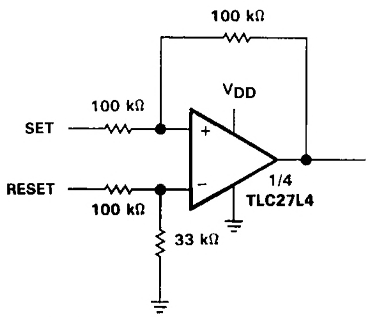


FIGURE 44. MULTIVIBRATOR

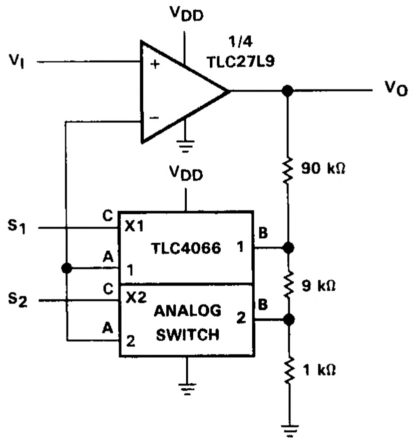


NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

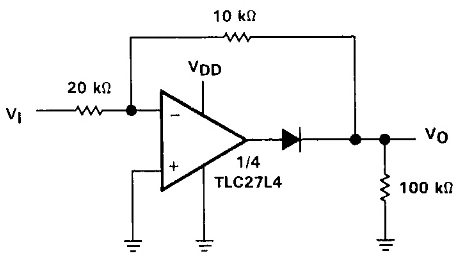
TYPICAL APPLICATION DATA

SELECT:	S_1	S_2
A_V	10	100



NOTE: V_{DD} = 5 V to 12 V

FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

FIGURE 47. FULL-WAVE RECTIFIER

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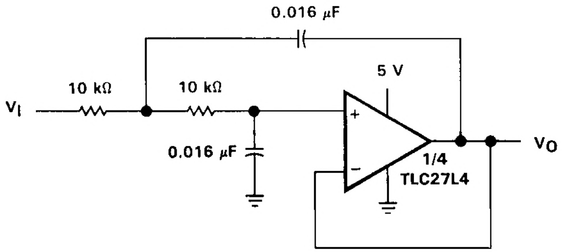
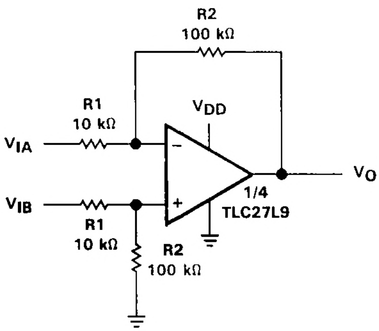
TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

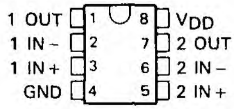
$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER

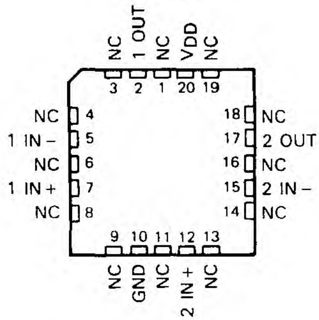
D3140, OCTOBER 1987—REVISED FEBRUARY 1989

- Trimmed Offset Voltage: TLC27M7 . . . 500 µV Max at 25 °C, V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days
- Wide Range of Supply Voltages over Specified Temperature Range:
  - −55°C to 125°C . . . 4 V to 16 V
  - −40°C to 85°C . . . 4 V to 16 V
  - 0°C to 70°C . . . 3 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 32 nV/$\sqrt{Hz}$ at f = 1 kHz
- Low Power . . . Typically 2.1 mW at 25°C, V_{DD} = 5 V
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latchup Immunity

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



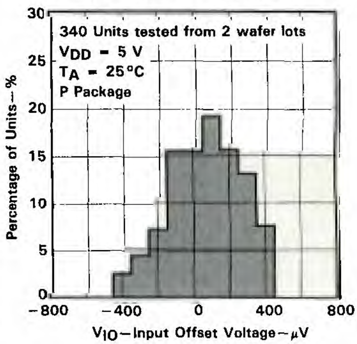
NC –No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	[illegible]	TLC27M7CD	—	[illegible]	[illegible]
	[illegible]	TLC27M2BCD	—	[illegible]	[illegible]
	5 mV	[illegible]	—	[illegible]	[illegible]
	10 mV	[illegible]	—	[illegible]	[illegible]
−40°C to 85°C	500 µV	[illegible]	—	[illegible]	[illegible]
	2 mV	[illegible]	—	[illegible]	TLC27M2BIP
	5 mV	[illegible]	—	[illegible]	[illegible]
	10 mV	[illegible]	—	[illegible]	[illegible]
−55°C to 125°C	500 µV	—	TLC27M7MFK	TLC27M7MJG	—
	10 mV	—	TLC27M2MFK	TLC27M2MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27M7CDR).

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



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description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

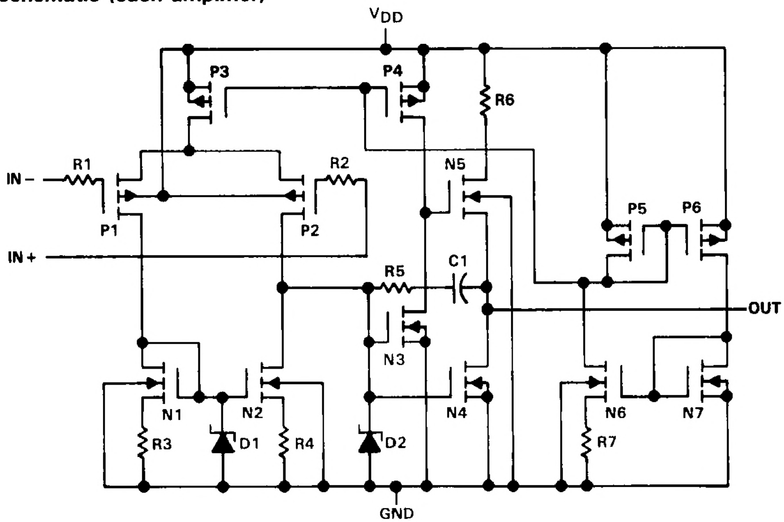
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	−55°C to 125°C
I-suffix	−40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	[illegible] mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−55°C	3	3.9		
				125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−55°C	15	290		
				125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				−55°C	60	89		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				−55°C		340	[illegible]	
				125°C		140	[illegible]	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		190	[illegible]	µV
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−55°C	7.8	8.6		
					125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−55°C	15	420		
					125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	93		
					125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		[illegible]	[illegible]	µA
					−55°C		[illegible]	[illegible]	
					125°C		[illegible]	[illegible]	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25 °C		1.1	10	mV
				Full [illegible]			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		0.9	5	
				Full [illegible]			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		220	2000	µV
				Full [illegible]			[illegible]	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		185	[illegible]	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25 °C to 85 °C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25 °C		0.1		pA
				85 °C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25 °C		0.6		pA
				85 °C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25 °C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25 °C	3.2	3.9		V
				−40 °C	3	3.9		
				85 °C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25 °C		0	50	mV
				−40 °C		0	50	
				85 °C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25 °C	25	170		V/mV
				−40 °C	15	270		
				85 °C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25 °C	65	91		dB
				−40 °C	60	90		
				85 °C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25 °C	70	93		dB
				−40 °C	60	91		
				85 °C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25 °C		[illegible]	560	µA
				−40 °C		[illegible]	[illegible]	
				85 °C		[illegible]	[illegible]	

† Full range is −40 °C to 85 °C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full [illegible]			13	mV
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		0.9	5	mV
				Full [illegible]			7	mV
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		224	[illegible]	μV
				Full range			[illegible]	μV
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	μV
				Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		[illegible]	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−40°C	7.8	8.7		V
				85°C	7.8	8.7		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	mV
				85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	[illegible]		V/mV
				−40°C	15	[illegible]		V/mV
				85°C	15	220		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−40°C	60	93		dB
				85°C	60	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		dB
				85°C	60	94		dB
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		[illegible]	600	μA
				−40°C		[illegible]	[illegible]	μA
				85°C		[illegible]	[illegible]	μA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				[illegible]			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		220	2000	μV
				Full [illegible]			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		185	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				0°C	3	3.9		
				70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				0°C	15	[illegible]		
				70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				0°C	60	91		
				70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				0°C		[illegible]	640	
				70°C		[illegible]	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full [illegible]			12	
		TLC27M2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	[illegible]		0.9	5	mV
					Full [illegible]			6.5	
		TLC27M2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	[illegible]		224	[illegible]	μV
					F[illegible]			[illegible]	
		TLC27M7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	[illegible]		190	800	μV
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	[illegible]		V/mV
					0°C	15	[illegible]		
					70°C	15	[illegible]		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	μA
					0°C		345	800	
					70°C		[illegible]	[illegible]	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

TEXAS INSTRUMENTS
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operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.49		
				[illegible]		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		[illegible]		
				85°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

TEXAS INSTRUMENTS
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operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		[illegible]		
				70°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				[illegible]		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

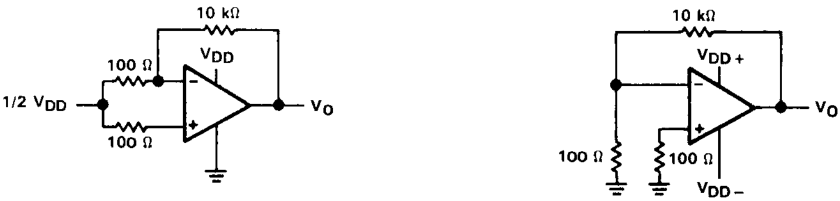
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

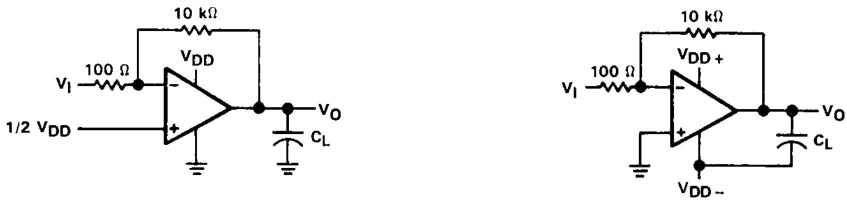
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

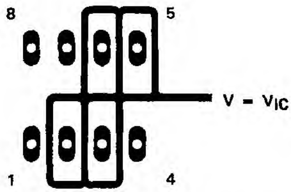


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

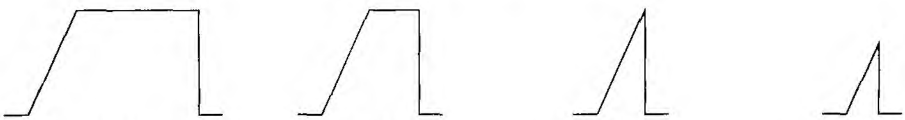
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) $f = 1$ kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

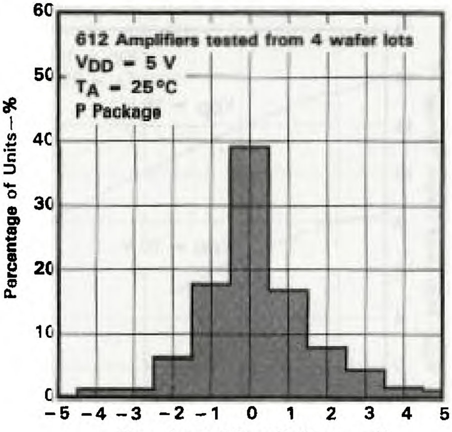


FIGURE 6

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

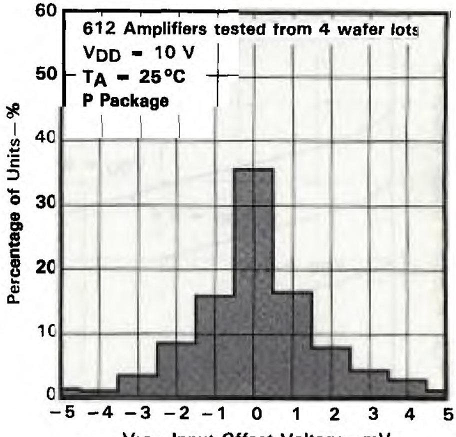


FIGURE 7

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

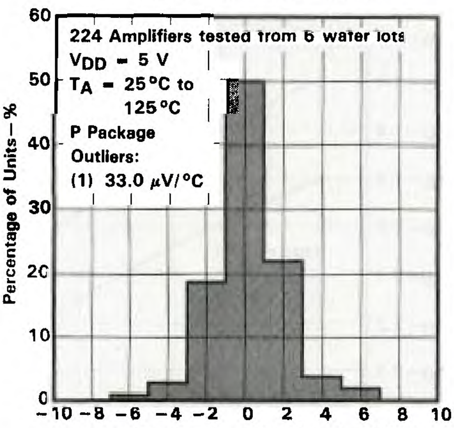


FIGURE 8

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

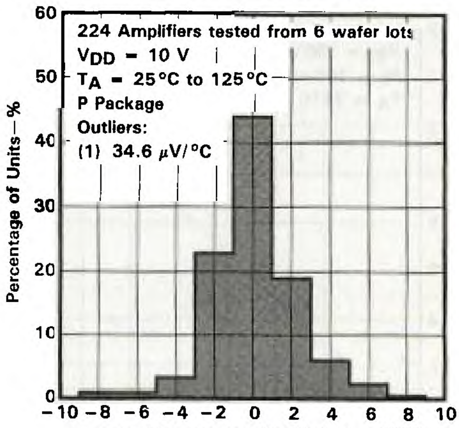


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

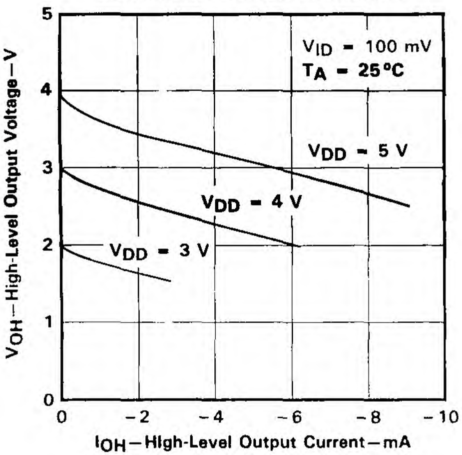


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

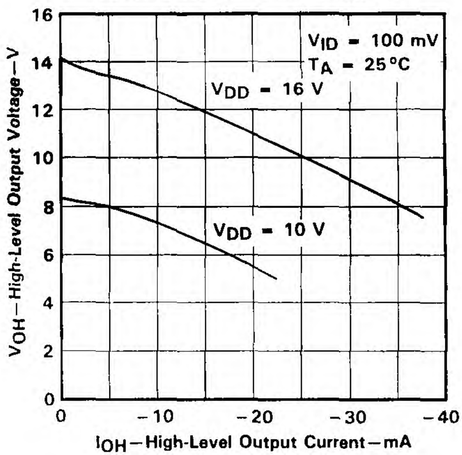


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

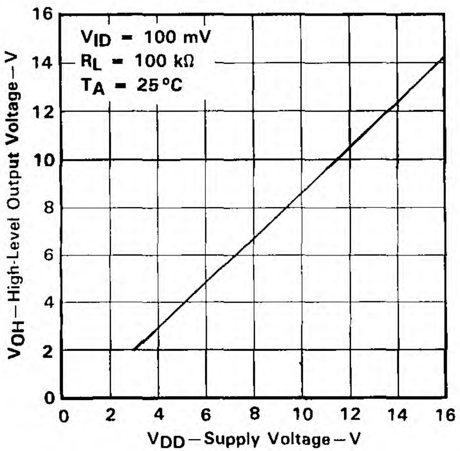


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

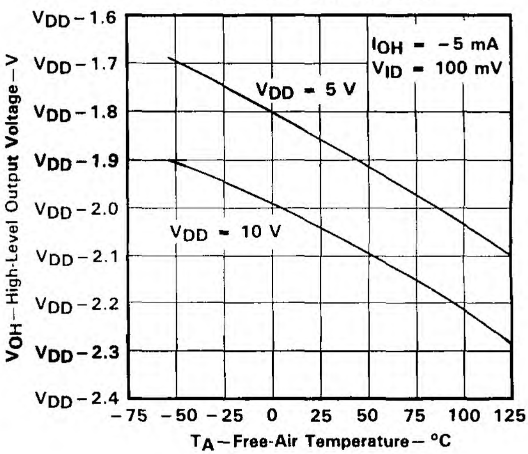


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

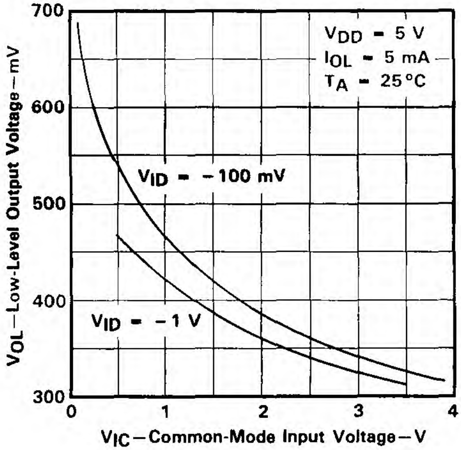


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

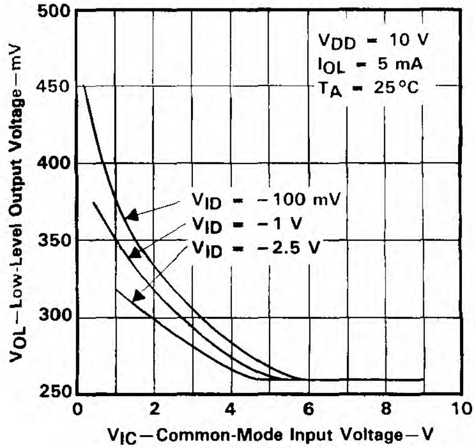


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

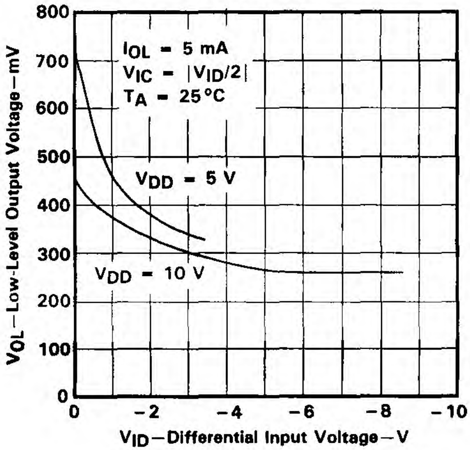


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

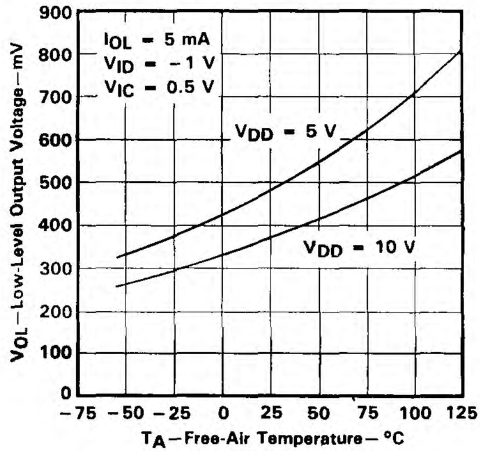


FIGURE 17

2
Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

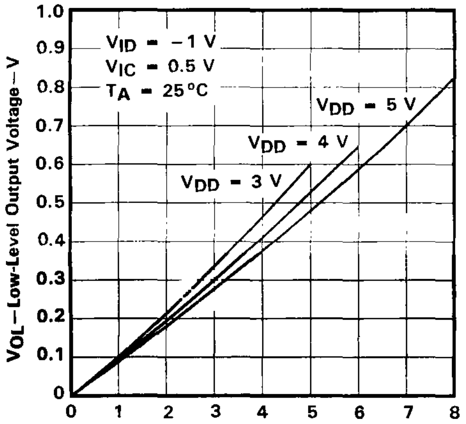


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

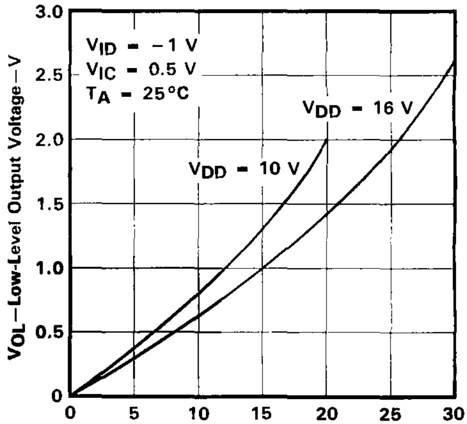


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

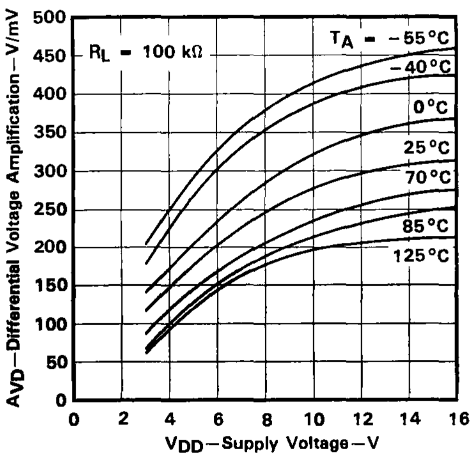


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

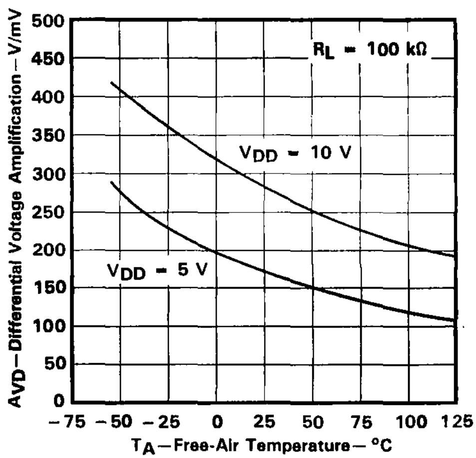


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

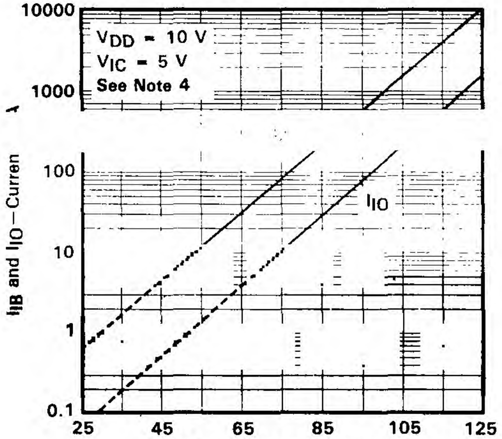


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

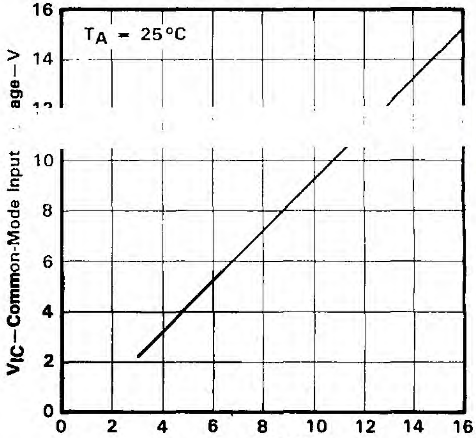


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

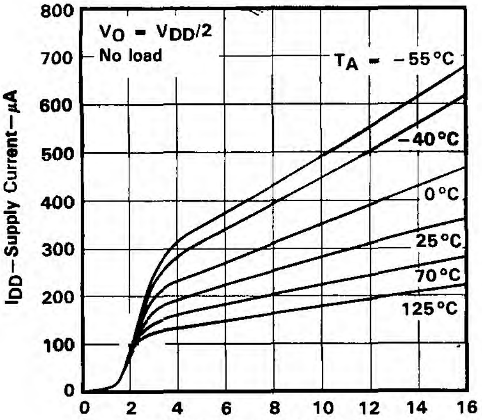


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

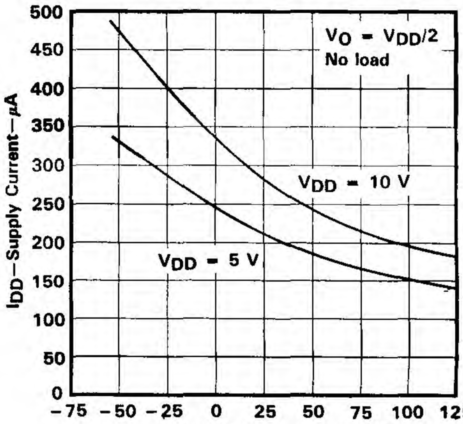


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

2
Operational Amplifiers

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

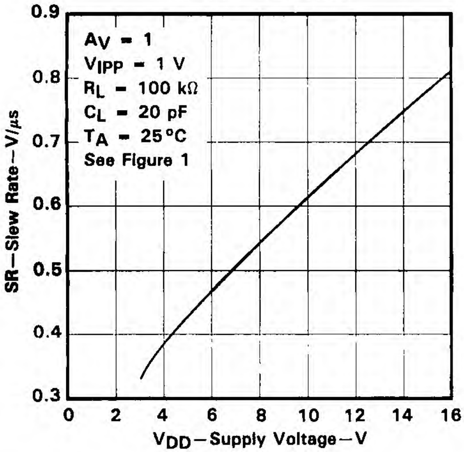


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

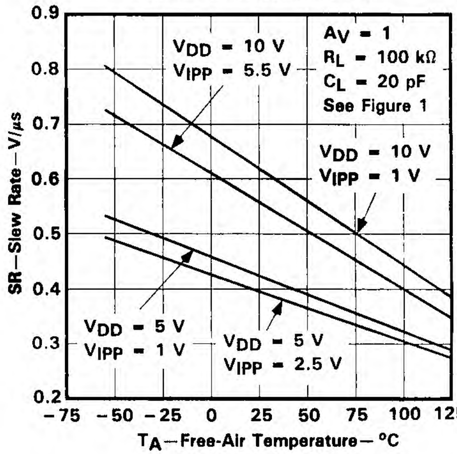


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

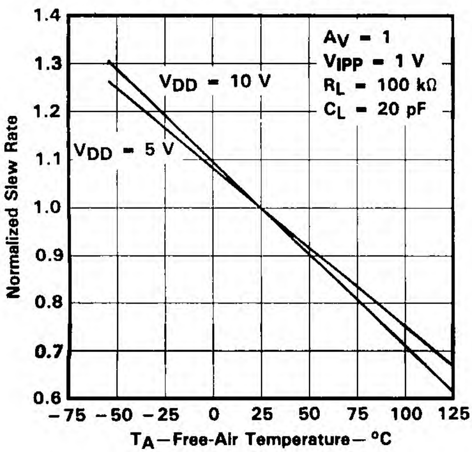


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

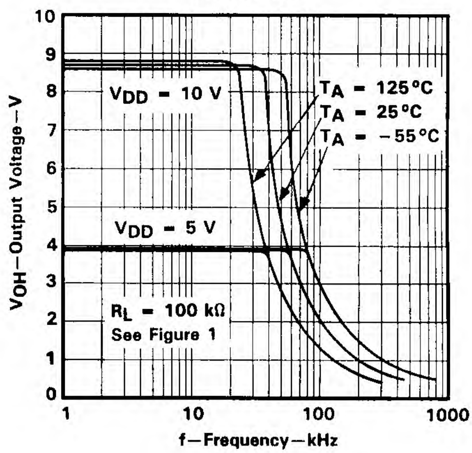


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

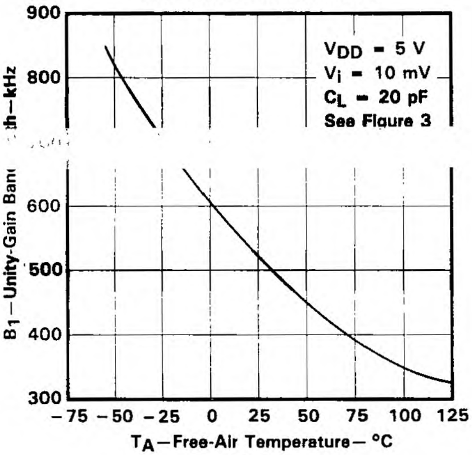


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

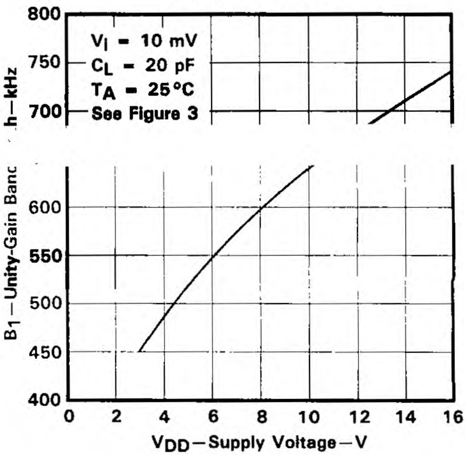


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

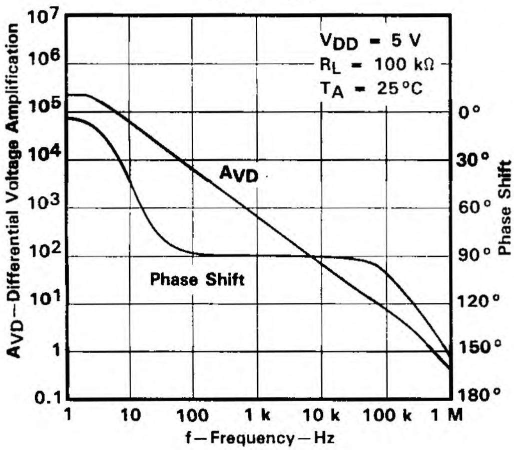


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

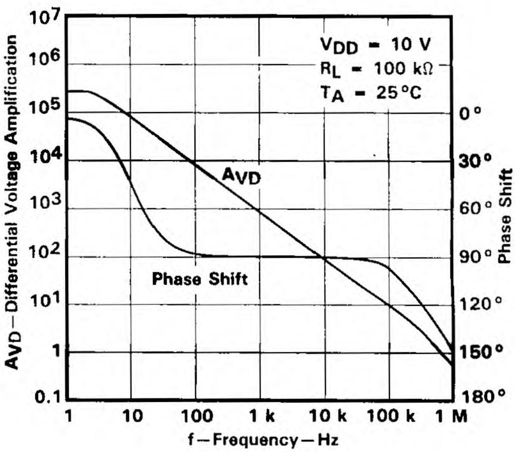


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

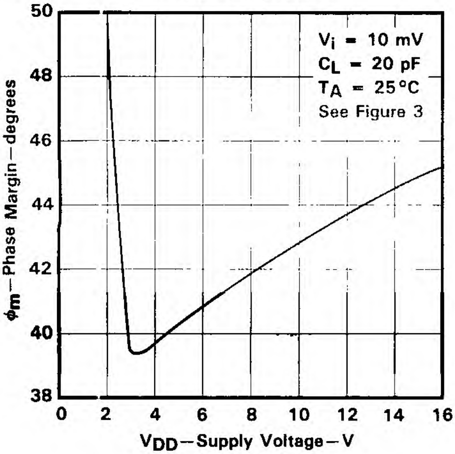


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

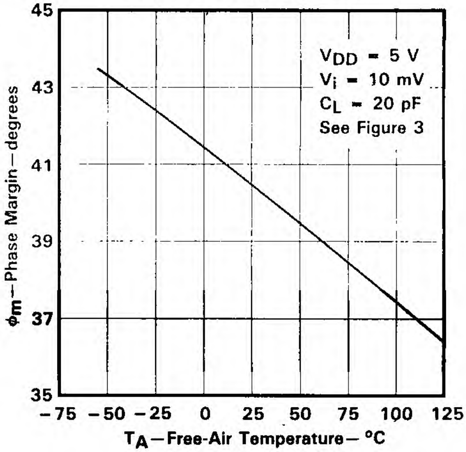


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

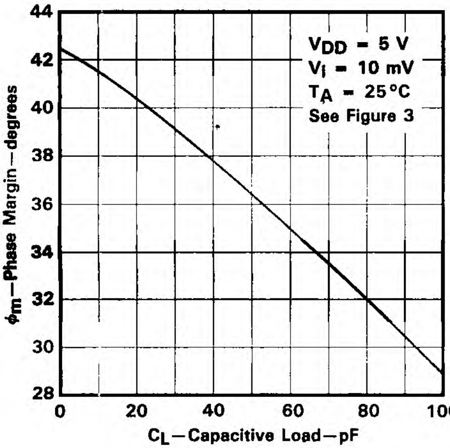


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

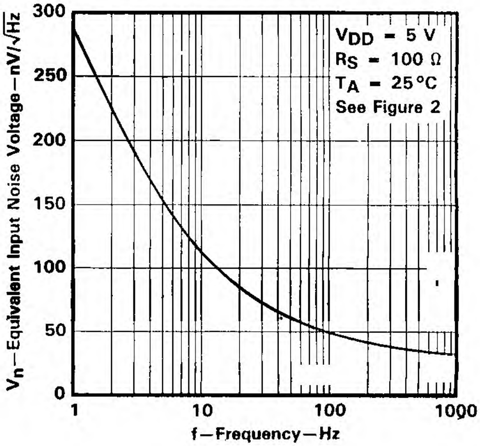


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

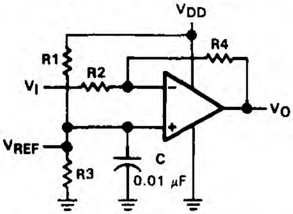
single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

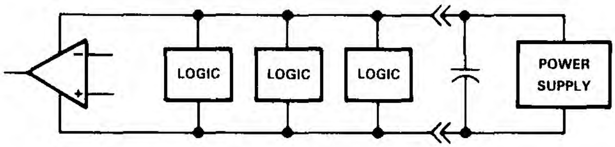
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



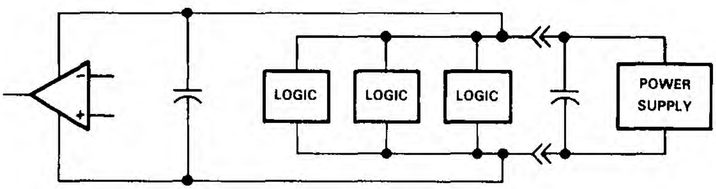
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

2 Operational Amplifiers

TYPICAL APPLICATION DATA

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

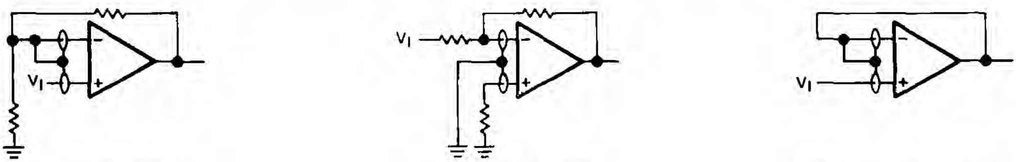
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

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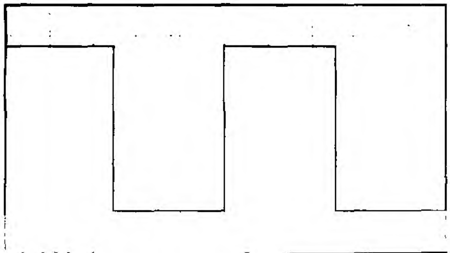
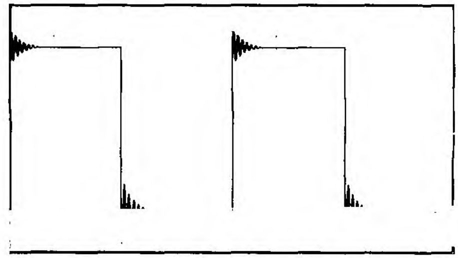
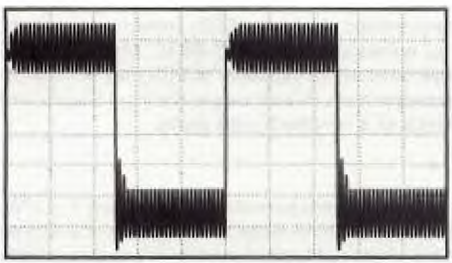
TYPICAL APPLICATION DATA



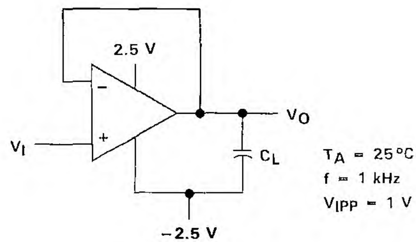
(a) C_L = 20 pF, R_L = no load



(b) C_L = 170 pF, R_L = no load



(c) C_L = 190 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of Rp, a voltage offset from 0 V at the output will occur. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA

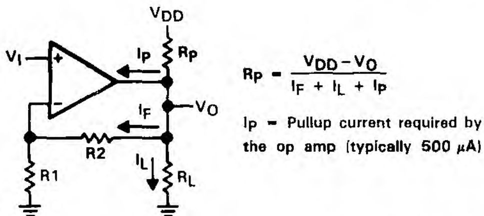


FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

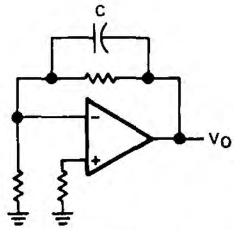


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

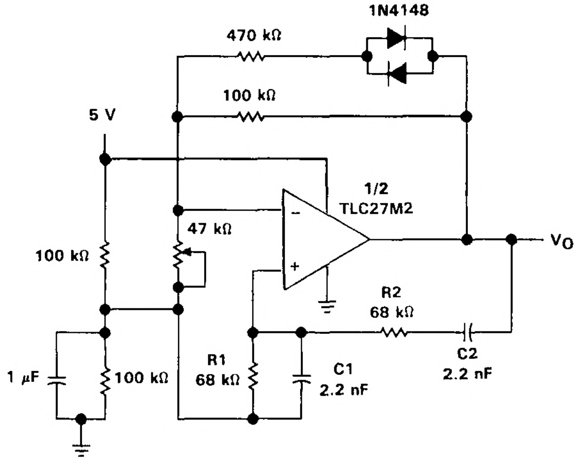
The TLC27M2 and TLC27M7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

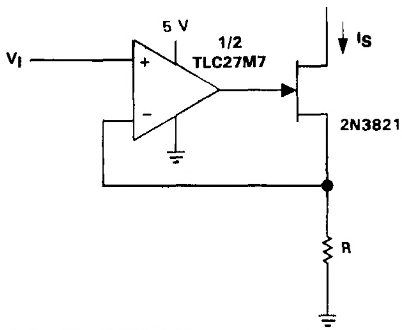
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi \sqrt{R1\,R2\,C1\,C2}}$$

FIGURE 44. WIEN OSCILLATOR

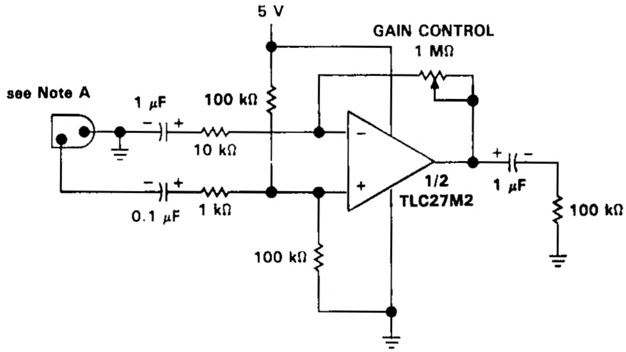


NOTES: V_I = 0 V to 3 V

$$I_S = \frac{V_I}{R}$$

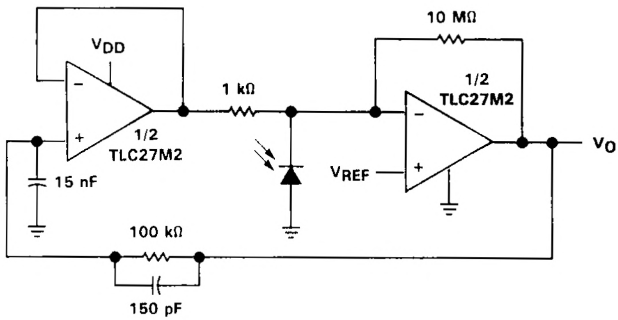
FIGURE 45. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A.: Low to medium impedance dynamic mike

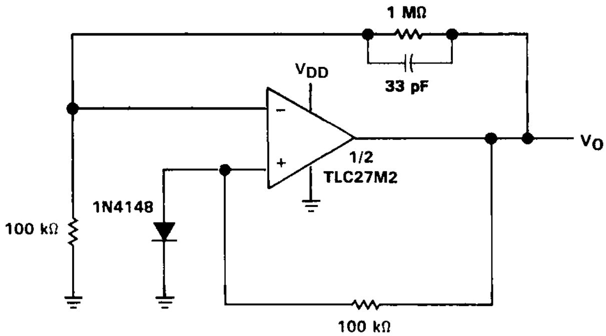
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

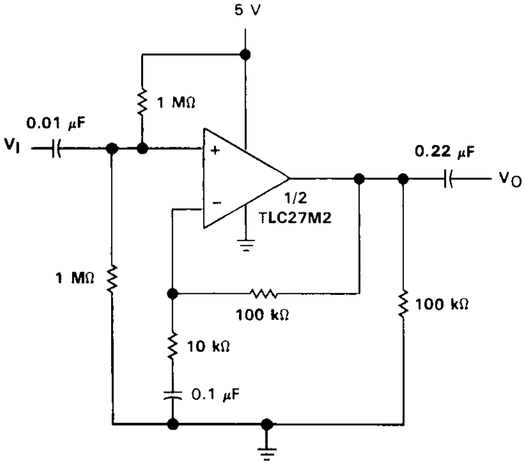
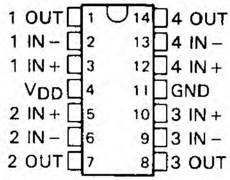


FIGURE 49. SINGLE-RAIL AC AMPLIFIER

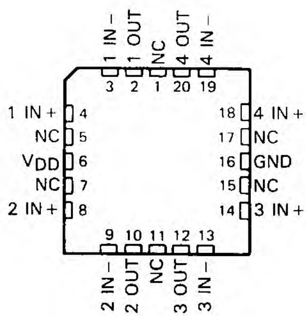
D3143, OCTOBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage: TLC27M9 . . . 900 μV Max at 25 °C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/√Hz at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



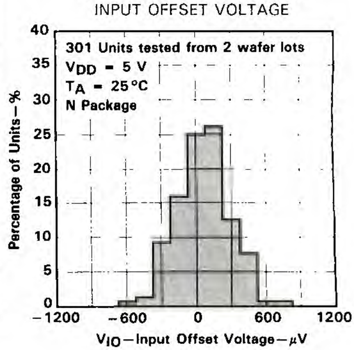
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE SMALL OUTLINE (D)	PACKAGE CHIP CARRIER (FK)	PACKAGE CERAMIC DIP (J)	PACKAGE PLASTIC DIP (N)
0°C to 70°C	[illegible] μV	[illegible]	—	[illegible]	[illegible]
	[illegible] mV	[illegible]	—	[illegible]	[illegible]
	5 mV	[illegible]M4[illegible]	—	[illegible]M4ACJ	[illegible]M4ACN
	10 mV	[illegible]M4[illegible]	—	[illegible]M4CJ	[illegible]M4CN
−40°C to 85°C	900 μV	TLC27M9ID	—	TLC2[illegible]	[illegible]
	2 mV	TLC27M4BID	—	TLC2[illegible]	[illegible]
	5 mV	[illegible]4AID	—	[illegible]M4AIJ	[illegible]M4A[illegible]
	10 mV	[illegible]4ID	—	[illegible]M4IJ	[illegible]M4IN
−55°C to 125°C	900 μV	—	TLC27M9MFK	TLC27M9MJ	—
	10 mV	—	TLC27M4MFK	TLC27M4MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27M9CDR).

DISTRIBUTION OF TLC27M9
INPUT OFFSET VOLTAGE



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description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

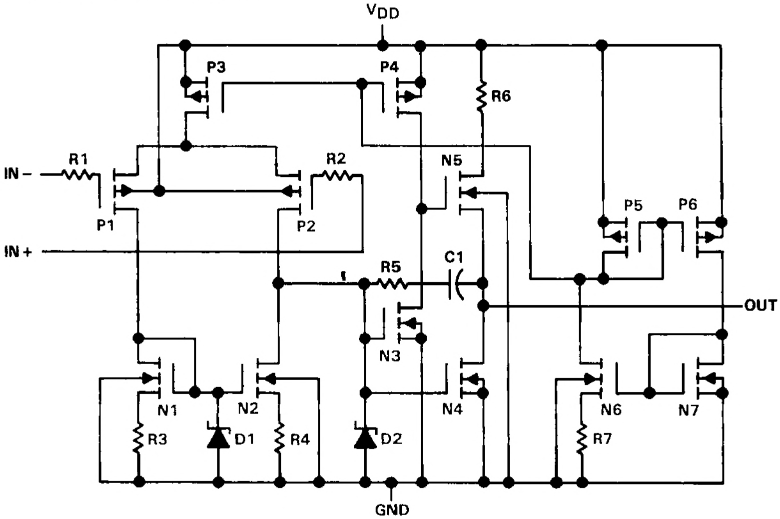
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25 °C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	−55 °C to 125 °C
I-suffix	−40 °C to 85 °C
C-suffix	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C
Case temperature for 60 seconds: FK package	260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package	260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300 °C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$ °C POWER RATING	DERATING FACTOR ABOVE $T_A = 25$ °C	$T_A = 70$ °C POWER RATING	$T_A = 85$ °C POWER RATING	$T_A = 125$ °C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M SUFFIX			I-SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		[illegible]	−0.2		8.5	V
Operating free-air temperature, T_A		−55		[illegible]	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full			12	mV
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	[illegible]		210	900	μV
					Full range			3750	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−55°C	3	3.9		
					125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−55°C	15	290		
					125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					−55°C	60	89		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		[illegible]	1120	μA
					−55°C		[illegible]	1760	
					125°C		280	720	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25 °C		1.1	10	mV
					Full [illegible]			12	mV
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	[illegible]		220	1200	μV
					Full range			4300	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25 °C to 125 °C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25 °C		0.1		pA
					125 °C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25 °C		0.7		pA
					125 °C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25 °C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25 °C	8	8.7		V
					−55 °C	7.8	8.6		V
					125 °C	7.8	8.8		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25 °C		0	50	mV
					−55 °C		0	50	mV
					125 °C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25 °C	25	275		V/mV
					−55 °C	15	420		V/mV
					125 °C	15	190		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25 °C	65	94		dB
					−55 °C	60	93		dB
					125 °C	60	93		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25 °C	70	93		dB
					−55 °C	60	91		dB
					[illegible] C	60	94		dB
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	[illegible] C		570	[illegible]	μA
					−55 °C		[illegible]	[illegible]	μA
					125 °C		360	960	μA

† Full range is −55 °C to 125 °C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full [illegible]			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		0.9	5	
				Full [illegible]			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		250	2000	µV
				Full [illegible]			[illegible]	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	[illegible]		210	[illegible]	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		[illegible]	[illegible]	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−40°C	3	3.9		
				85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−40°C	15	270		
				85°C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				−40°C	60	90		
				85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		420	1120	µA
				−40°C		630	1600	
				85°C		320	800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full [illegible]			13	mV
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	[illegible]		0.9	5	mV
					Full range			7	mV
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	[illegible]	μV
					Full range			[illegible]	μV
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		[illegible]	[illegible]	μV
					Full range			[illegible]	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		[illegible]	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−40°C	7.8	8.7		V
					85°C	7.8	8.7		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	mV
					85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−40°C	15	390		V/mV
					85°C	15	220		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	93		dB
					85°C	60	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		dB
					85°C	60	94		dB
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	[illegible]	μA
					−40°C		900	[illegible]	μA
					85°C		410	1040	μA

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	[illegible]	µV
				Full range			[illegible]	µV
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			1500	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				0°C	3	3.9		V
				70°C	3	4		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	mV
				70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				0°C	15	200		V/mV
				70°C	15	[illegible]		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				0°C	60	91		dB
				70°C	60	92		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		dB
				70°C	60	94		dB
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		[illegible]	[illegible]	µA
				0°C		[illegible]	[illegible]	µA
				70°C		340	880	µA

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	μV
					Full range			3000	
		TLC27M9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	[illegible]	
					Full range			[illegible]	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					0°C	15	[illegible]		
					70°C	15	[illegible]		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	[illegible]	μA
					0°C		[illegible]	[illegible]	
					70°C		440	[illegible]	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		[illegible]		kHz
				−55°C		[illegible]		
				125°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				[illegible]		[illegible]		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	[illegible]		[illegible]		kHz
				−55°C		[illegible]		
				[illegible]		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

2

Operational Amplifiers

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		[illegible]		kHz
				−40°C		[illegible]		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		610		
				70°C		[illegible]		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		4[illegible]		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

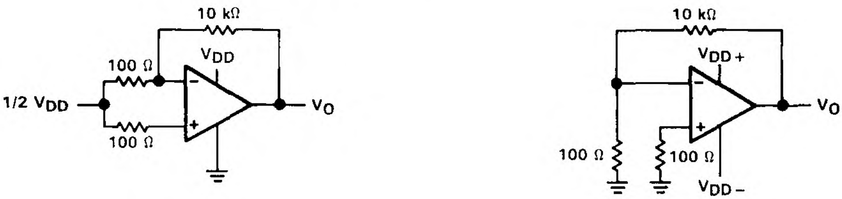
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

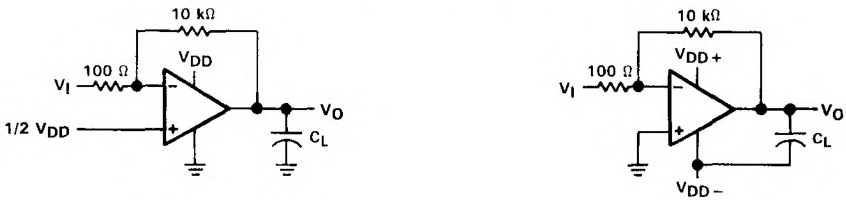
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply **(b) Split-Supply**

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

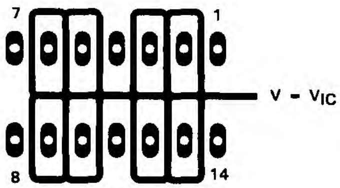


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

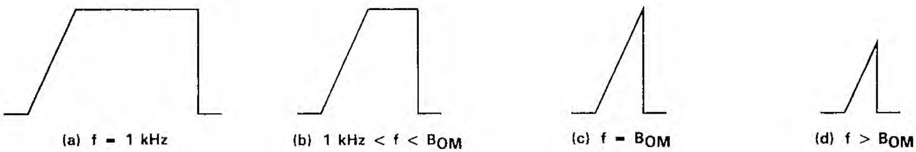


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

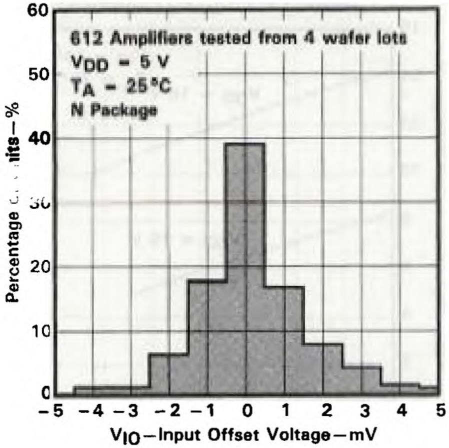

FIGURE 6

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

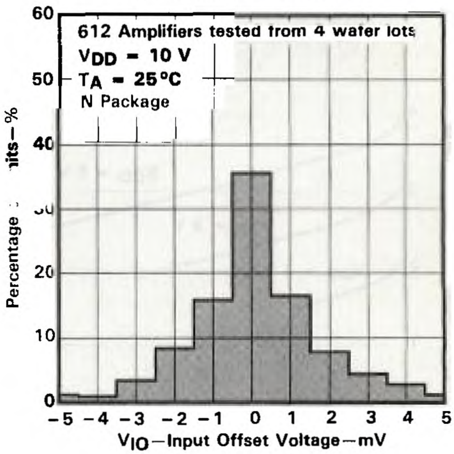

FIGURE 7

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

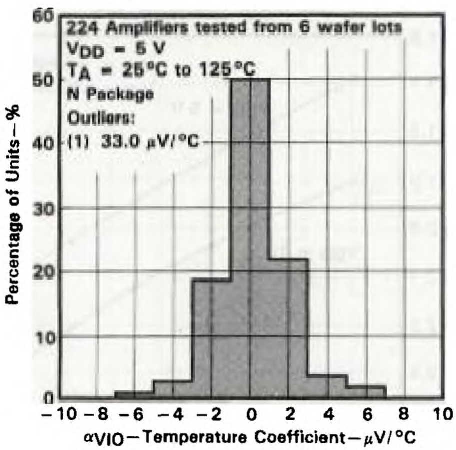

FIGURE 8

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

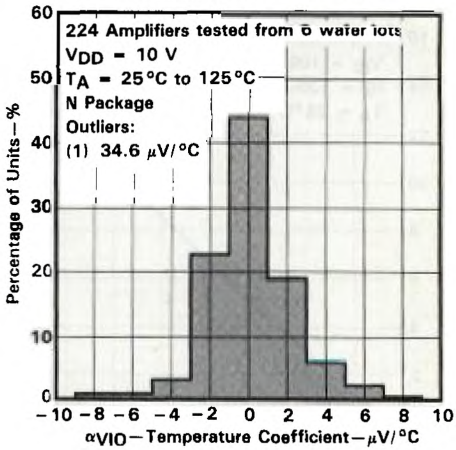

FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

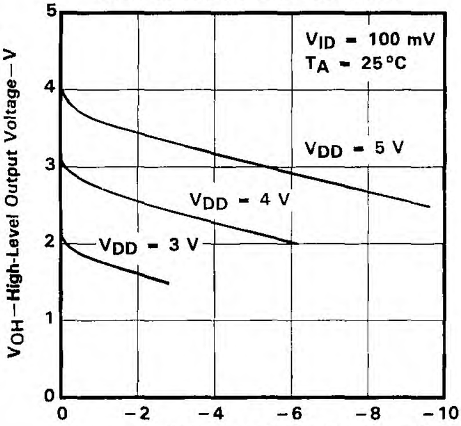

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

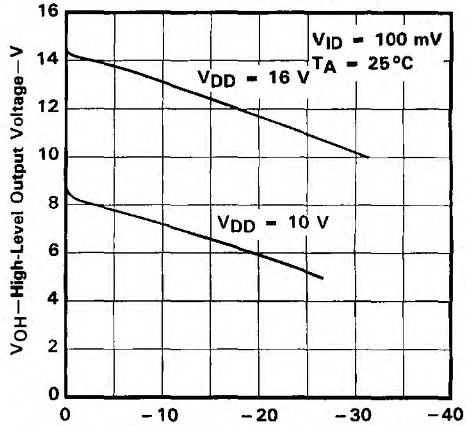

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

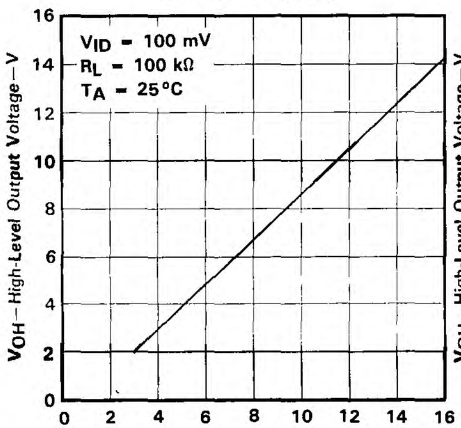

FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

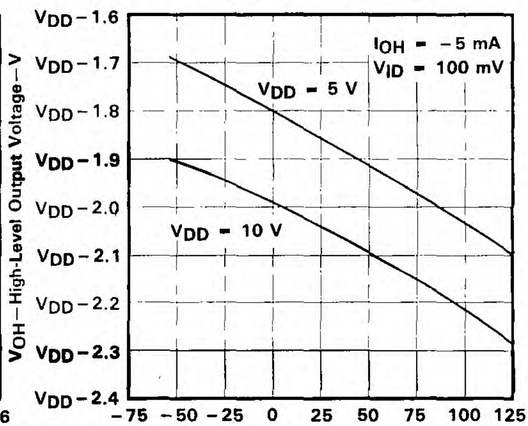

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

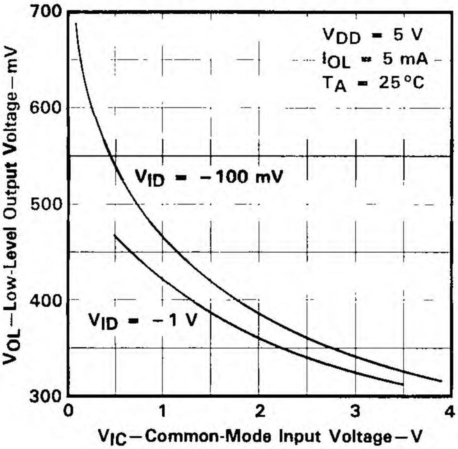

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

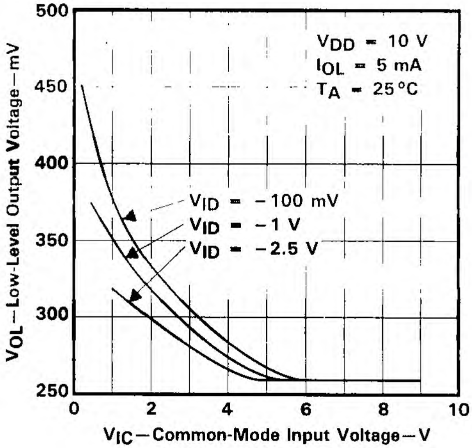

FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

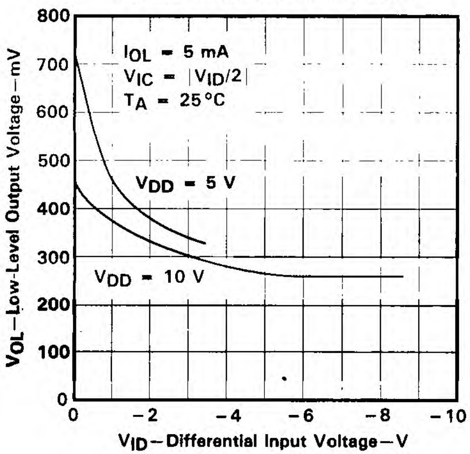

FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

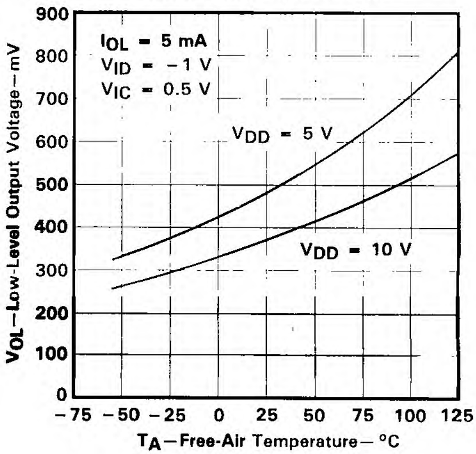

FIGURE 17

2
Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

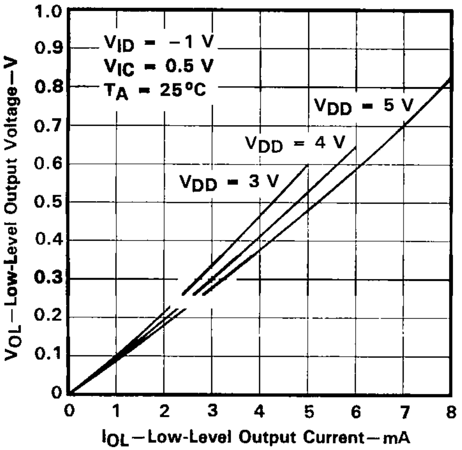

FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

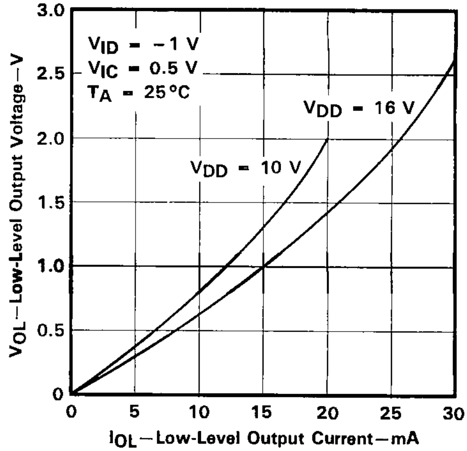

FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

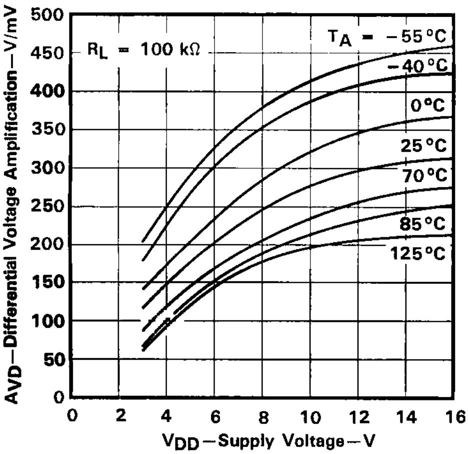

FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

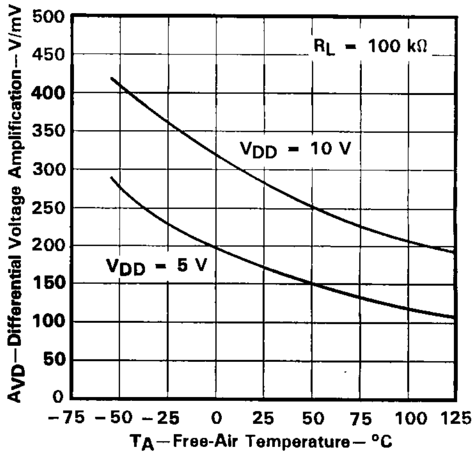

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

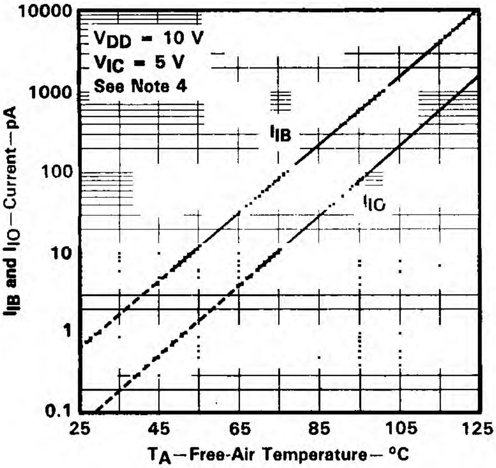


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

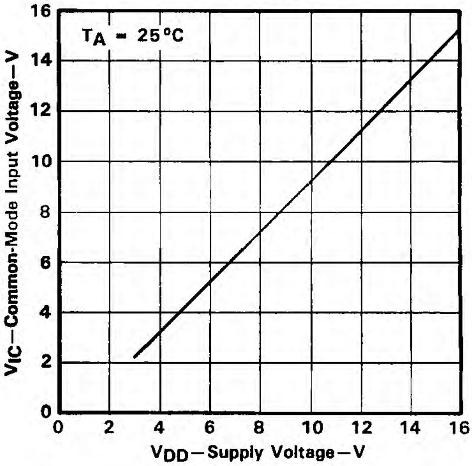


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

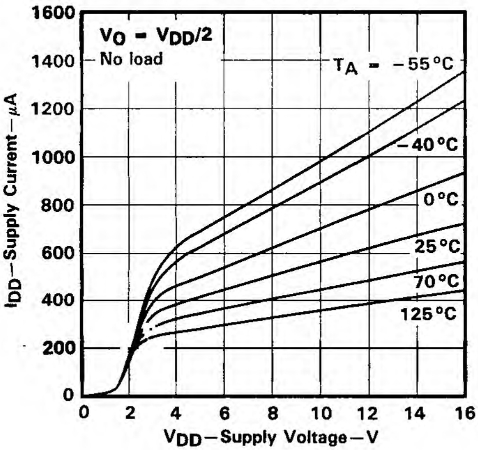


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

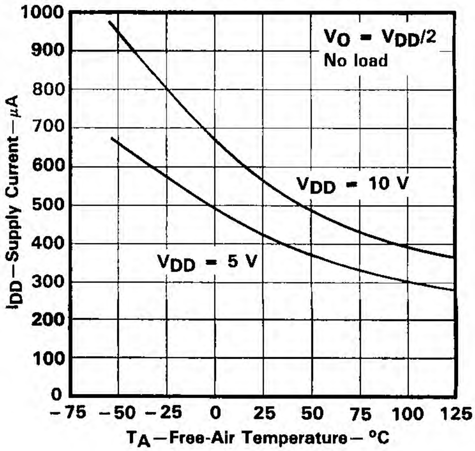


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

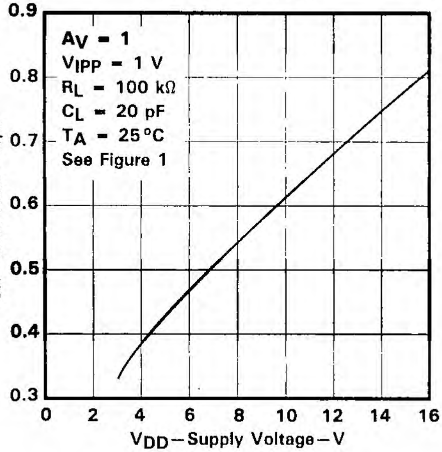


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

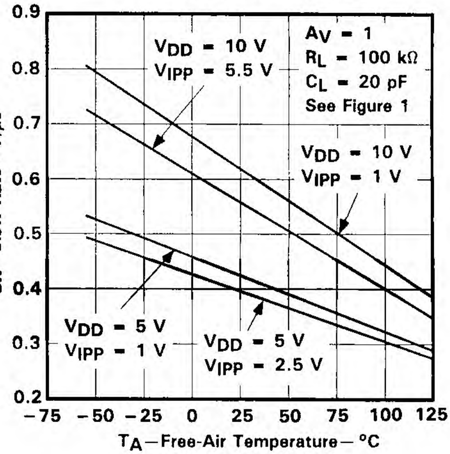


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

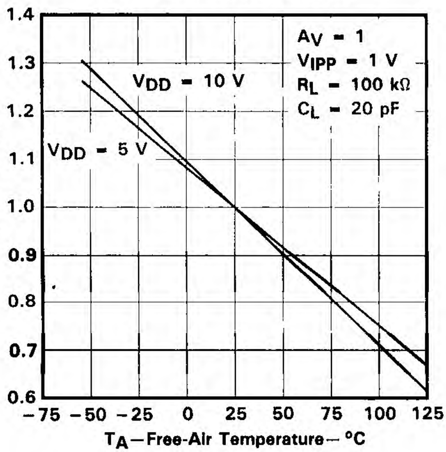


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

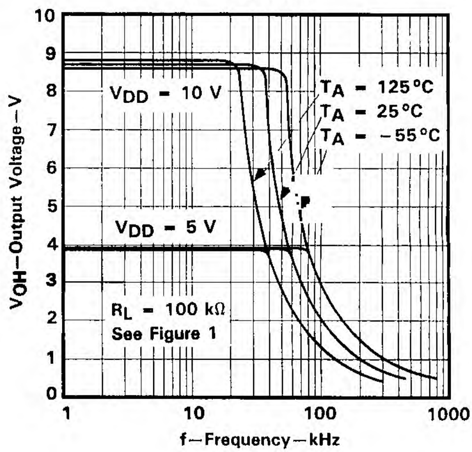


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

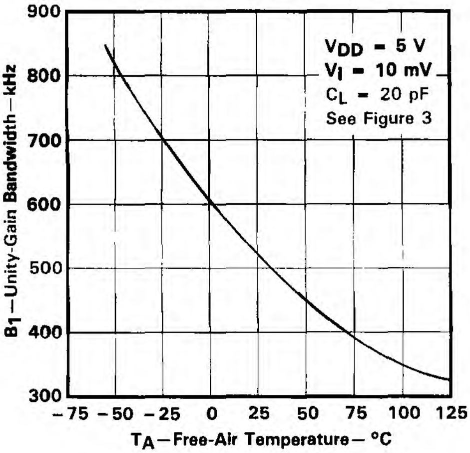


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

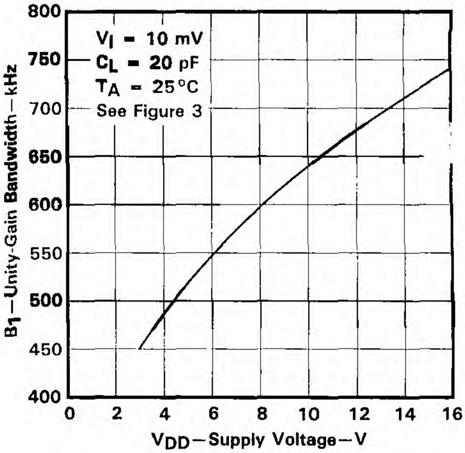


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

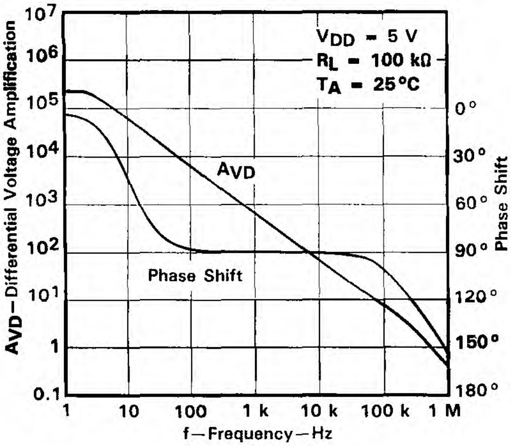


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

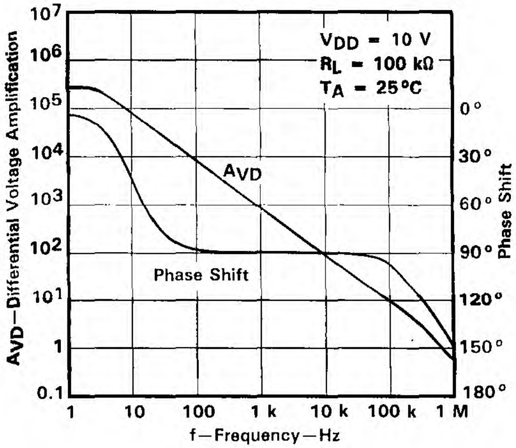


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

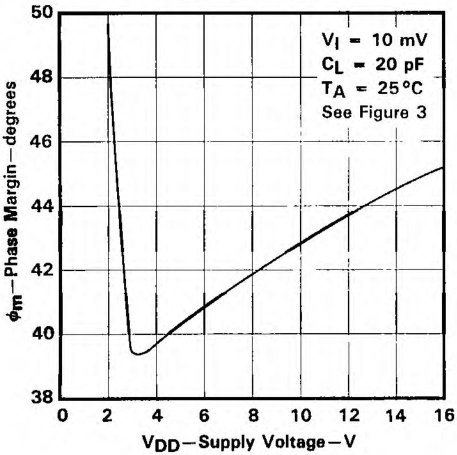


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

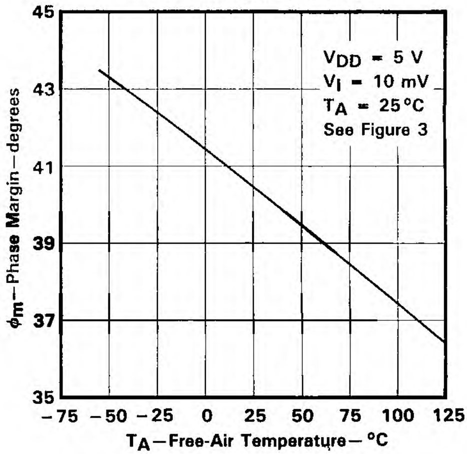


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

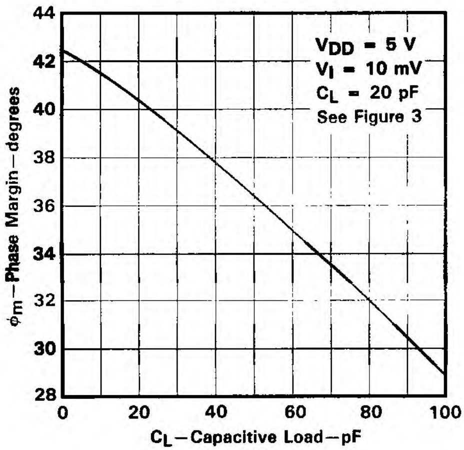


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

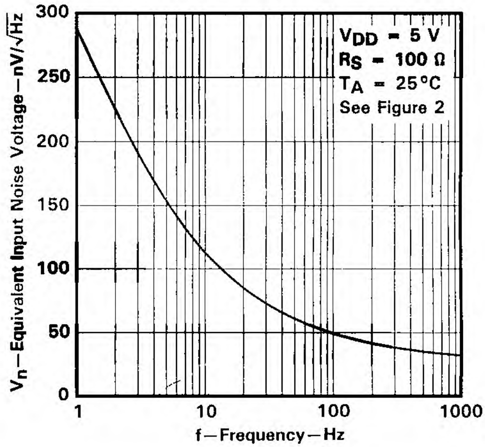


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

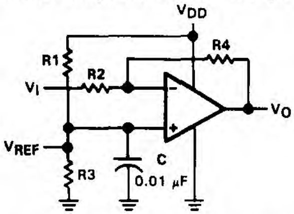
single-supply operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

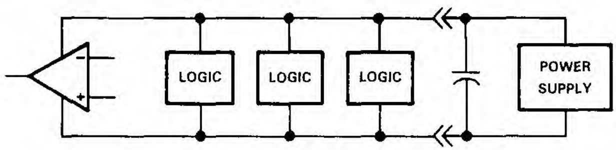
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



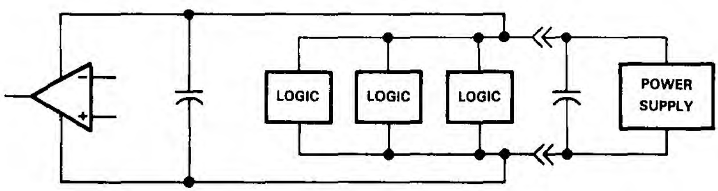
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

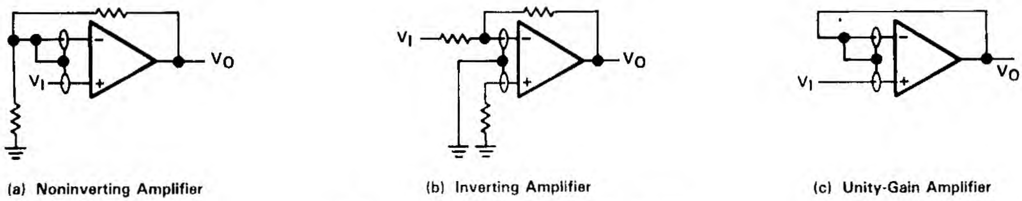


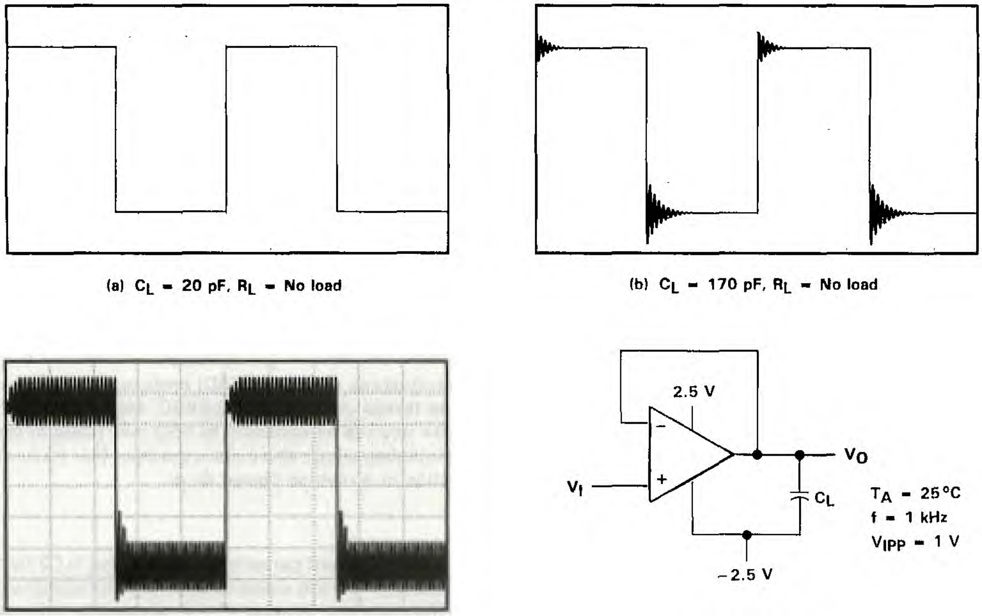
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 170 pF, R_L = No load

(c) C_L = 190 pF, R_L = No load

(d) Test Circuit

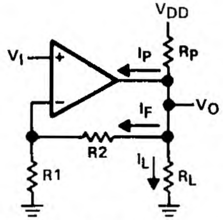
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

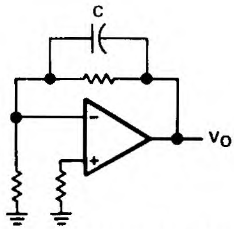


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

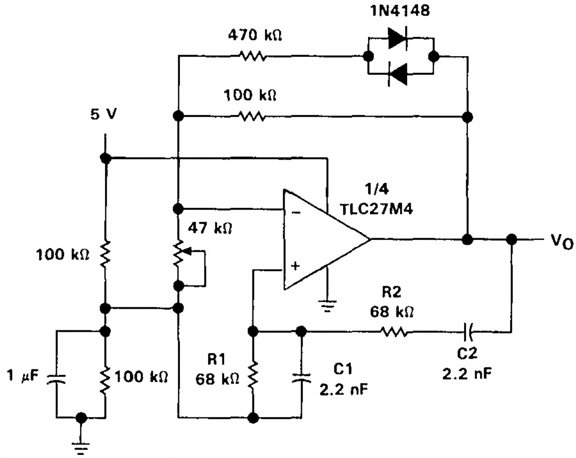
The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

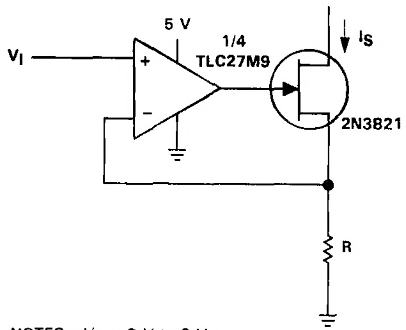
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2\ V$

$f_O = \frac{1}{2\pi \sqrt{R \quad C2}}$

FIGURE 44. WIEN OSCILLATOR



NOTES: $V_I = 0\ V$ to $3\ V$

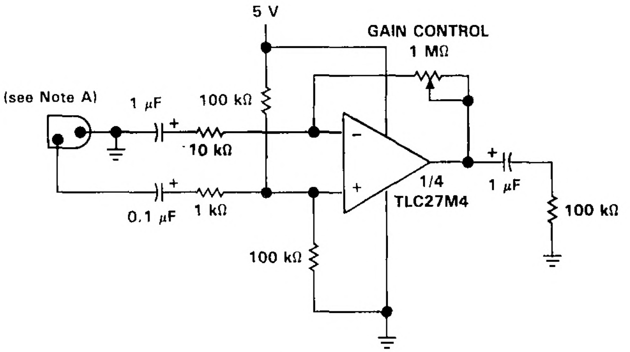
$I_S = \frac{V_I}{R}$

FIGURE 45. PRECISION LOW-CURRENT SINK

2

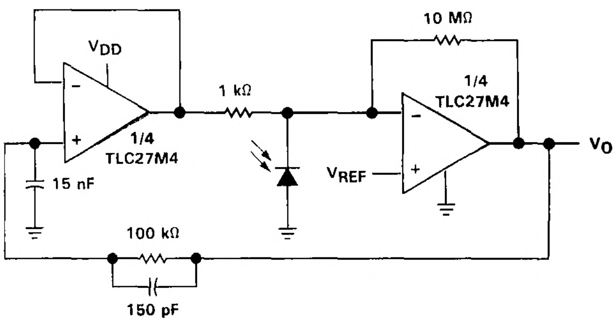
Operational Amplifiers

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike.

FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

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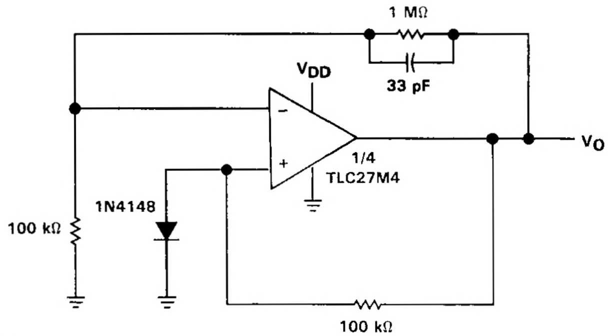
TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

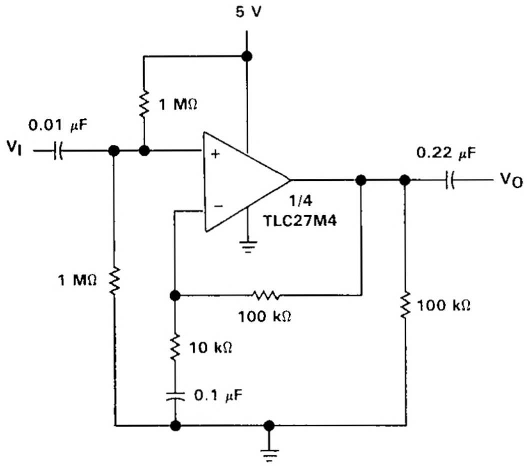
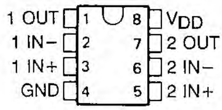


FIGURE 49. SINGLE-RAIL AC AMPLIFIER

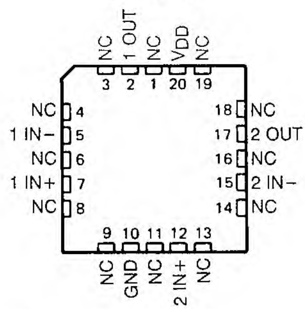
D3146, AUGUST 1988 – REVISED OCTOBER 1988

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 450 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

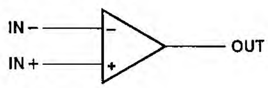
The TLC1078 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1078C is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC1078 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

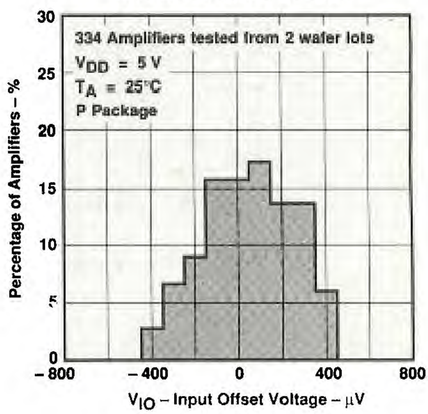
Since this device is functionally compatible as well as pin compatible with the TLC27L2 and TLC27L7, the TLC1078 easily upgrades existing designs that can benefit from its improved performance.

The TLC1078 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

symbol (each amplifier)



DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1078 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

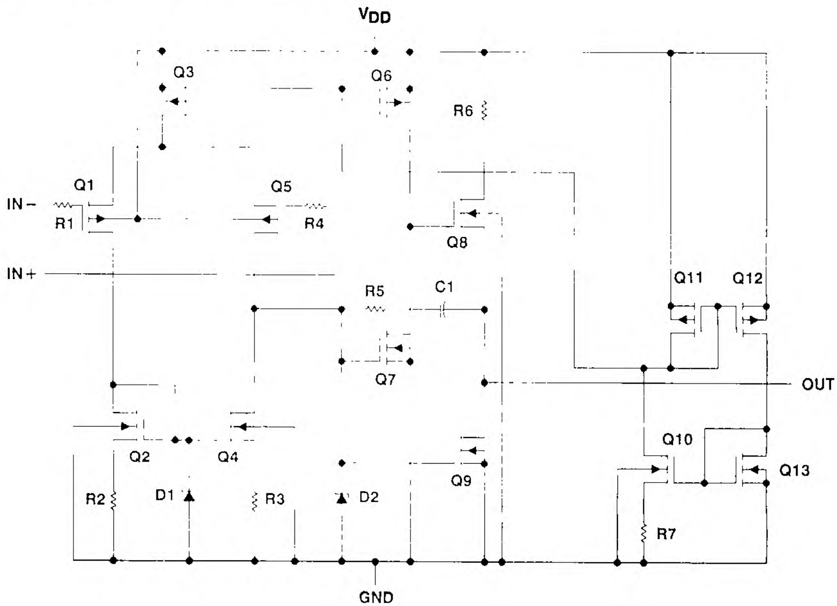
The M- suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I- suffix devices are characterized for operation from −40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D) SEE NOTE 1	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1078CD	—	TLC10[illegible]	TLC1078CP
−40°C to 85°C	TLC1078ID	—	TLC10[illegible]	TLC1078IP
−55°C to 125°C	—	TLC1078MFK	TLC1078MJG	—

NOTE 1: The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).

equivalent schematic (each amplifier)



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2)		18 V
Different input voltage (see Note 3)		$\pm V_{DD}$
Input voltage range, V_I (any input)		−0.3 V to V_{DD}
Input current, I_I (each input)		±5 mA
Output current, I_O (each output)		±30 mA
Total current into V_{DD} terminal (see Note 4)		45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)		Unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature, T_A:	M-suffix	−55°C to 125°C
	I-suffix	−40°C to 85°C
	C-suffix	0°C to 70°C
Storage temperature range		−65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		4	−0.2		4	−0.2		4	V
	V_{DD} = 10 V	0		9	−0.2		9	−0.2		9	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ See Note 7	25°C	[illegible]	525		500	850		V/mV
			0°C		680		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		20	34		29	46	μA
			0°C		24	42		36	66	
			70°C		16	28		22	40	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

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electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			950			1100	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C				500	850		V/mV
			−40°C				500	1550		
			85°C	150	300		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			−40°C		31	54		50	86	
			85°C		15	26		20	36	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

2

Operational Amplifiers

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			1250			1400	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	95		75	[illegible]		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (two amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		20	34		29	46	μA
			−55°C		35	60		56	96	
			125°C		14	24		18	30	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	lent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

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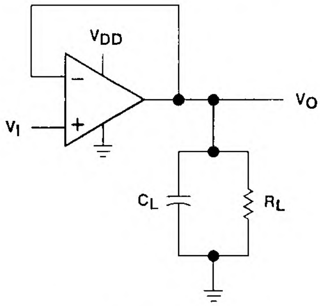
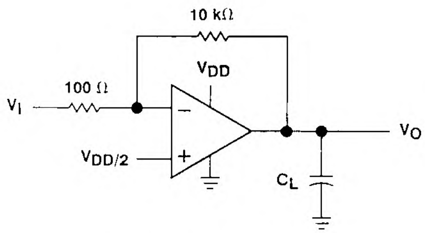
PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

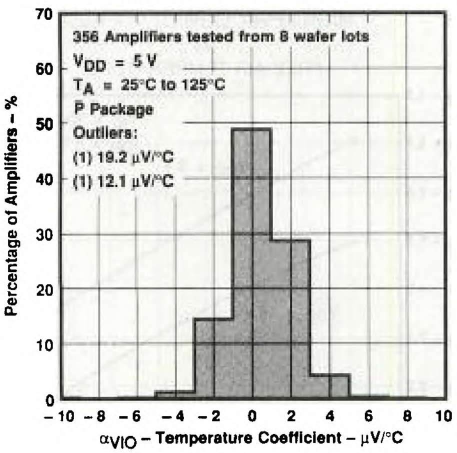


FIGURE 3

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

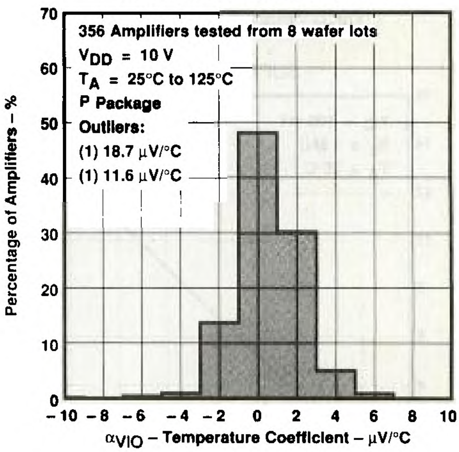


FIGURE 4

2
Operational Amplifiers

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

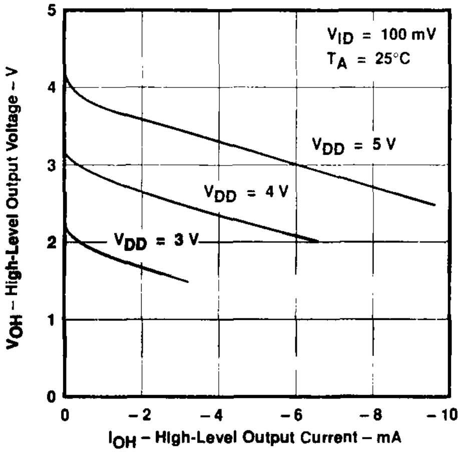


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

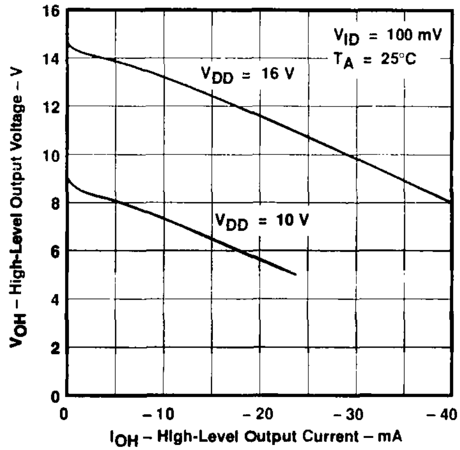


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

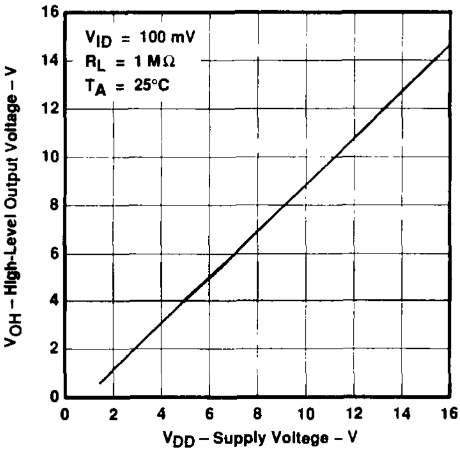


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

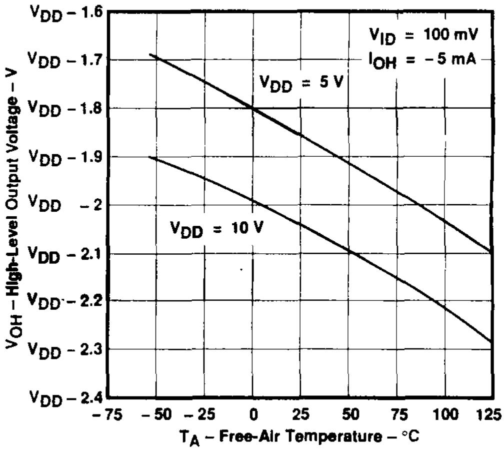


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

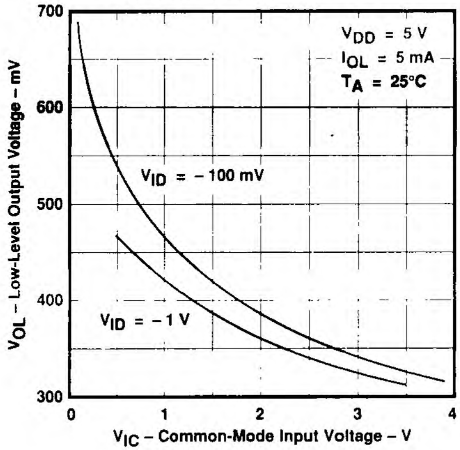


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

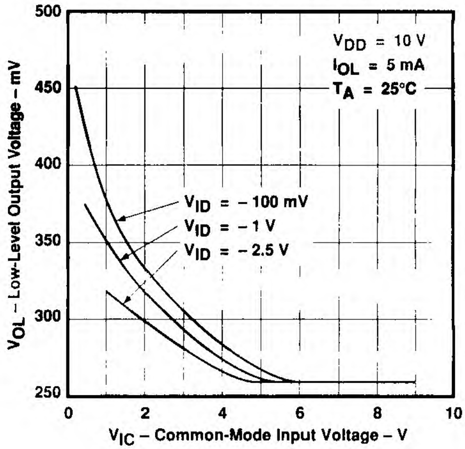


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

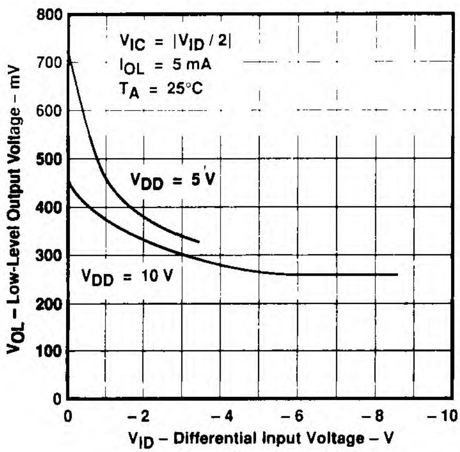


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

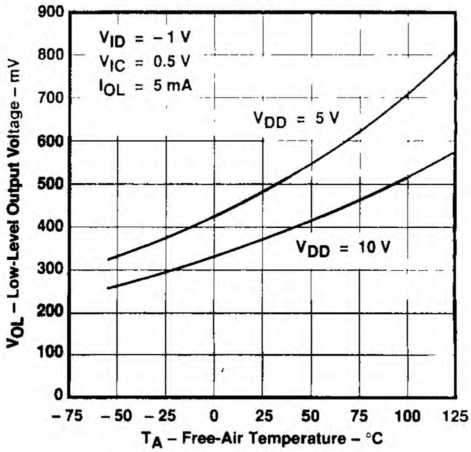


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

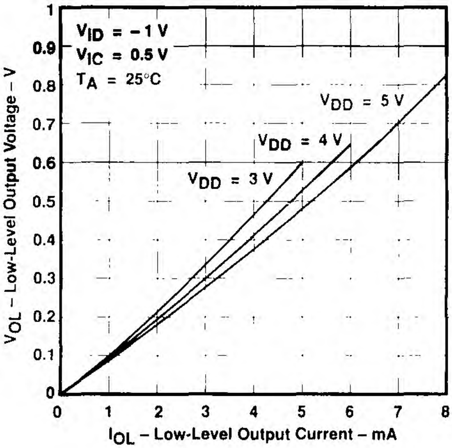


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

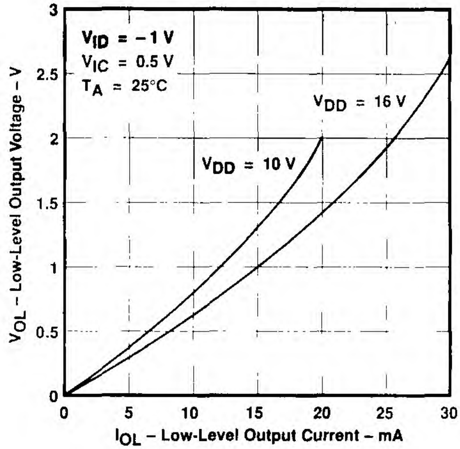


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

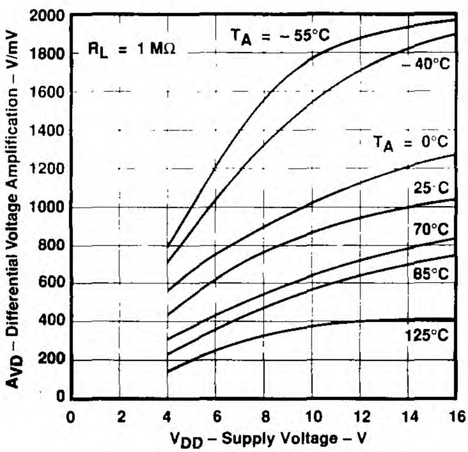


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

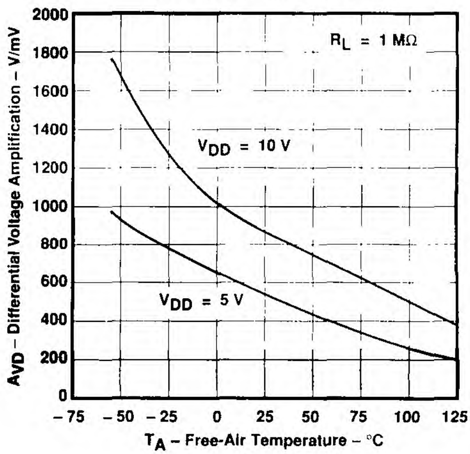


FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

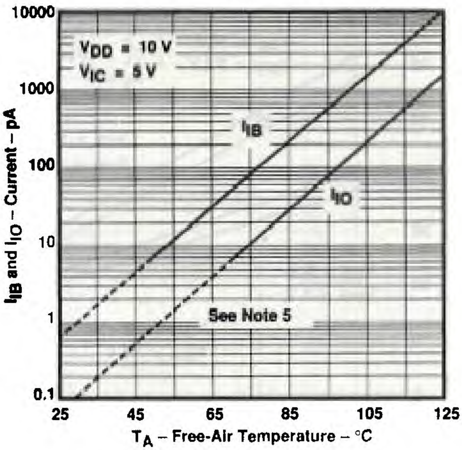

FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

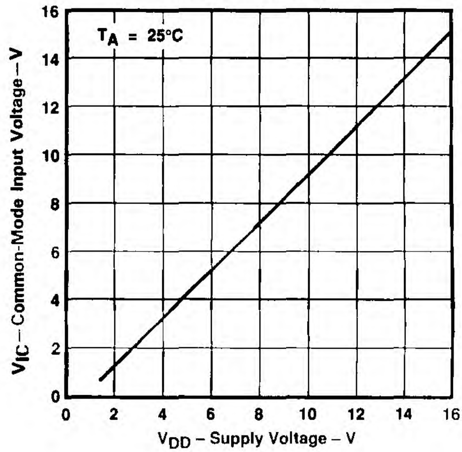

FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

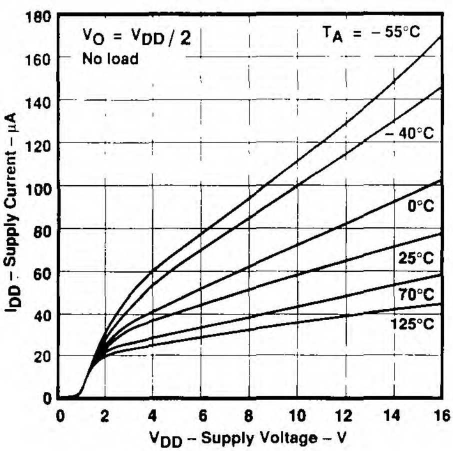

FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

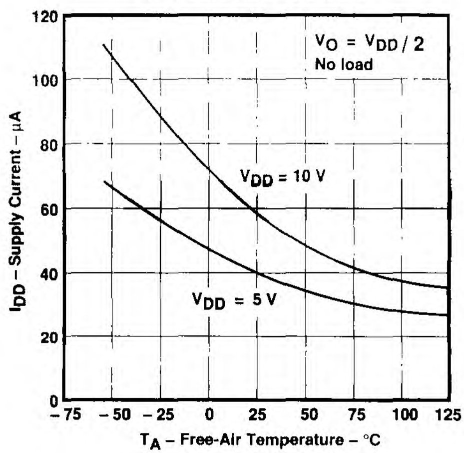

FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathmatically.

2

Operational Amplifiers

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

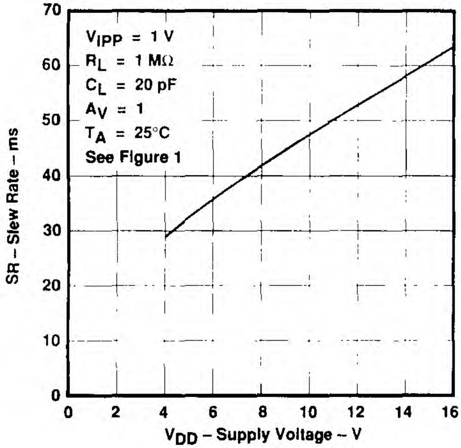

FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

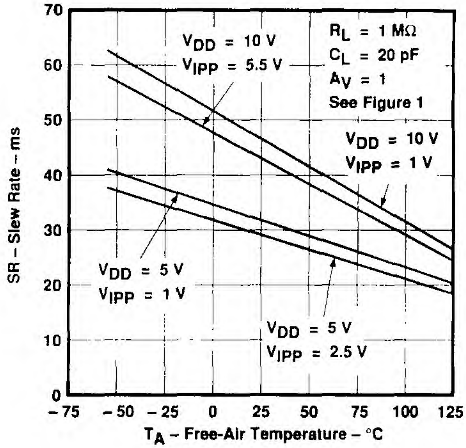

FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

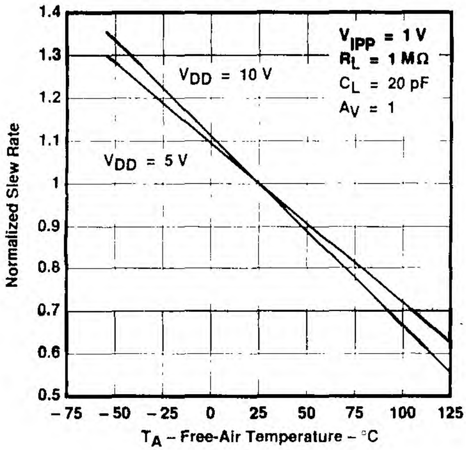

FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

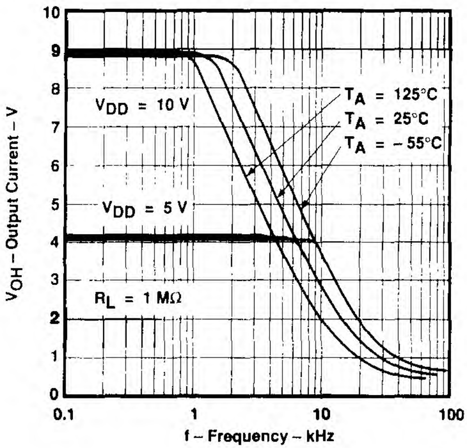

FIGURE 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

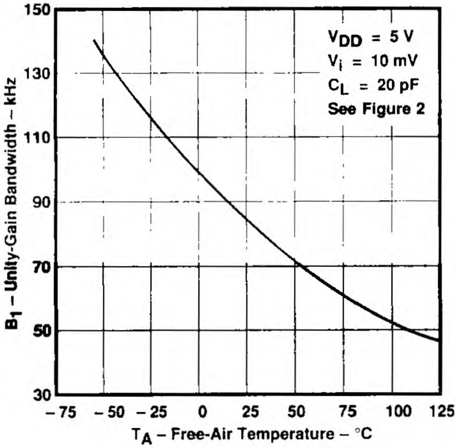

FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

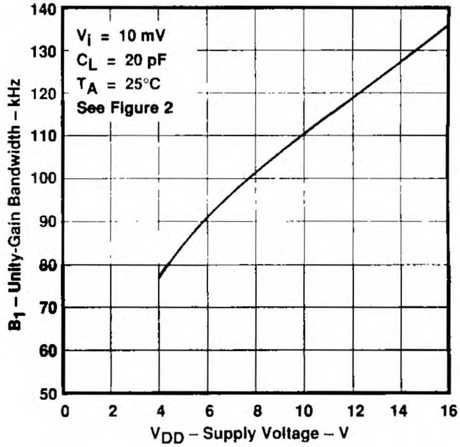

FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

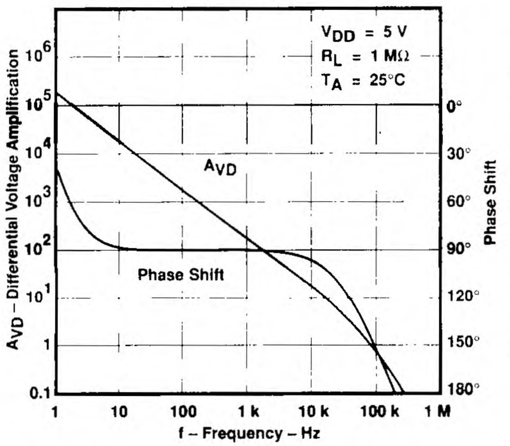

FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

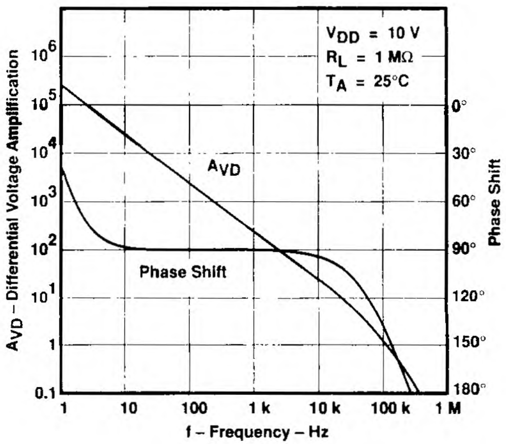

FIGURE 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

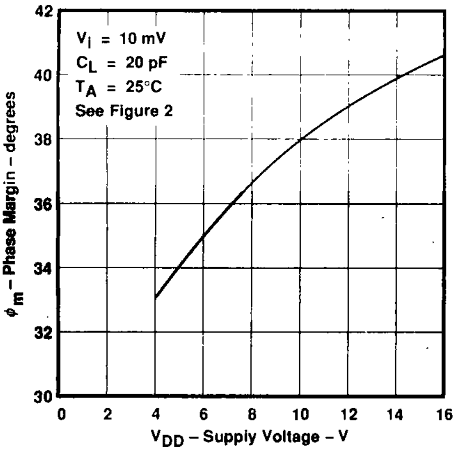

FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

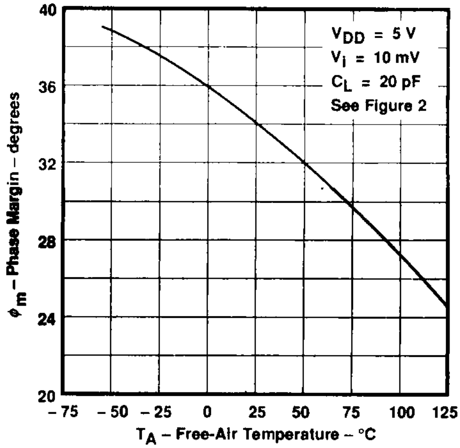

FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

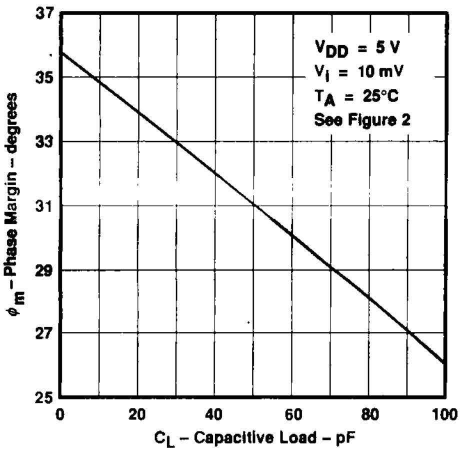

FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

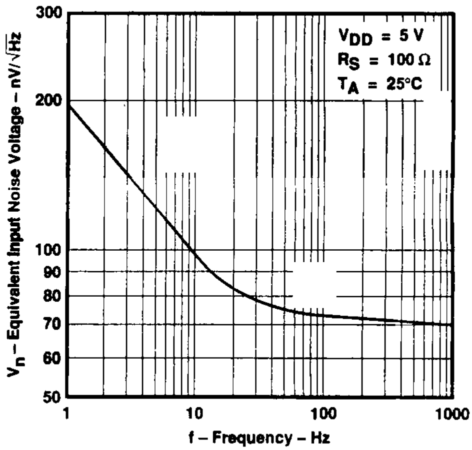

FIGURE 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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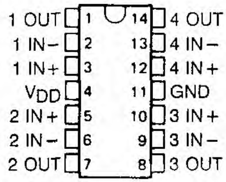
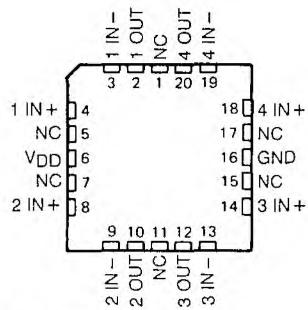
D3147, AUGUST 1988—REVISED OCTOBER 1988

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 850 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **14-Pin Small-Outline Package Option Also Available in Tape and Reel**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

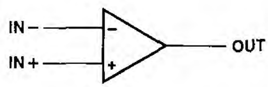
The TLC1079 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1079 is an ideal solution for low-voltage, battery-operated systems. The 20-mA output drive capability means that the TLC1079 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

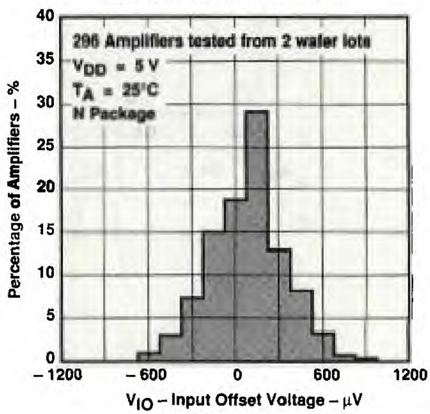
Since this device is functionally compatible as well as pin compatible with the TLC27L4 and TLC27L9, the TLC1079 easily upgrades existing designs that can benefit from its improved performance.

The TLC1079 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

symbol (each amplifier)



DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1079 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

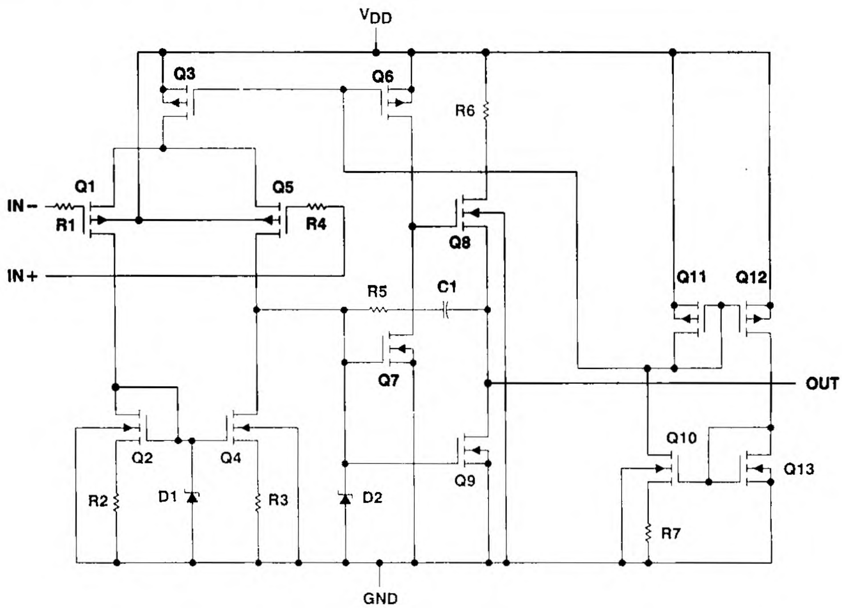
The M- suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I- suffix devices are characterized for operation from −40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D) SEE NOTE 1	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC1079CD	–	TLC1079CJ	TLC1079CN
−40°C to 85°C	TLC1079ID	–	TLC1079IJ	TLC1079IN
−55°C to 125°C	–	TLC1079MFK	TLC1079MJ	–

NOTE 1: The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1079CDR).

equivalent schematic (each amplifier)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . 18 V
Different input voltage (see Note 3) . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . −0.3 V to V_{DD}
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O (each output) . . . . ±30 mA
Total current into V_{DD} terminal (see Note 4) . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . −55°C to 125°C
I-suffix . . . . −40°C to 85°C
C-suffix . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		4	−0.2		4	−0.2		4	V
	$V_{DD} = 10$ V	0		9	−0.2		9	−0.2		9	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			[illegible]			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	525		500	850		V/mV
			0°C	250	700		500	1010		
			70°C	[illegible]	380		350	660		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		40	68		57	92	μA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

TEXAS INSTRUMENTS
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electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			85°C		200	2000		[illegible]	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	[illegible] to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	μA
			−40°C		62	108		98	172	
			85°C		29	52		40	72	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150	[illegible]		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	95		75	[illegible]		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		40	68		57	92	μA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

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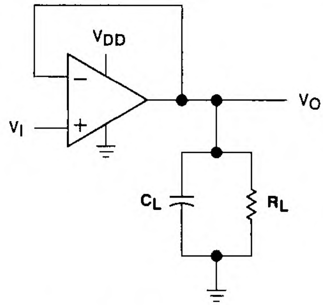
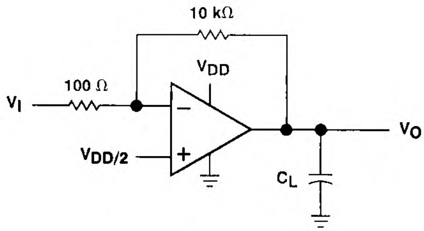
PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

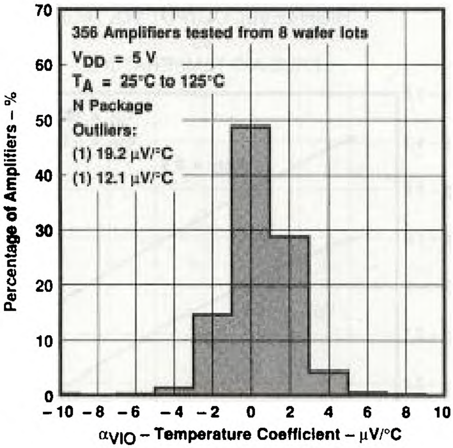


FIGURE 3

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

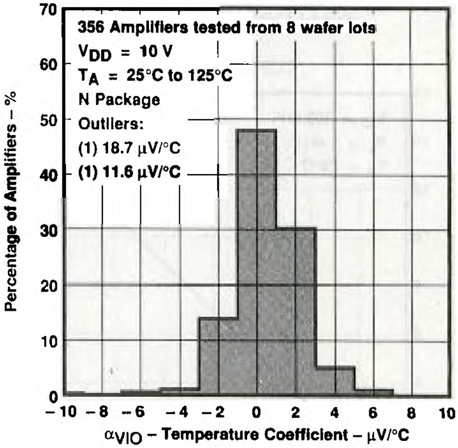


FIGURE 4

2

Operational Amplifiers

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

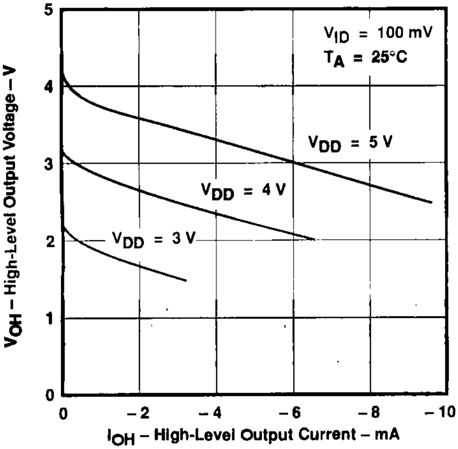


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

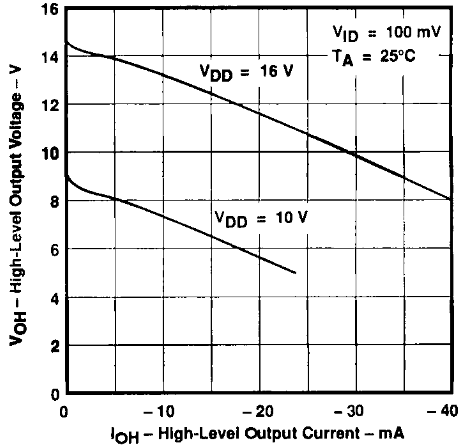


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

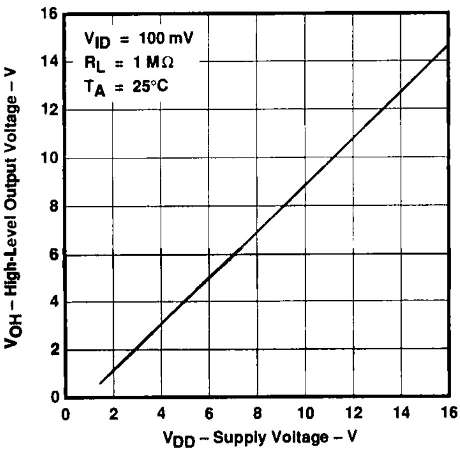


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

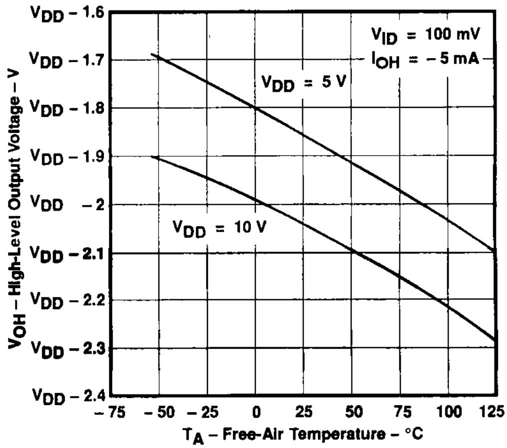


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

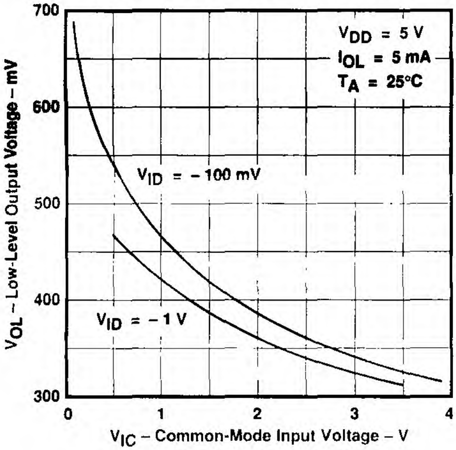


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

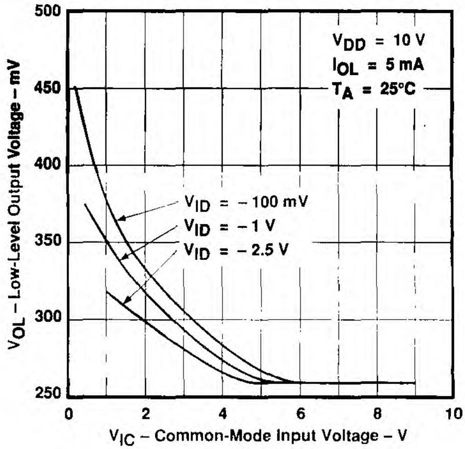


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

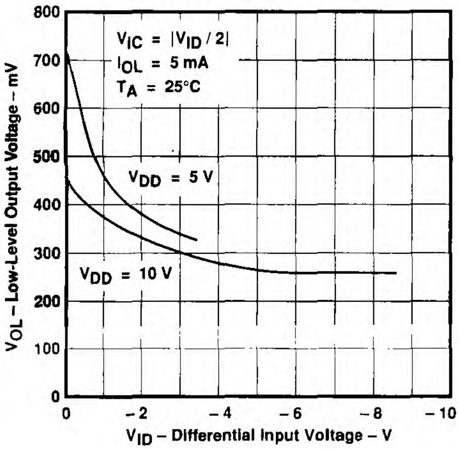


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

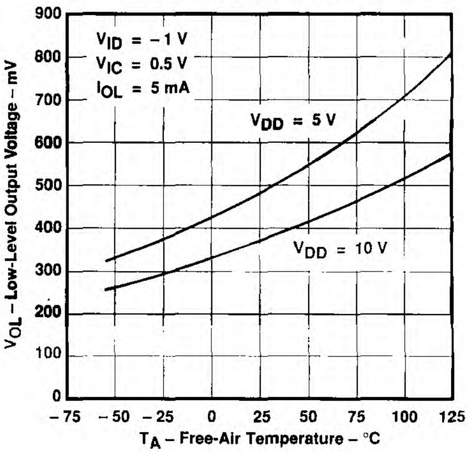


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

2

Operational Amplifiers

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

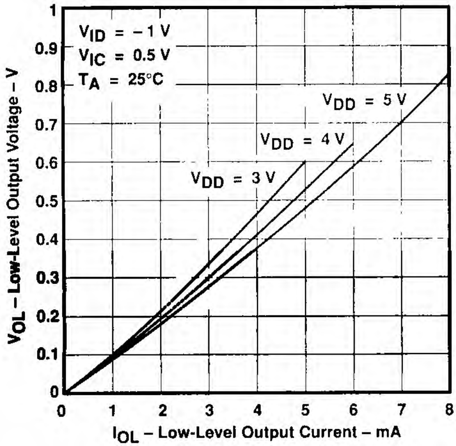


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

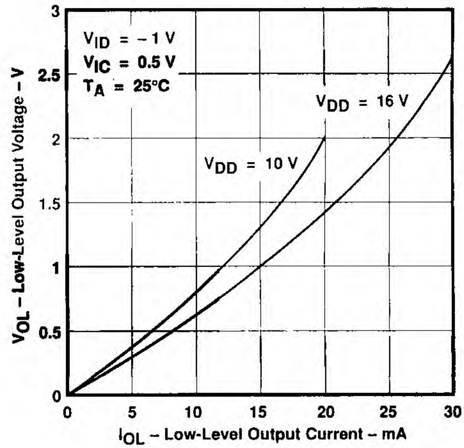


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

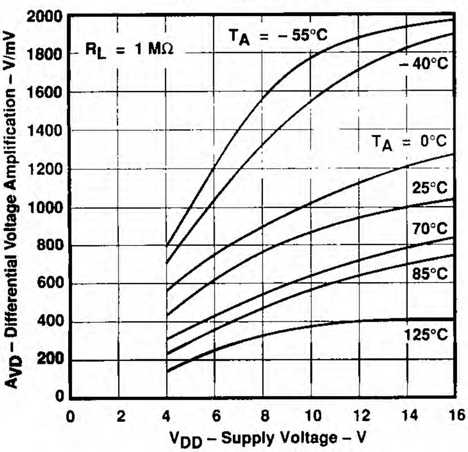


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

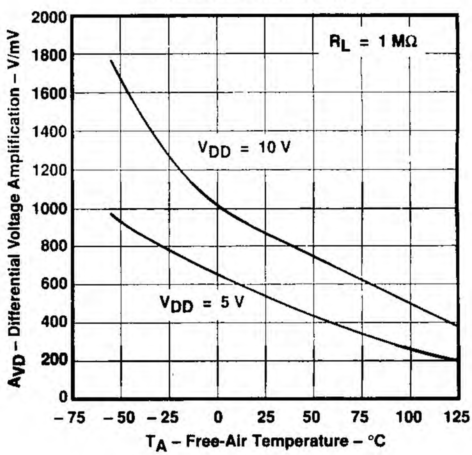


FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

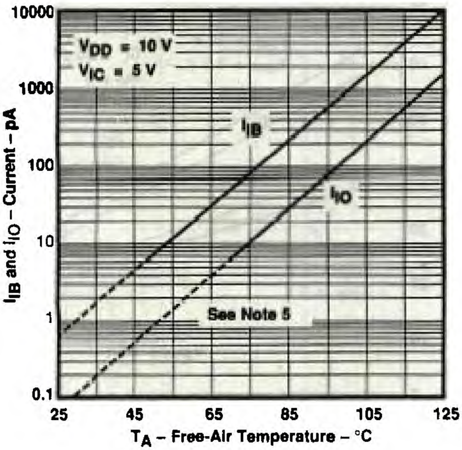


FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

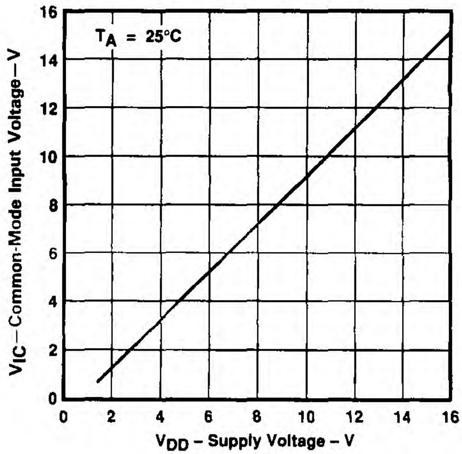


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

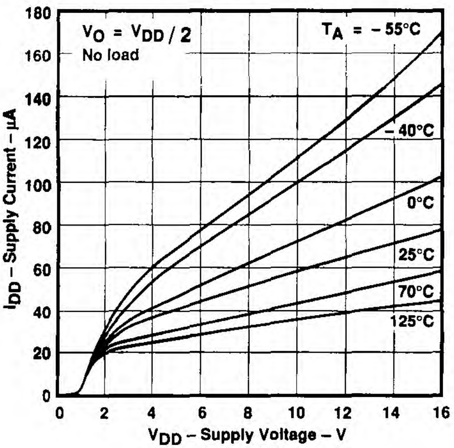


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

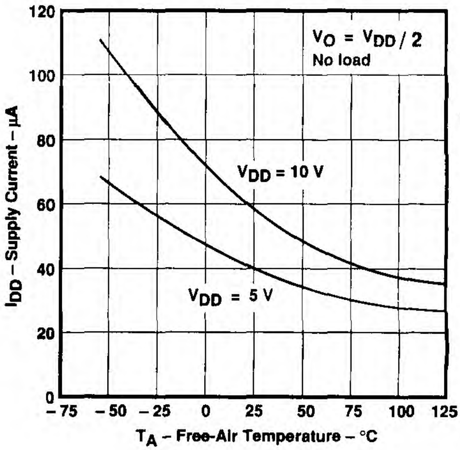


FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathmatically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

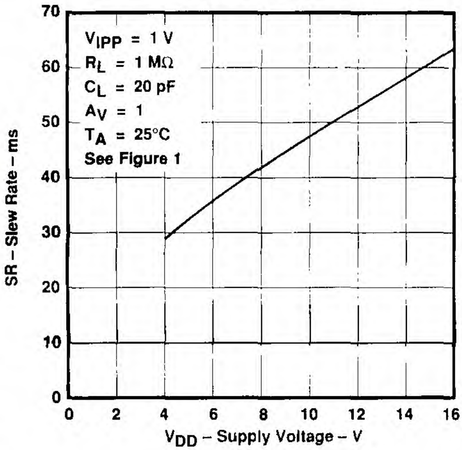


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

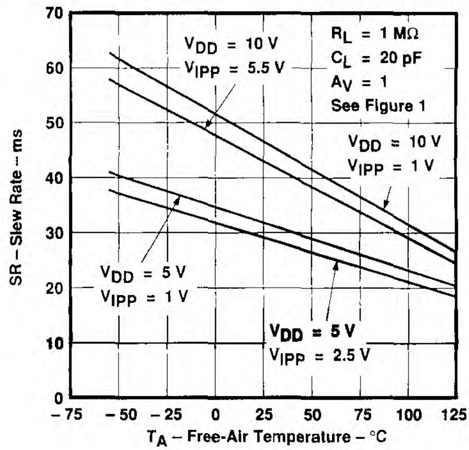


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

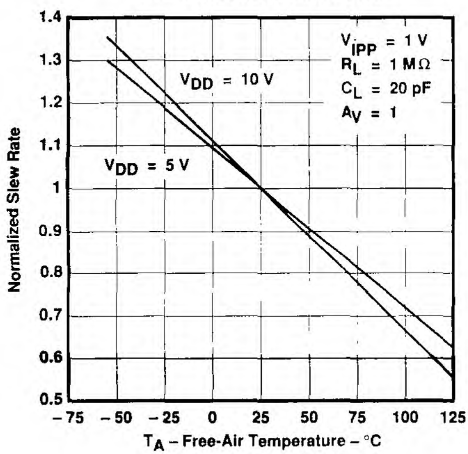


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

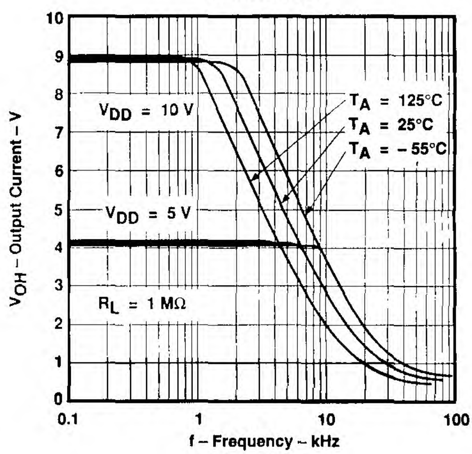


FIGURE 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

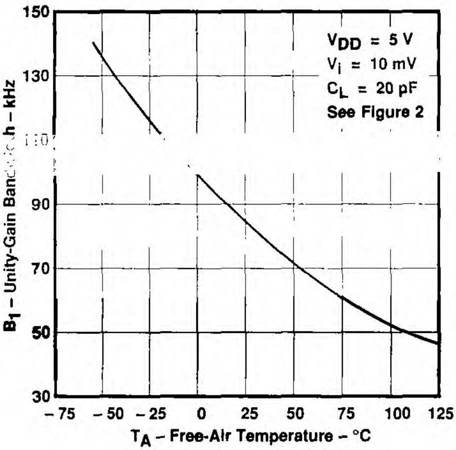


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

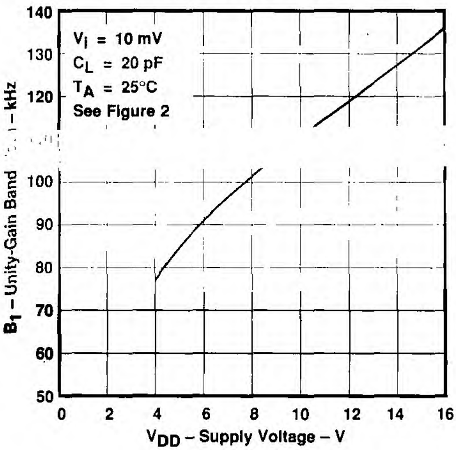


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

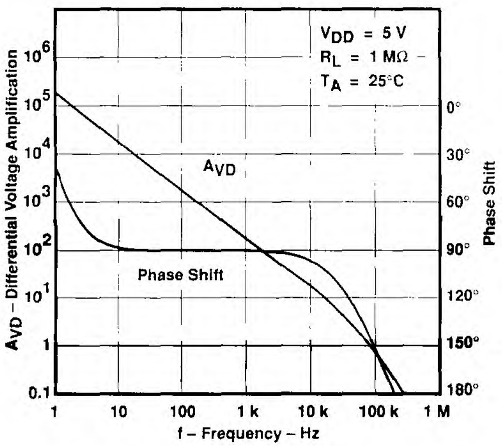


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

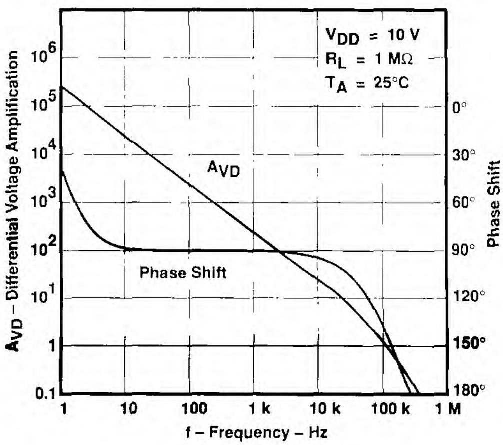


FIGURE 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

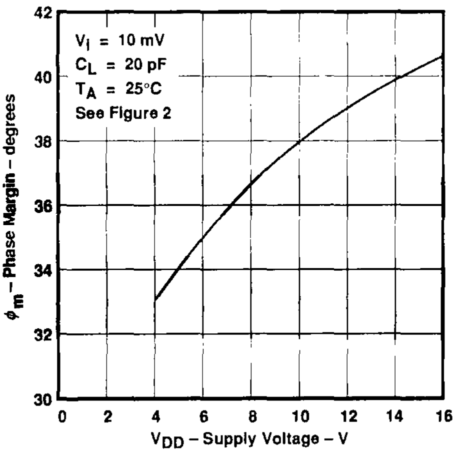


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

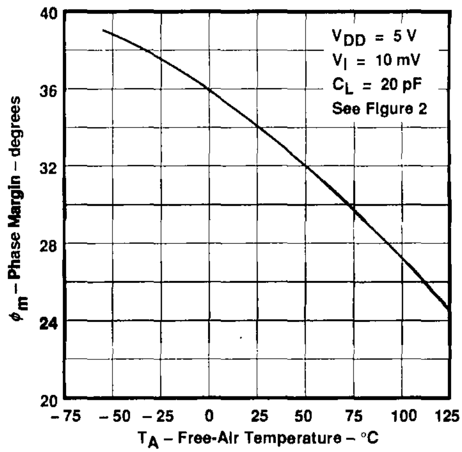


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

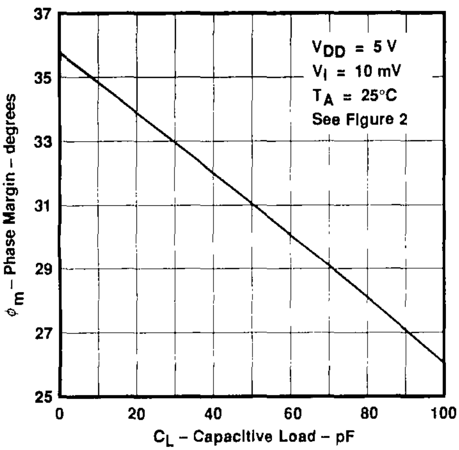


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

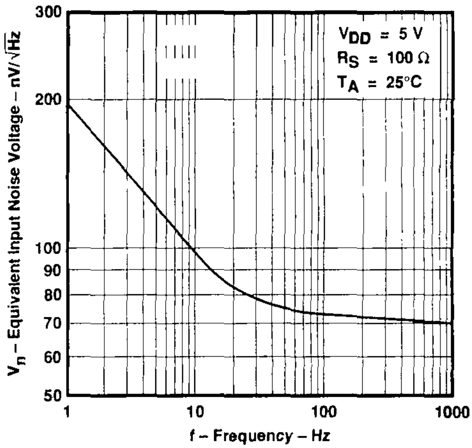


FIGURE 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

D3173, NOVEMBER 1988

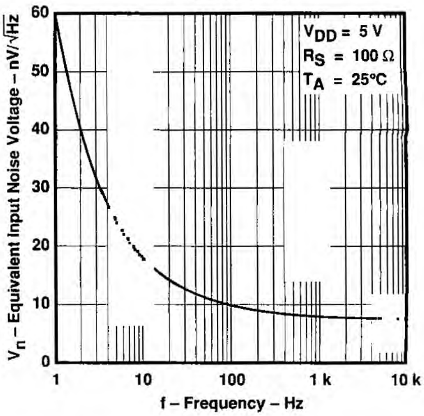
- **TLC2201B Is 100% Tested for Noise:**
  25 nV/√Hz Max at f = 10 Hz
  12 nV/√Hz Max at f = 1 kHz
- **Low Input Offset Voltage . . . 200 μV Max**
- **Excellent Offset Voltage Stability with Temperature . . . 0.5 μV/°C Typ**
- **Low Input Bias Current . . . 1 pA Typ at T_A = 25°C**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

The TLC2201, TLC2201A, and TLC2201B are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal conditioning applications in either single-supply or split-supply configurations.

TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
vs
FREQUENCY



2

Operational Amplifiers

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup. In addition, internal ESD protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	V_n max f = 10 Hz AT 25°C	V_n max f = 1 kHz AT 25°C	PACKAGE SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)	METAL CAN (L)
0°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BCD	TLC2201BCP	TLC2201BCJG	—	TLC2201BCL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201ACD	TLC2201ACP	TLC2201ACJG	—	TLC2201ACL
70°C	500 μV	—	—	TLC2201CD	T [illegible] P	TLC2201CJG	—	TLC2201CL
– 40°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BID	T [illegible] IP	TLC2201BIJG	—	TLC2201BIL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AID	TLC2201AIP	TLC2201AIJG	—	TLC2201AIL
85°C	500 μV	—	—	TLC2201ID	TI [illegible] IP	TL [illegible]	—	TLC2201IL
– 55°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BMD	TI [illegible] BMP	TL [illegible] G	TLC2201BMFK	TLC2201BML
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AMD	TLC2201AMP	TLC2201AMJG	TLC2201AMFK	TLC2201AML
125°C	500 μV	—	—	TLC2201MD	TLC2201MP	TLC2201MJG	TLC2201MFK	TLC2201ML

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2201BCDR).

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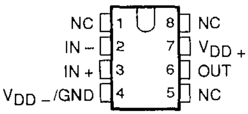
TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

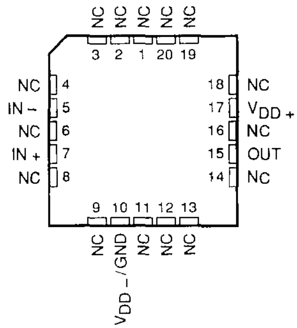
description (continued)

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

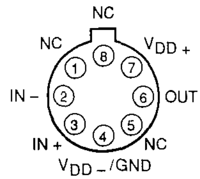
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



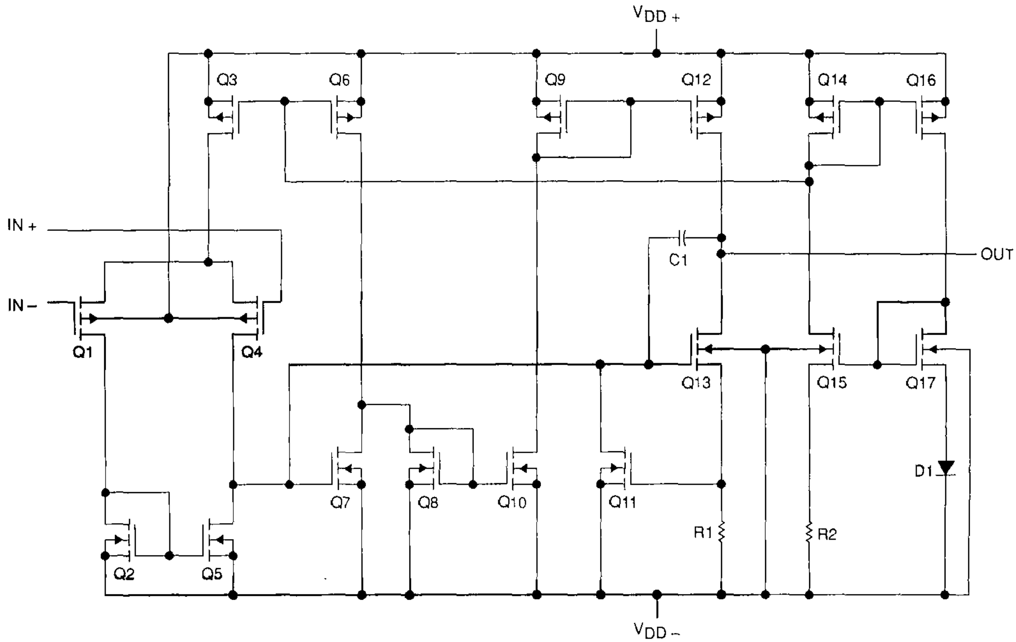
L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

equivalent schematic



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... −8 V
Differential input voltage (see Note 2) .... ±16 V
Input voltage range, V_I (any input, see Note 1) .... ±8 V
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Continuous total dissipation .... see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... −55°C to 125°C
I-suffix .... −40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX		I-SUFFIX		C-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	−55	125	−40	85	0	70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		V
			Full range	– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	200			
		V_O = ± 4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ± 2.3 V to ± 8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ± 2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	200			200			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	45			45			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM MIN	TLC2201AM TYP	TLC2201AM MAX	TLC2201BM MIN	TLC2201BM TYP	TLC2201BM MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM MIN	TLC2201AM TYP	TLC2201AM MAX	TLC2201BM MIN	TLC2201BM TYP	TLC2201BM MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		V
			Full range	– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	250			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	65			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/µs
			Full range	1.4			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI MIN	TLC2201AI TYP	TLC2201AI MAX	TLC2201BI MIN	TLC2201BI TYP	TLC2201BI MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	250			250			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	65			65			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI MIN	TLC2201AI TYP	TLC2201AI MAX	TLC2201BI MIN	TLC2201BI TYP	TLC2201BI MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.4			1.4			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201I MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201I MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$,	25°C	400	560		V/mV
			Full range	300			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		
			Full range	70			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.5			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201AC MIN	TLC2201AC TYP	TLC2201AC MAX	TLC2201BC MIN	TLC2201BC TYP	TLC2201BC MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	300			300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	70			70			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201AC MIN	TLC2201AC TYP	TLC2201AC MAX	TLC2201BC MIN	TLC2201BC TYP	TLC2201BC MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	[illegible]		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION

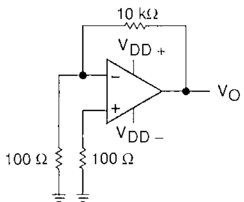
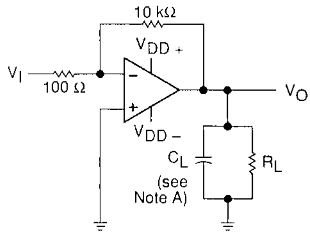
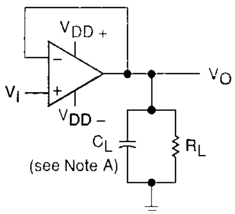


FIGURE 1. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 2. PHASE MARGIN TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 3. SLEW RATE TEST CIRCUIT

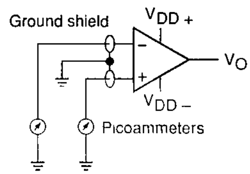


FIGURE 4. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLC2201, TLC2201A, and TLC2201B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual applications requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2201B device, while lot sample testing is performed on the TLC2201A. For other noise test requirements, please contact the factory.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage	6
		vs Temperature	7
[illegible]	Common-mode rejection ratio	vs Frequency	8
V_{OM}	Maximum peak output voltage	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency	12
		vs Current	13
		vs Temperature	14
V_{OL}	Low-level output voltage	vs Output current	15
		vs Temperature	16
A_{VD}	Differential voltage amplification	vs Frequency	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
I_{DD}	Supply current	vs Supply voltage	21
		vs Temperature	22
SR	Slew rate	vs Supply voltage	23
		vs Temperature	24
	Pulse response	Small-signal	25, 26
		Large-signal	27, 28
V_{NPP}	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz	29
		0.1 to 10 Hz	30
	Gain-bandwidth product	vs Supply voltage	31
		vs Temperature	32
ϕ_m	Phase margin	vs Supply voltage	33
		vs Temperature	34
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2201
INPUT OFFSET VOLTAGE

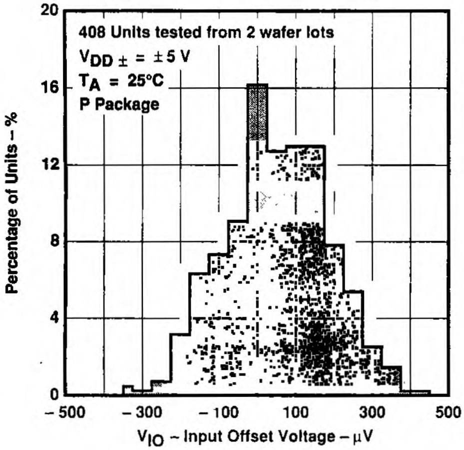


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

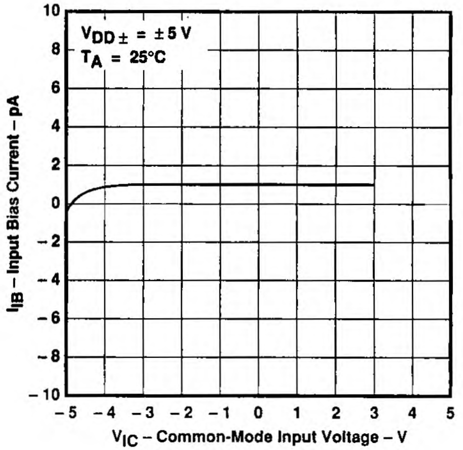


FIGURE 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

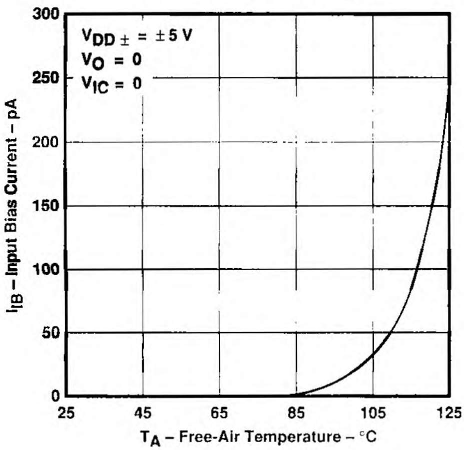


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

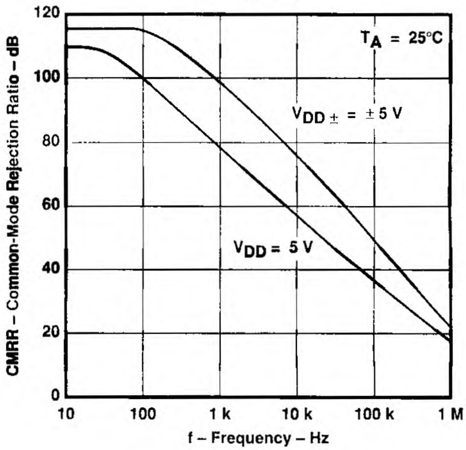


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

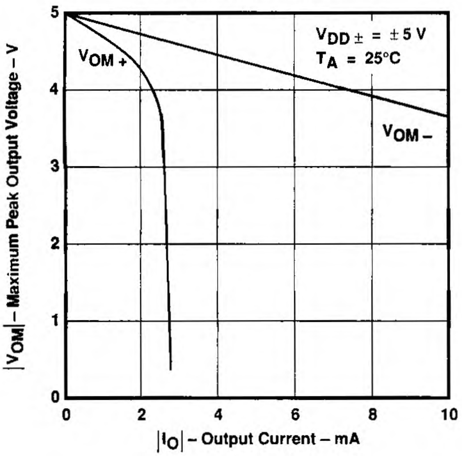


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

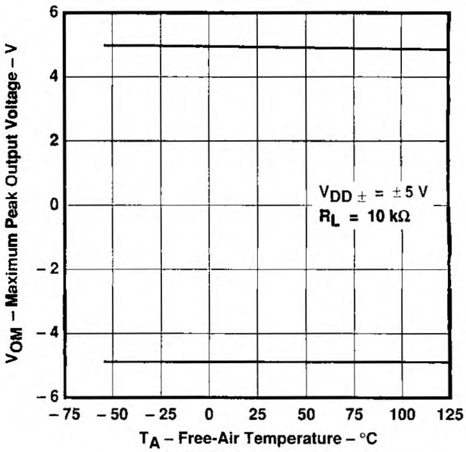


FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

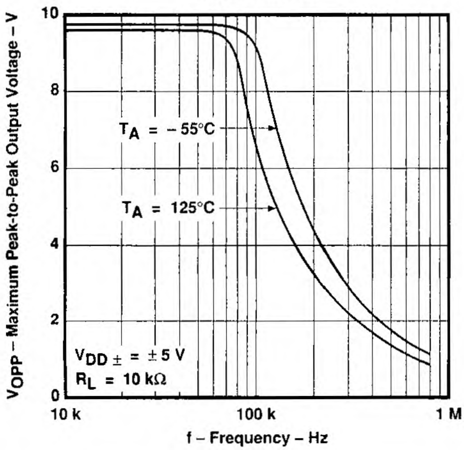


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

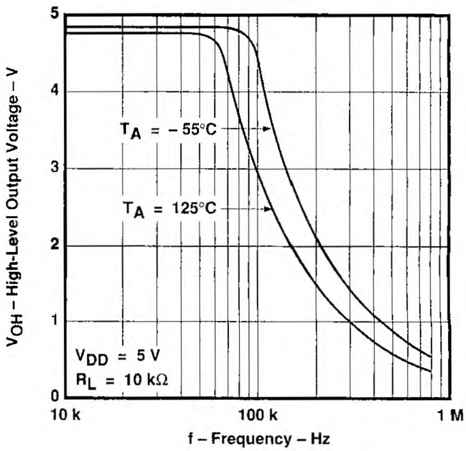


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

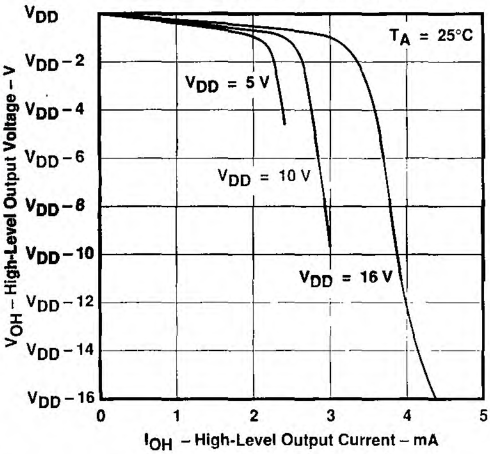


FIGURE 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

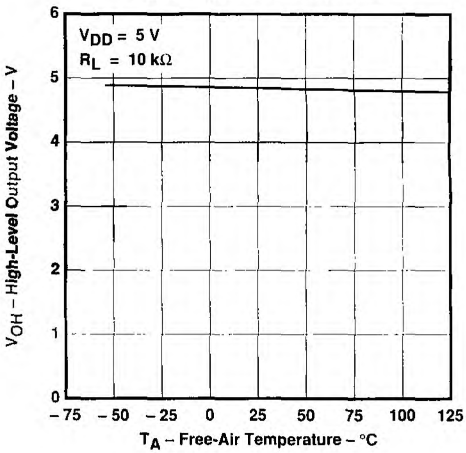


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

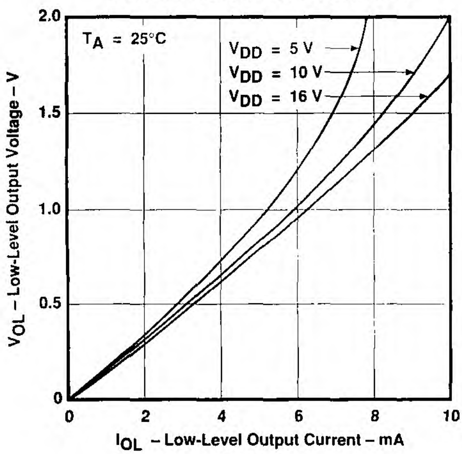


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

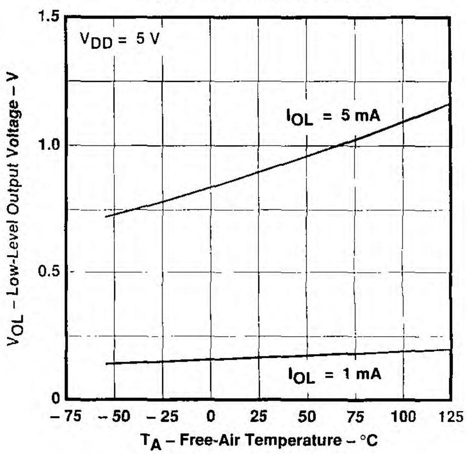


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

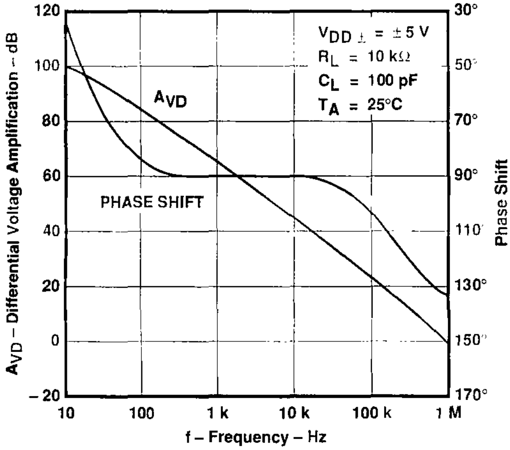


FIGURE 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

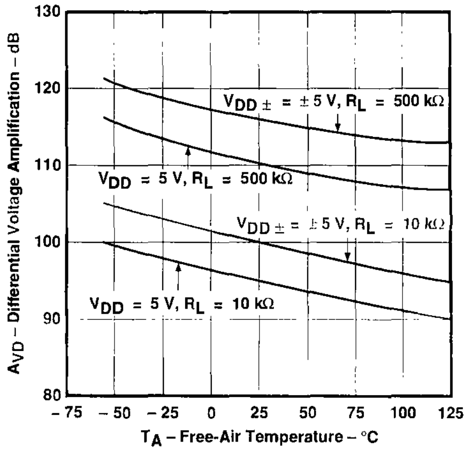


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

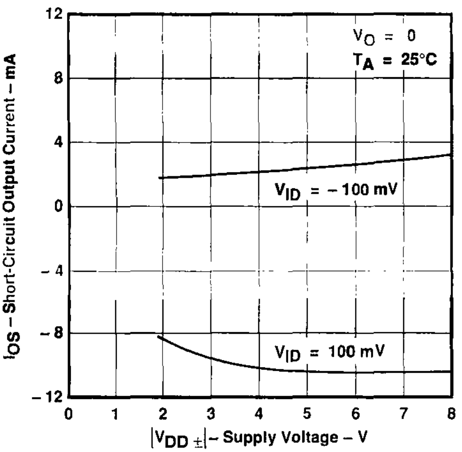


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

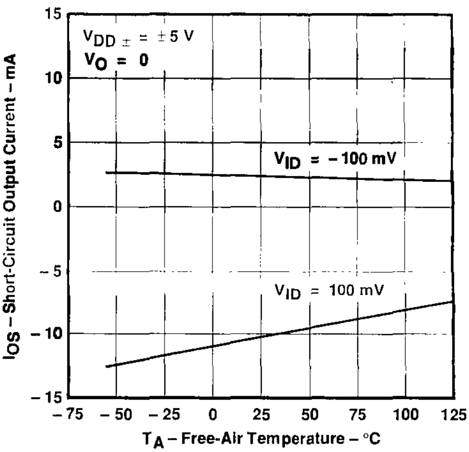


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Operational Amplifiers 2

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

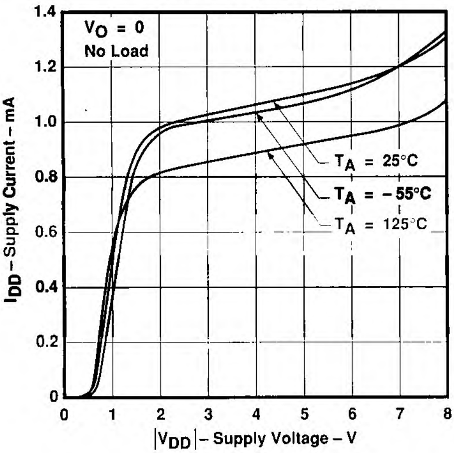


FIGURE 21

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

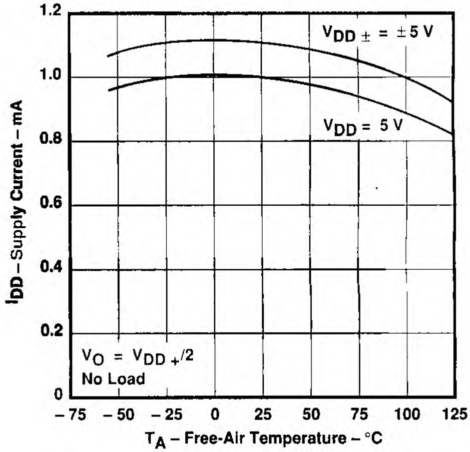


FIGURE 22

SLEW RATE
vs
SUPPLY VOLTAGE

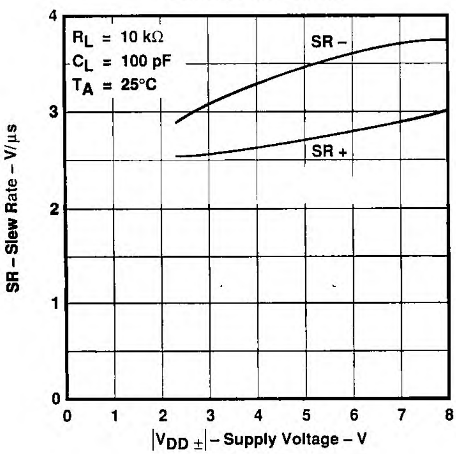


FIGURE 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

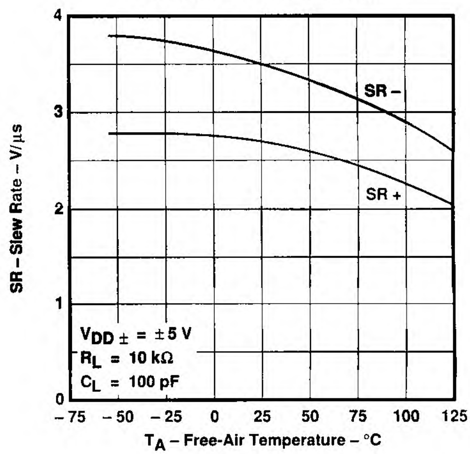


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

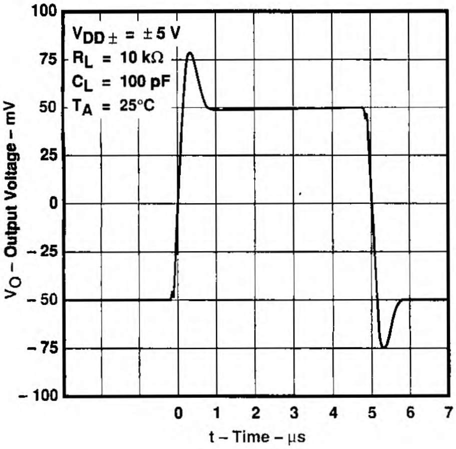


FIGURE 25

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

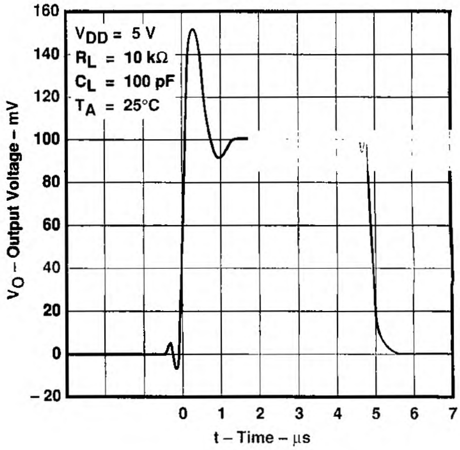


FIGURE 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

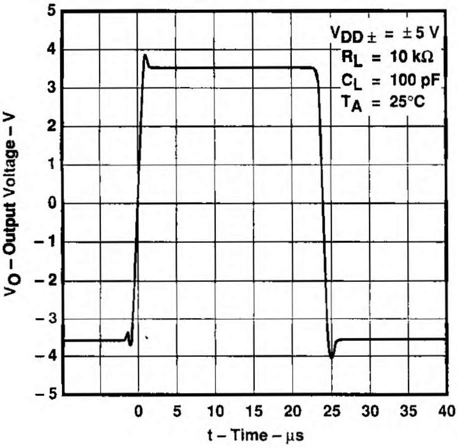


FIGURE 27

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

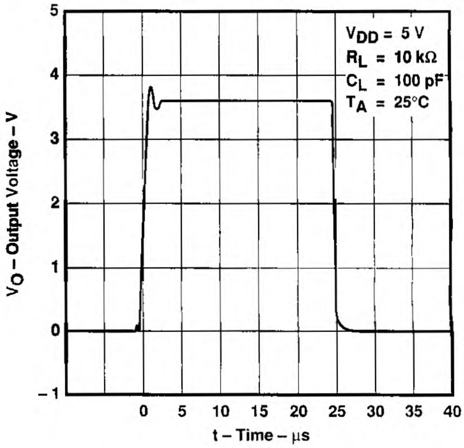


FIGURE 28

TYPICAL CHARACTERISTICS†

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

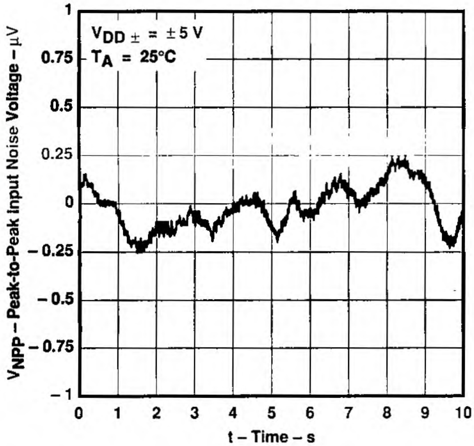


FIGURE 29

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

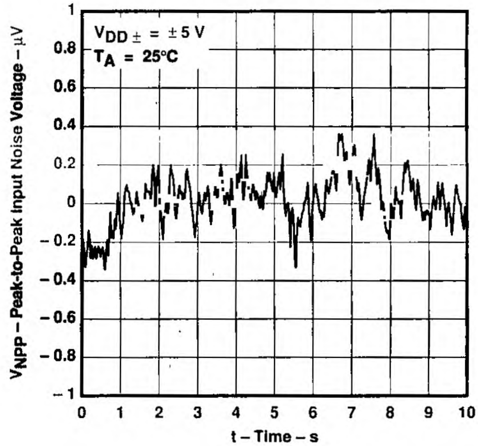


FIGURE 30

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

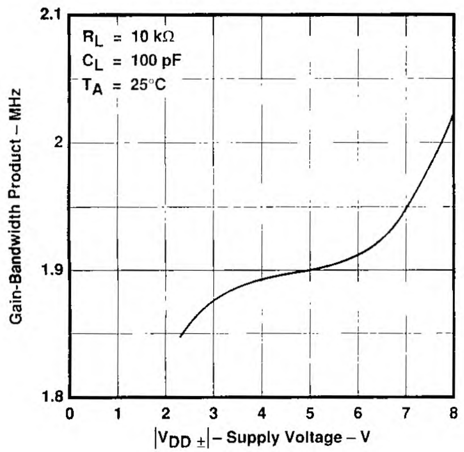


FIGURE 31

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

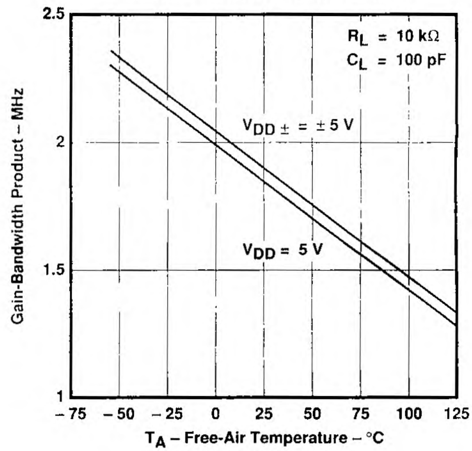


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

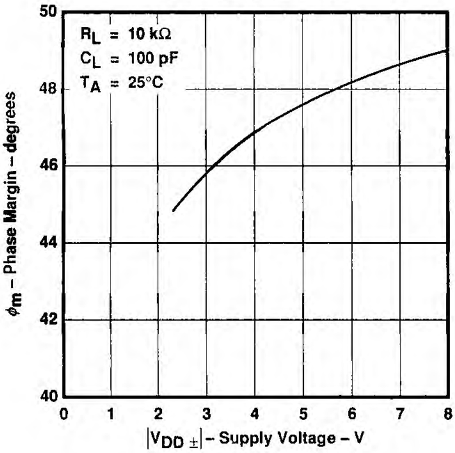


FIGURE 33

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

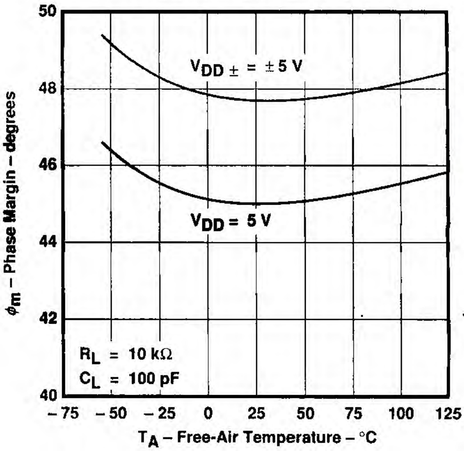


FIGURE 34

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

latchup avoidance

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2201, TLC2201A, and TLC2201B inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup; however, techniques reducing the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

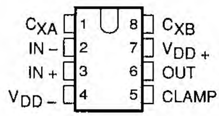
electrostatic discharge protection

These devices use internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

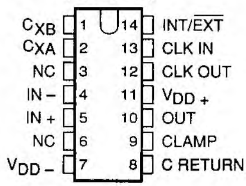
TLC2652, TLC2652A Advanced LinCMOS™ PRECISION CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

- Extremely Low Offset Voltage . . . 1 µV Max
- Extremely Low Change in Offset Voltage with Temperature . . . 0.003 µV/°C Typ
- Low Input Offset Current . . . 500 pA Max at T_A = −55°C to 125°C
- AVD . . . 135 dB Min
- CMRR and kSVR . . . 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

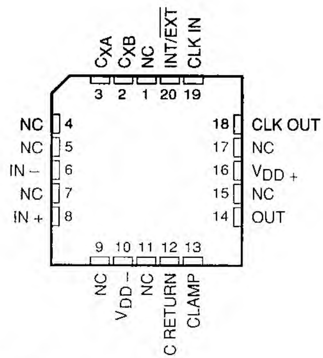
D008, JG, or P PACKAGE (TOP VIEW)



D014, J, or N PACKAGE (TOP VIEW)



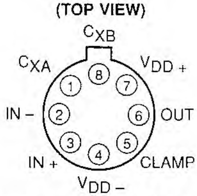
FK PACKAGE (TOP VIEW)



description

The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments **Advanced LinCMOS**™ process. This process in conjunction with unique chopper-stabilization circuitry produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

L PACKAGE (TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE 8-PIN SMALL-OUTLINE (D008)	8-PIN PLASTIC DIP (P)	8-PIN CERAMIC DIP (JG)	8-PIN METAL CAN (L)	14-PIN SMALL-OUTLINE (D014)	14-PIN PLASTIC DIP (N)	14-PIN CERAMIC DIP (J)	20-PIN CHIP CARRIER (FK)
0°C to 70°C	1 µV	TLC2652AC-8D	TLC2652ACP	TLC2652ACJG	TLC2652ACL	TLC2652AC-14D	TLC2652ACN	TLC2652ACJ	—
	3 µV	T[illegible]3D	T[illegible]	T[illegible]	T[illegible]	[illegible]4D	TLC2652CN	TLC2652CJ	—
−40°C to 85°C	1 µV	T[illegible]8D	T[illegible]	T[illegible]G	T[illegible]	[illegible]14D	TLC2652AIN	TLC2652AIJ	—
	3 µV	T[illegible]D	T[illegible]	T[illegible]IG	TLC2652IL	TLC2652I-14D	TLC2652IN	TLC2652IJ	—
−[illegible] to 125°C	1 µV	T[illegible]M-8D	T[illegible]MP	T[illegible]MJG	TLC2652AML	TLC2652AM-14D	TLC2652AMN	TLC2652AMJ	TLC2652AMFK
	3 µV	TLC2652M-8D	TLC2652MP	TLC2652MJG	TLC2652ML	TLC2652M-14D	TLC2652MN	TLC2652MJ	TLC2652MFK

D008 and D014 packages are available taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC2652AC-8DR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

Chopper stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2652 and TLC2652A an ideal choice for low-level signal processing applications such as strain gauges, thermocouples, and other transducer amplifiers. (For applications that require extremely low noise and higher usable bandwidth, use the TLC2654 or TLC2654A device, which has a chopping frequency of 10 kHz.)

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±1.9 V.

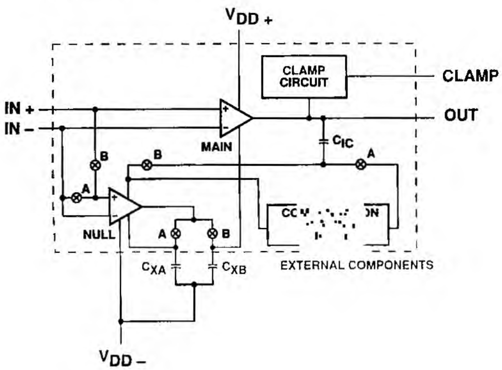
Two external capacitors are required for operation of the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is made accessible to allow the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold level of the TLC2652 and TLC2652A require no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overload recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

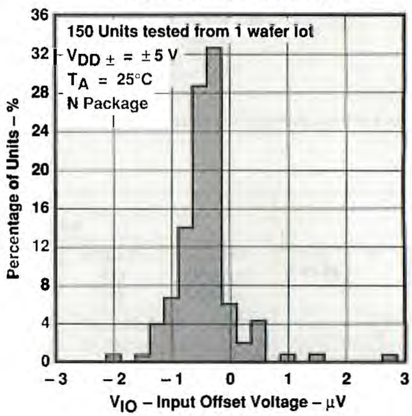
The device inputs and output are designed to withstand −100-mA surge currents without sustaining latchup. Additionally, the TLC2652 and TLC2652A incorporate internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

functional block diagram



DISTRIBUTION OF TLC2652
INPUT OFFSET VOLTAGE



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... −8 V
Differential input voltage (see Note 2) .... ±16 V
Input voltage range, V_I (any input, see Note 1) .... ±8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins .... V_{DD-} to V_{DD-} +5.2 V
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins .... ±5 mA
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... −55°C to 125°C
I-suffix .... −40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	± 1.9		± 8	± 1.9		± 8	± 1.9		± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V
Clock Input voltage	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V
Operating free-air temperature, T_A	− 55		125	− 40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AM MIN	TLC2652AM TYP	TLC2652AM MAX	TLC2652M MIN	TLC2652M TYP	TLC2652M MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5	[illegible]		0.6	[illegible]	μV
			Full range			4			6	
α_{VIO}	Temperature coefficient of input offset voltage		−55°C to 125°C		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	150		120	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AM			TLC2652M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	[illegible]	2.8		2	2.8		V/μs
			Full range	1.3			1.3			
SR −	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.6			1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94			94		nV/√Hz
		f = 1 kHz	25°C		23			23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is − 55°C to 125°C.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AI			TLC2652I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5	1		0.6	3	µV
			Full range			2.95			4.95	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 3.1			– 5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	·	135	150		120	150		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AI MIN	TLC2652AI TYP	TLC2652AI MAX	TLC2652I MIN	TLC2652I TYP	TLC2652I MAX	UNIT
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.4			1.4			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is − 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AC			TLC2652C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		0.5	1		0.6	3	µV
			Full range			2.35			4.35	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	150		120	150		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2652AC MIN	TLC2652AC TYP	TLC2652AC MAX	TLC2652C MIN	TLC2652C TYP	TLC2652C MAX	UNIT
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	[illegible]	2.8		2	2.8		V/μs
			Full range	1.5			1.5			
SR –	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Normalized input offset voltage	vs Chopping frequency	1
I_{IB}	Input bias current	vs Common-mode input voltage	2
		vs Chopping frequency	3
		vs Temperature	4
I_{IO}	Input offset current	vs Chopping frequency	5
		vs Temperature	6
	Clamp current	vs Output voltage	7
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9, 10
		vs Temperature	11, 12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
	Gain-bandwidth product	vs Supply voltage	28
		vs Temperature	29
ϕ_m	Phase margin	vs Supply voltage	30
		vs Temperature	31
		vs Load capacitance	32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

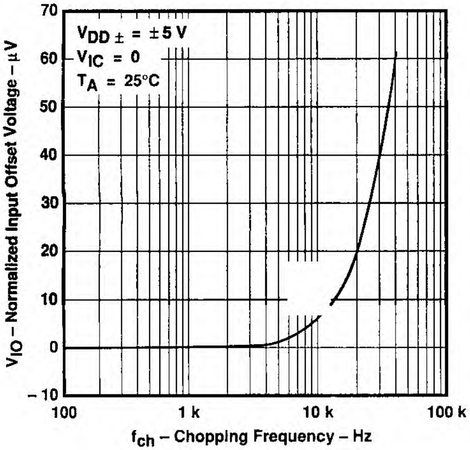


FIGURE 1

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

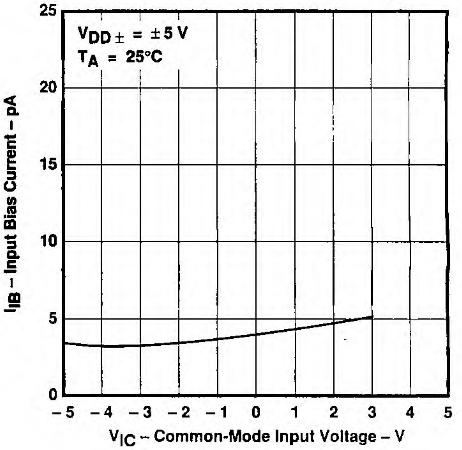


FIGURE 2

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

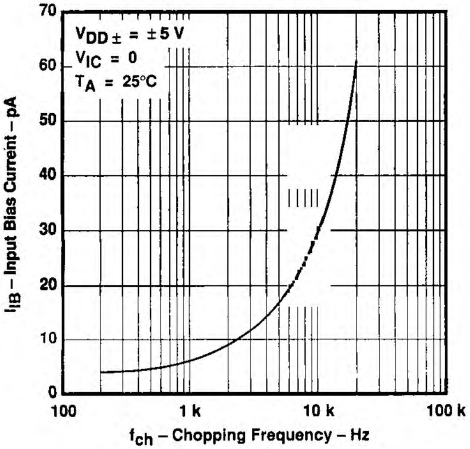


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

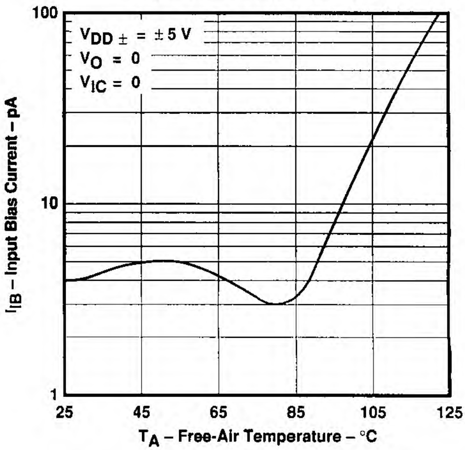


FIGURE 4

2

Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

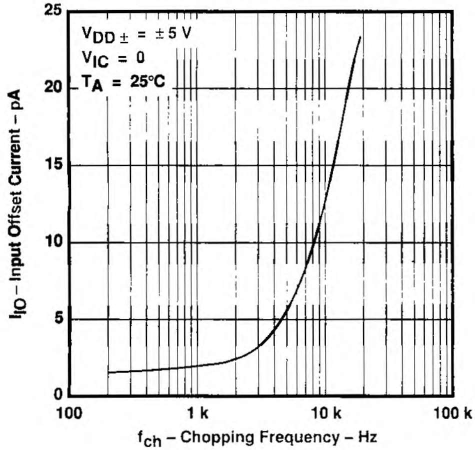


FIGURE 5

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

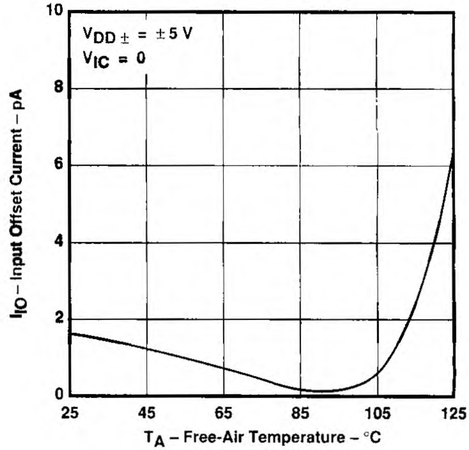


FIGURE 6

CLAMP CURRENT
vs
OUTPUT VOLTAGE

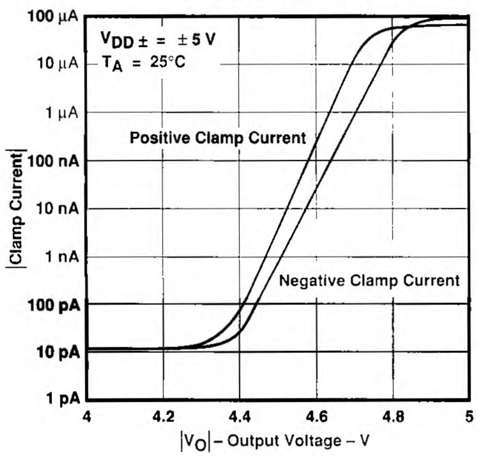


FIGURE 7

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

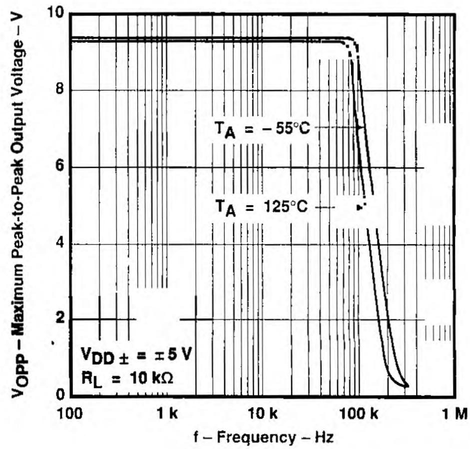


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

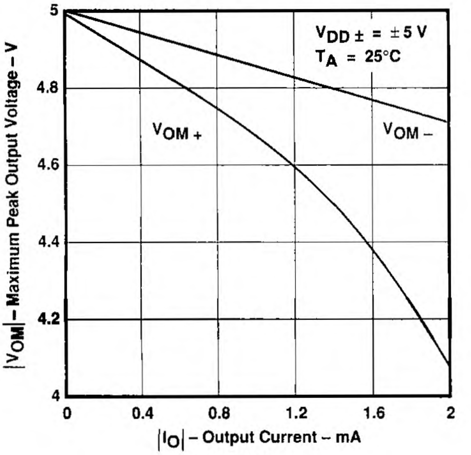

FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

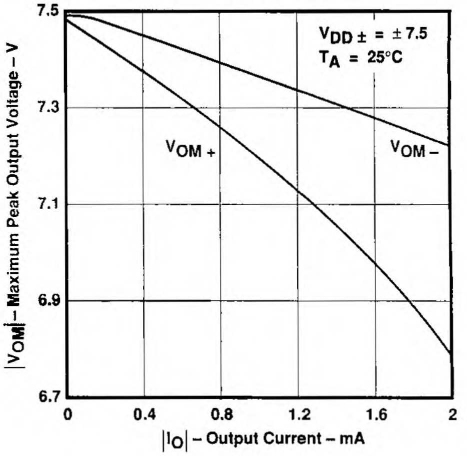

FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

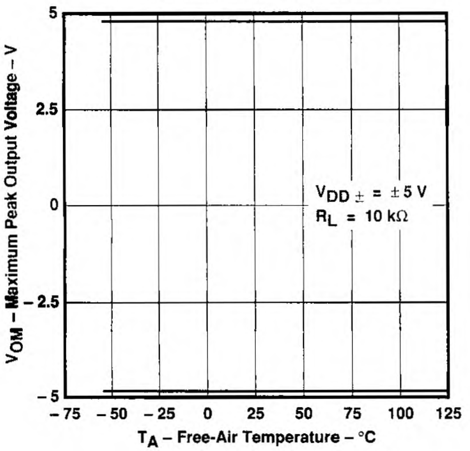

FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

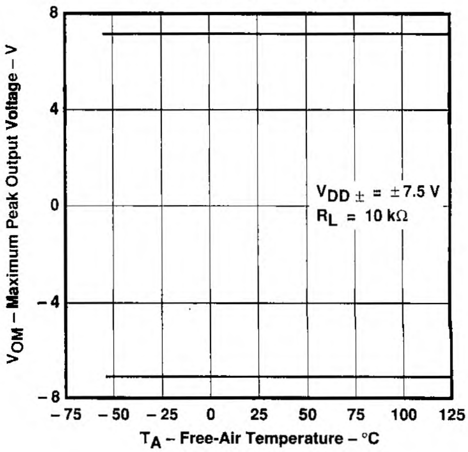

FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

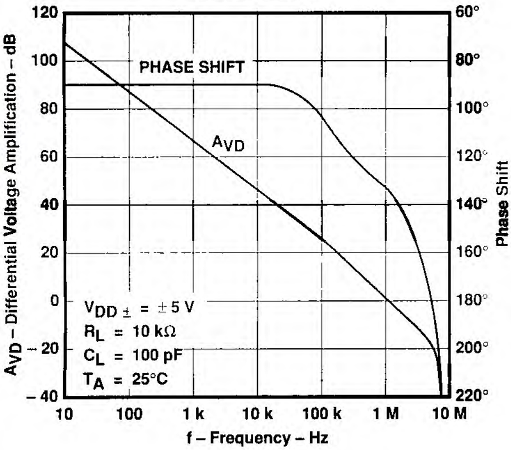

FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

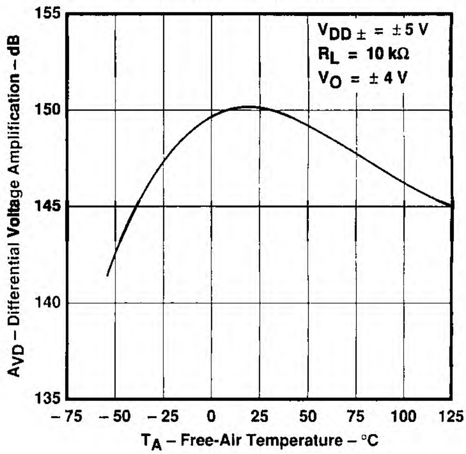

FIGURE 14

CHOPPING FREQUENCY vs SUPPLY VOLTAGE

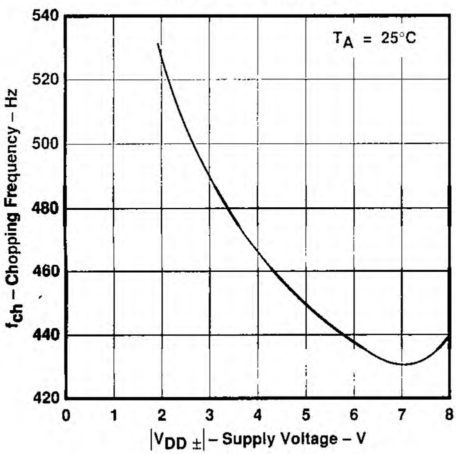

FIGURE 15

CHOPPING FREQUENCY vs FREE-AIR TEMPERATURE

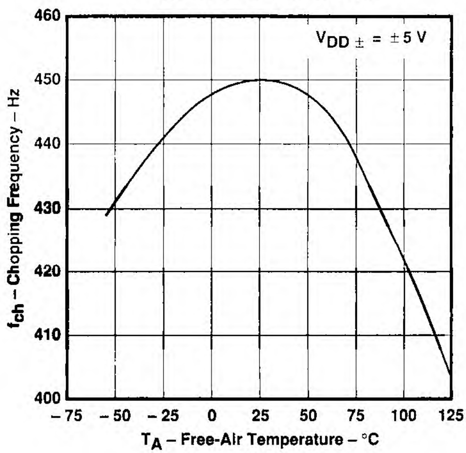

FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

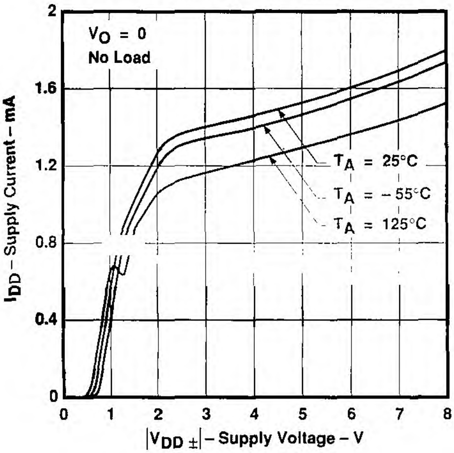


FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

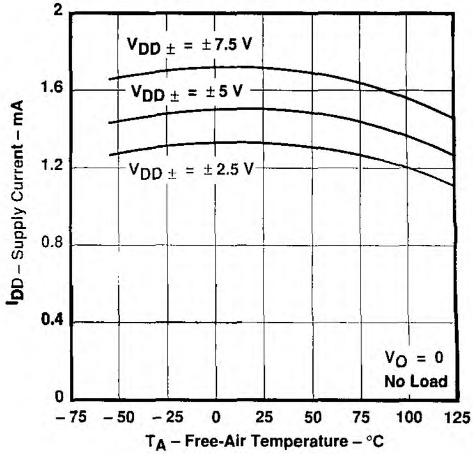


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

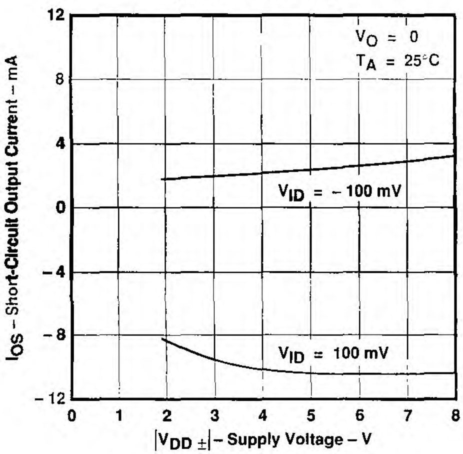


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

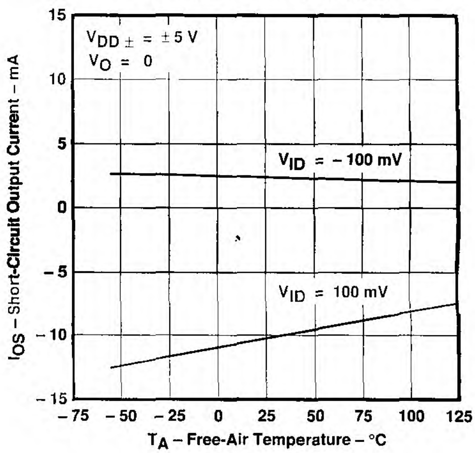


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

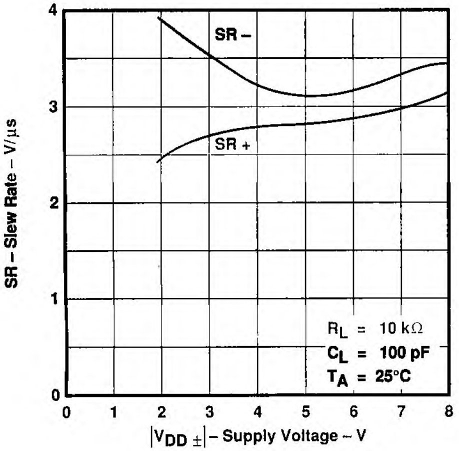


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

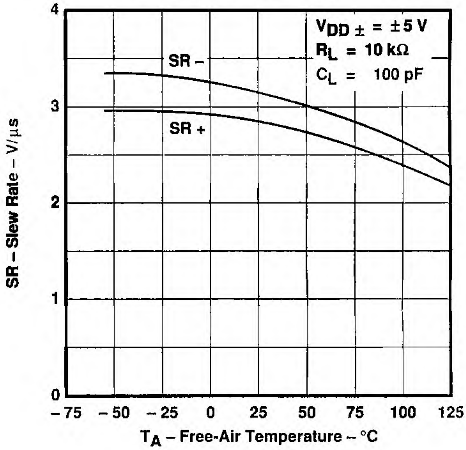


FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

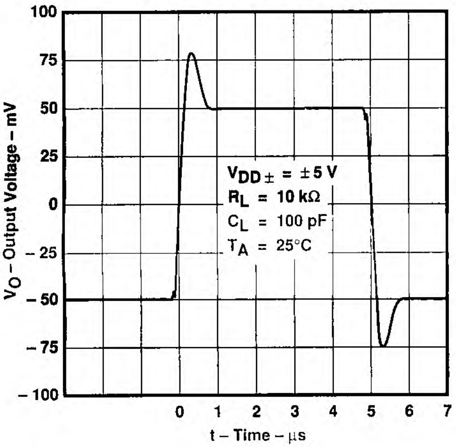


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

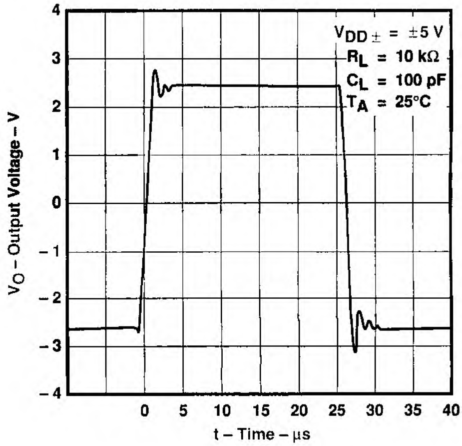


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

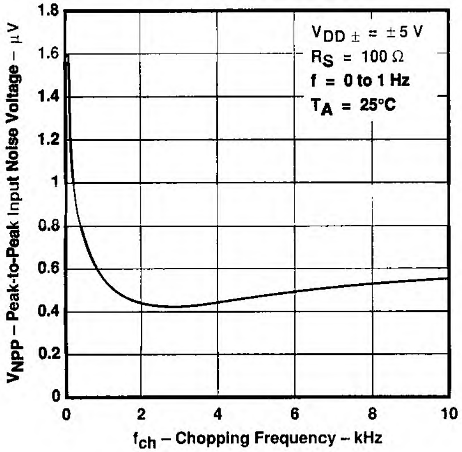


FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

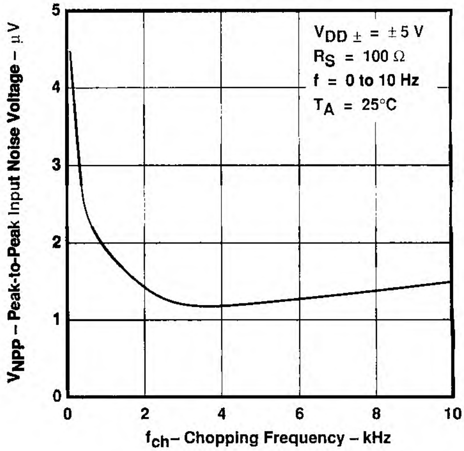


FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

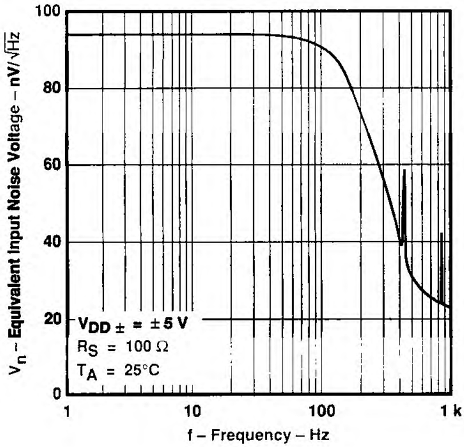


FIGURE 27

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

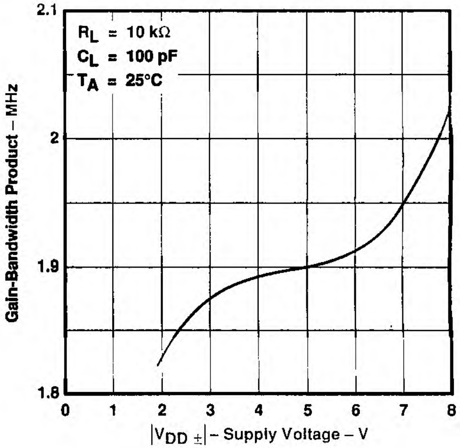


FIGURE 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

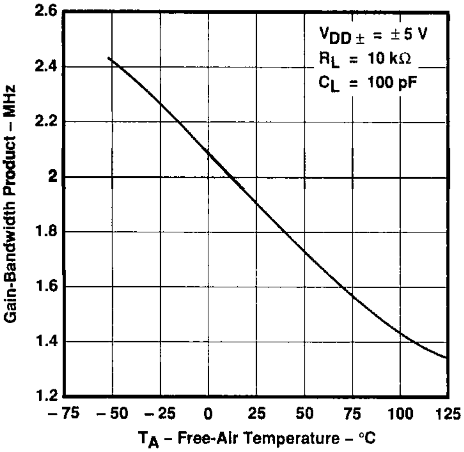


FIGURE 29

PHASE MARGIN
vs
SUPPLY VOLTAGE

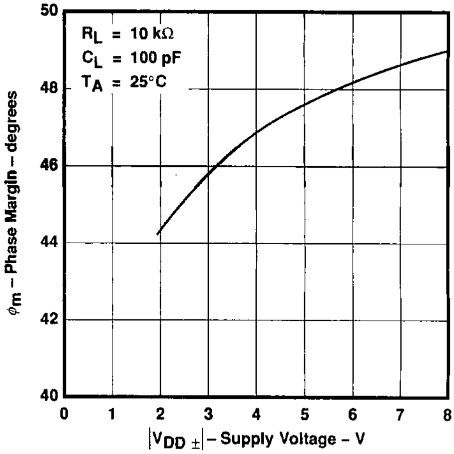


FIGURE 30

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

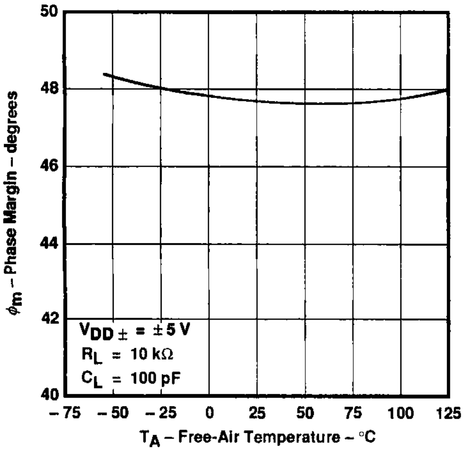


FIGURE 31

PHASE MARGIN
vs
LOAD CAPACITANCE

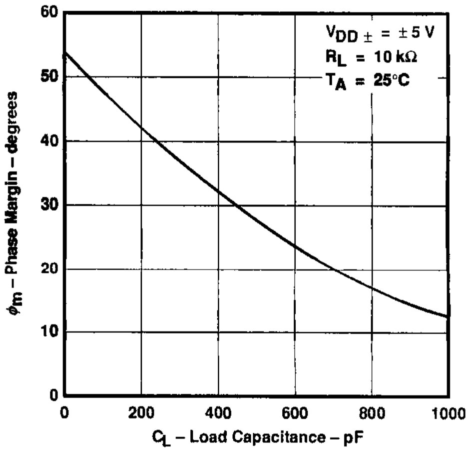


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation that can negate the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin will cause degradation in the noise performance. This problem is eliminated on the TLC2652.

internal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{EXT}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{EXT}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin. The duty cycle of the external clock is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be

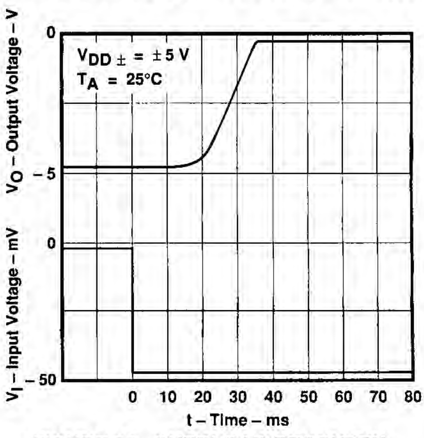


FIGURE 33. OVERLOAD RECOVERY

TYPICAL APPLICATION DATA

reduced further by using internal clamp circuitry accessible through the CLAMP pin.

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed- loop gain is reduced and the TLC2652 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.003 µV °C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptable to latchup due to their inherent parasitic thyristors, the TLC2652 inputs and output were designed to withstand –100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as is possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases; a nulling phase and an amplifying phase. The term *chopper-stabilized* derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the

TYPICAL APPLICATION DATA

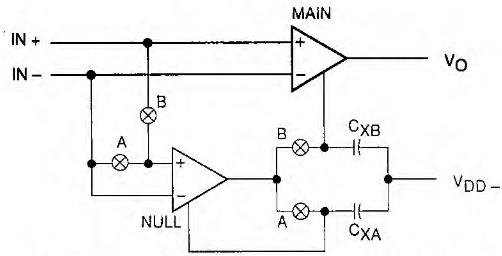


FIGURE 34. TLC2652 SIMPLIFIED BLOCK DIAGRAM

nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power-supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process with its low-noise analog MOS transistors and patent-pending input stage design significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches.

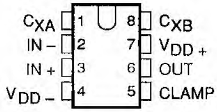
As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

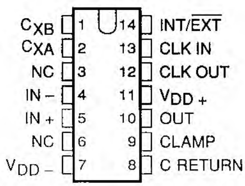
TLC2654, TLC2654A Advanced LinCMOS™ LOW-NOISE CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

- Input Noise Voltage . . .
  - 0.5 µV p-p Typ, f = 0 to 1 Hz
  - 1.5 µV p-p Typ, f = 0 to 10 Hz
  - 47 nV/√Hz Typ, f = 10 Hz
  - 13 nV/√Hz Typ, f = 1 kHz
- High Chopping Frequency . . . 10 kHz Typ
- No Clock Noise Below 10 kHz
- No Intermodulation Error Below 5 kHz
- Low Input Offset Voltage . . . 10 µV Max
- Excellent Offset Voltage Stability with Temperature . . . 0.3 µV/°C Max
- A_{VD} . . . 135 dB Min
- CMRR . . . 110 dB Min
- k_{SVR} . . . 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

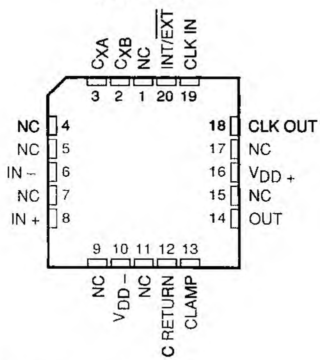
D008, JG, or P PACKAGE
(TOP VIEW)



D014, J, or N PACKAGE
(TOP VIEW)

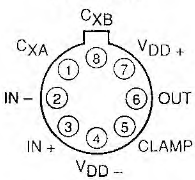


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case

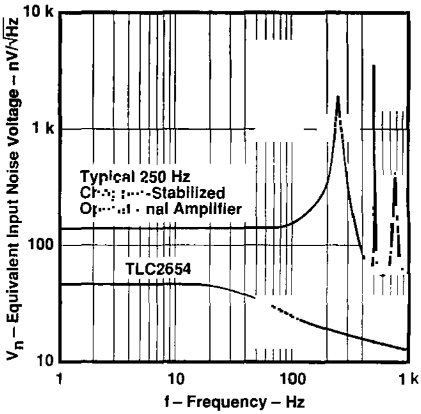
AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE							
		8-PIN				14-PIN			20-PIN
		SMALL-OUTLINE (D008)	PLASTIC DIP (P)	CERAMIC DIP (JG)	METAL CAN (L)	SMALL-OUTLINE (D014)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	10 µV	TLC2654AC-8D	TLC2654ACP	TLC2654ACJG	TLC2654ACL	TLC2654AC-14D	TLC2654ACN	TLC2654ACJ	—
	20 µV	TLC2654C-8D	TLC2654CP	TLC2654CJG	TLC2654CL	TLC2654C-14D	TLC2654CN	TLC2654CJ	—
[illegible]	10 µV	TLC2654AI-8D	TLC2654AIP	TLC2654AIJG	TLC2654AIL	TLC2654AI-14D	TLC2654AIN	TLC2654AIJ	—
	20 µV	TLC2654I-8D	TLC2654IP	TLC2654IJG	TLC2654IL	TLC2654I-14D	T [illegible]	T [illegible] IJ	—
[illegible] to 125°C	10 µV	TLC2654AM-8D	TLC2654AMP	TLC2654AMJG	TLC2654AML	TLC2654AM-14D	T [illegible]	T [illegible] AMJ	TLC2654AMFK
	20 µV	TLC2654M-8D	TLC2654MP	TLC2654MJG	TLC2654ML	TLC2654M-14D	TLC2654MN	TLC2654MJ	TLC2654MFK

D008 and D014 packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2654AC-8DR).

description

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper stabilization circuitry makes possible excellent dc precision. In addition, circuit techniques have been added that give the TLC2654 and TLC2654A noise performance unsurpassed by similar devices.

Chopper stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. The high chopping frequency of the TLC2654 and TLC2654A provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, make the TLC2654 and TLC2654A an ideal choice for a broad range of applications such as low-level low-frequency thermocouple amplifiers and strain gauges, as well as wide-bandwidth and subsonic circuits. (For applications requiring even greater dc precision, use the TLC2652 or TLC2652A device, which has a chopping frequency of 450 Hz.)

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2654 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time further.

The device inputs and output are designed to withstand −100 mA surge currents without sustaining latchup. In addition, the TLC2654 and TLC2654A incorporate internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... – 8 V
Differential input voltage (see Note 2) .... ± 16 V
Input voltage range, V_I (any input, see Note 1) .... ± 8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins .... V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) .... ± 5 mA
Output current, I_O .... ± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins .... ± 5 mA
Continuous total dissipation .... see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... – 55°C to 125°C
I-suffix .... – 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7 6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX		I-SUFFIX		C-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	± 2.3	± 8	± 2 3	± 8	± 2.3	± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} – 2.3	V_{DD-}	V_{DD+} – 2.3	V_{DD-}	V_{DD+} – 2.3	V
Clock input voltage	V_{DD-}	V_{DD-} + 5	V_{DD-}	V_{DD-} + 5	V_{DD-}	V_{DD-} + 5	V
Operating free-air temperature, T_A	– 55	125	– 40	85	0	70	°C

2 Operational Amplifiers

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		4	10		5	20	μV
			Full range			40			50	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	155		120	155		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	115			105			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	[illegible]	2		[illegible]	2		V/µs
			Full range	1.1			1.1			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47			47		nV/√Hz
		f = 1 kHz	25°C		13			13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		µV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is – 55°C to 125°C.

2
Operational Amplifiers

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AI MIN	TLC2654AI TYP	TLC2654AI MAX	TLC2654I MIN	TLC2654I TYP	TLC2654I MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		4	10		5	20	µV
			Full range			30			40	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.004	0.3		0.004	0.3	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			200			200	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			200			200	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	155		120	155		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AI			TLC2654I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		1.5	2		V/µs
			Full range	1.2			1.2			
SR −	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0 5			0.5		µV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AC MIN	TLC2654AC TYP	TLC2654AC MAX	TLC2654C MIN	TLC2654C TYP	TLC2654C MAX	UNIT
V_{IO}	Input offset voltage		25°C		4	10		5	20	μV
			Full range			24			34	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			150				
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	135	155		120	155		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AC MIN	TLC2654AC TYP	TLC2654AC MAX	TLC2654C MIN	TLC2654C TYP	TLC2654C MAX	UNIT
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.3			1.3			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1 kHz	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
	Normalized input offset voltage	vs Chopping frequency	2
I_{IO}	Input offset current	vs Chopping frequency	3
		vs Temperature	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Chopping frequency	6
		vs Temperature	7
	Clamp current	vs Output voltage	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage	29
		vs Temperature	30
	Phase margin	vs Supply voltage	31
		vs Temperature	32
ϕ_m	Phase shift	vs Frequency	13

2 Operational Amplifiers

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2654
INPUT OFFSET VOLTAGE

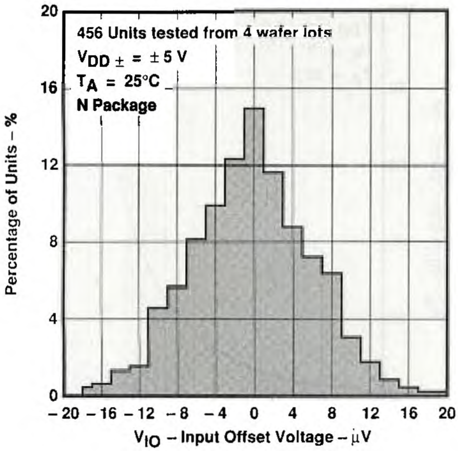


FIGURE 1

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

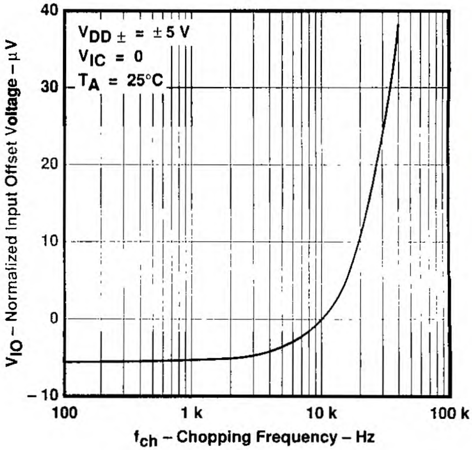


FIGURE 2

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

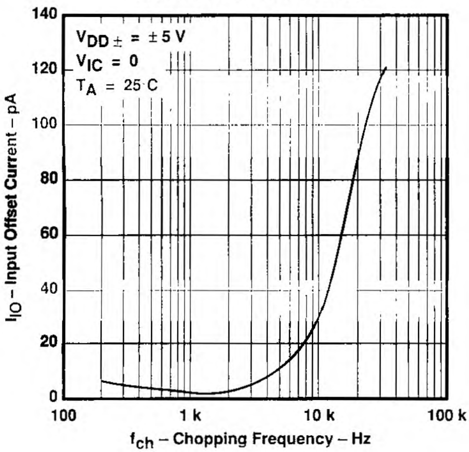


FIGURE 3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

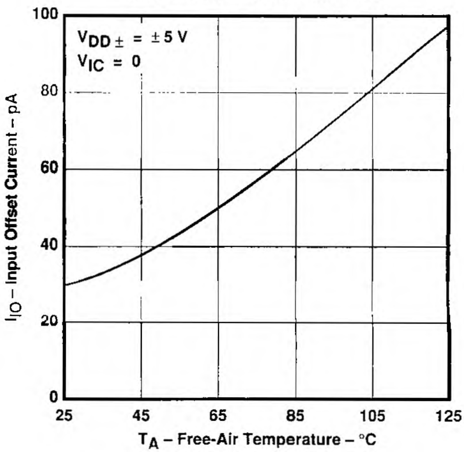


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

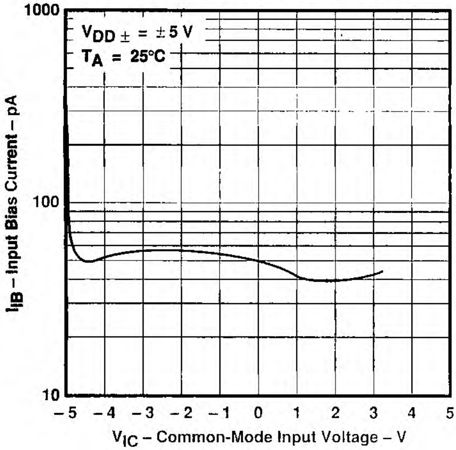


FIGURE 5

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

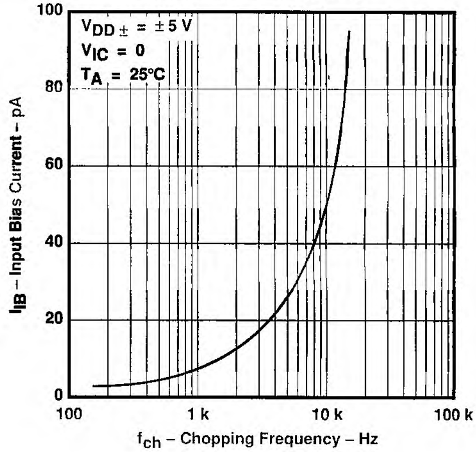


FIGURE 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

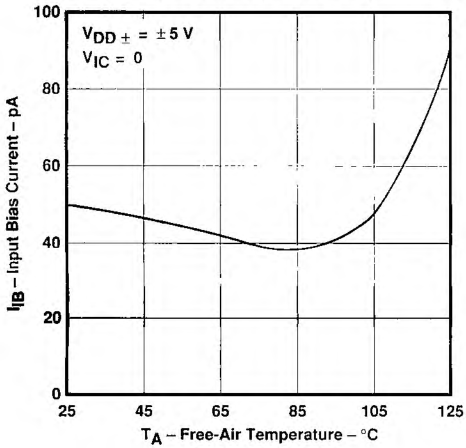


FIGURE 7

CLAMP CURRENT
vs
OUTPUT VOLTAGE

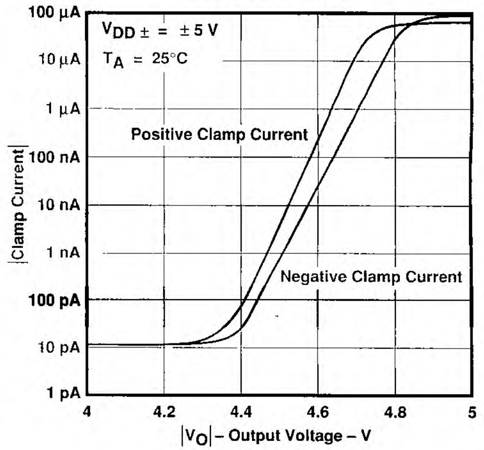


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

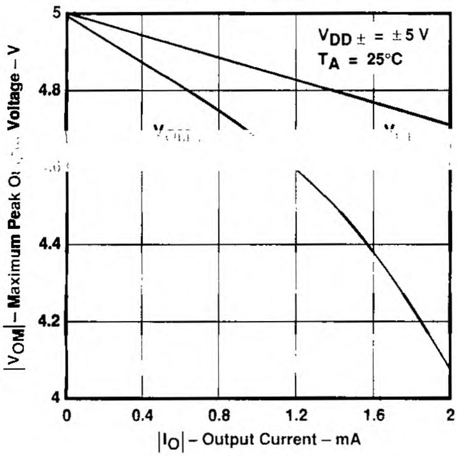


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

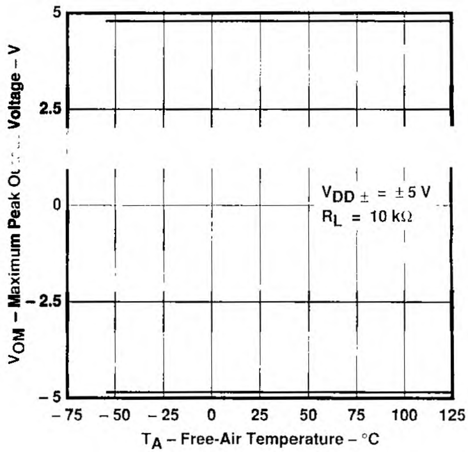


FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

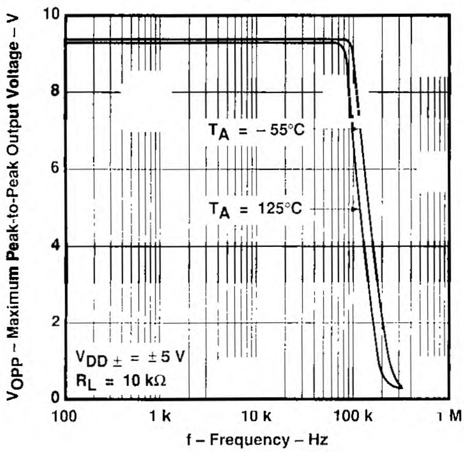


FIGURE 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

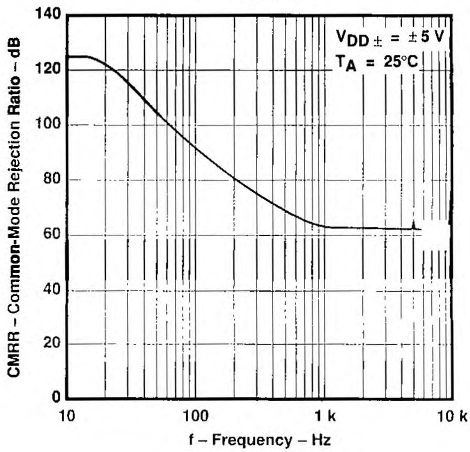


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

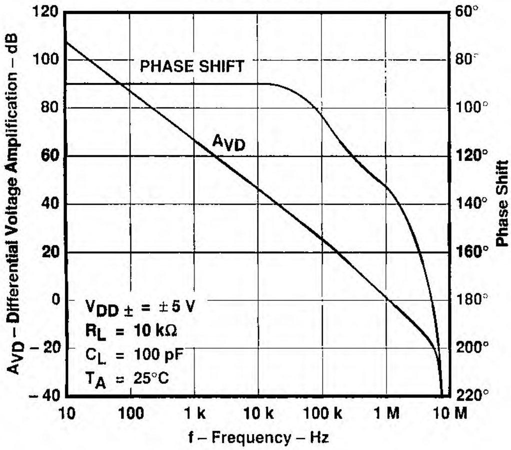


FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

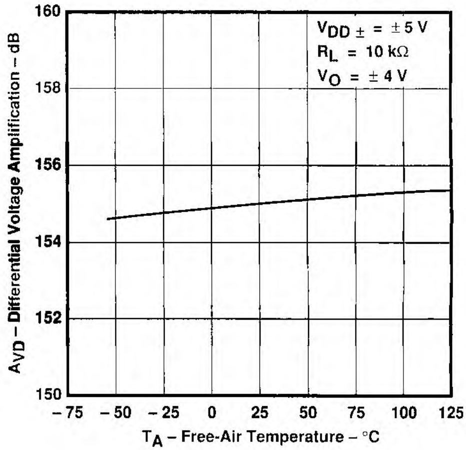


FIGURE 14

CHOPPING FREQUENCY vs SUPPLY VOLTAGE

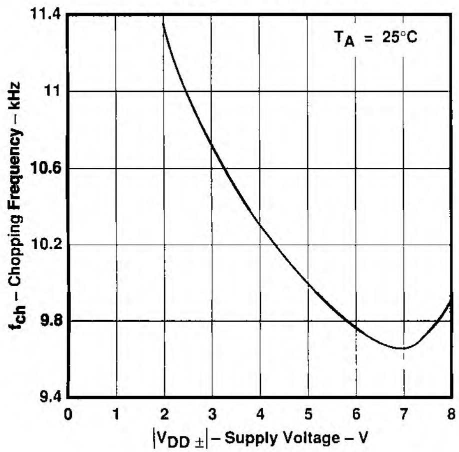


FIGURE 15

CHOPPING FREQUENCY vs FREE-AIR TEMPERATURE

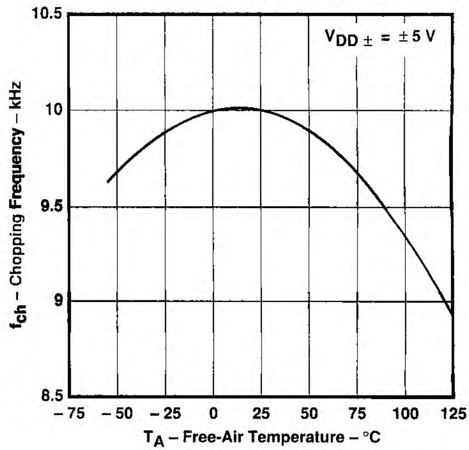


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

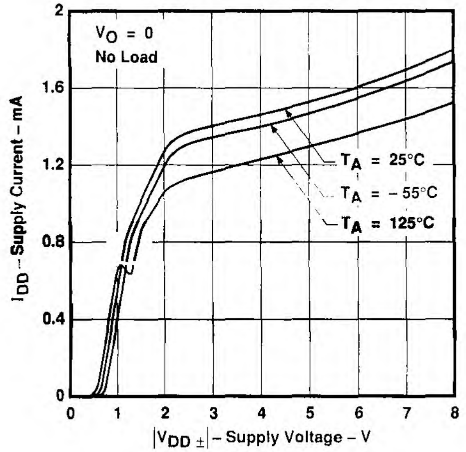


FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

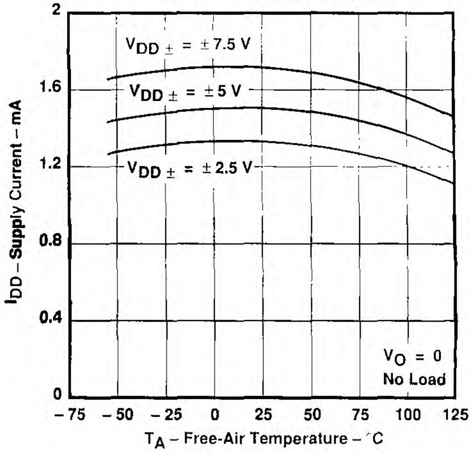


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

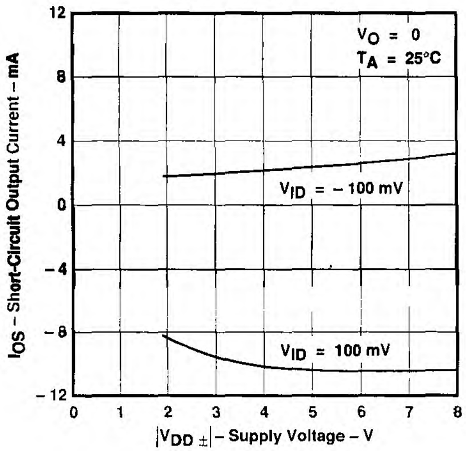


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

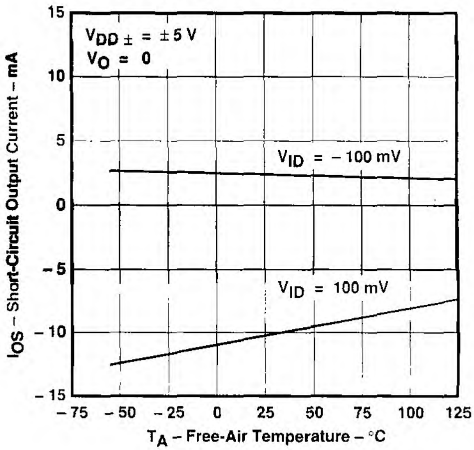


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

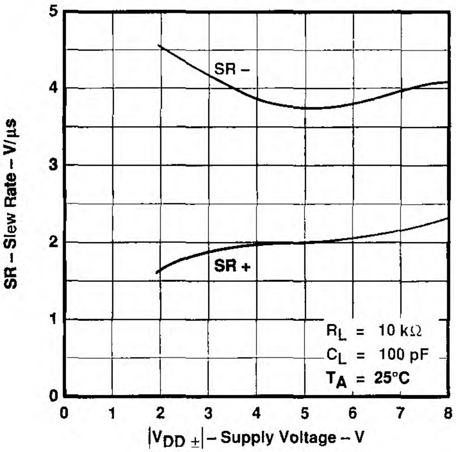


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

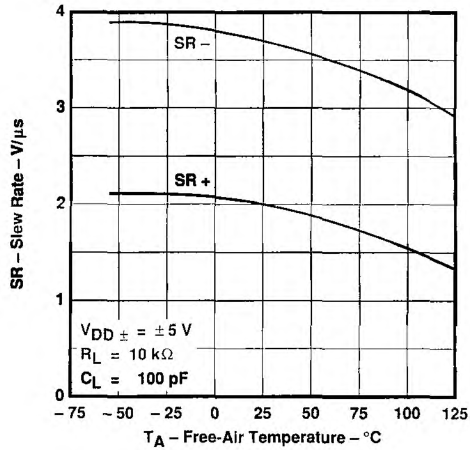


FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

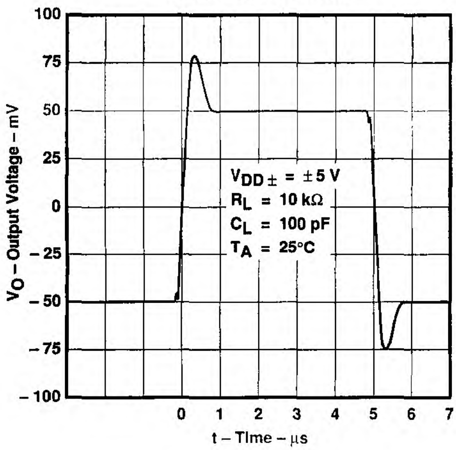


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

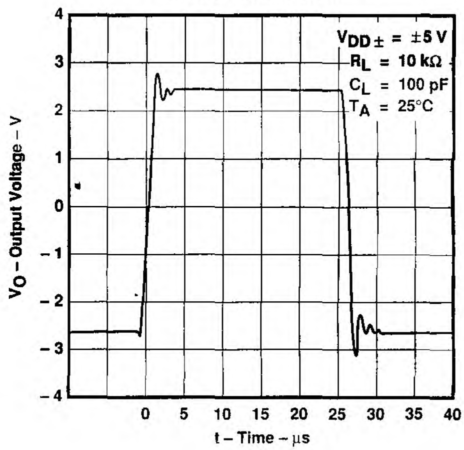


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

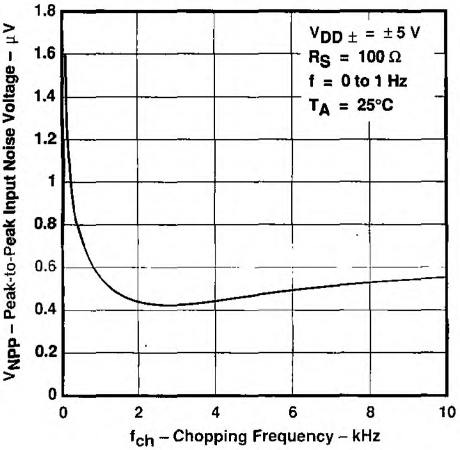


FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

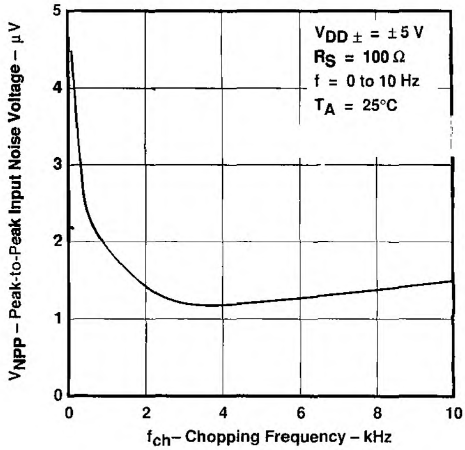


FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

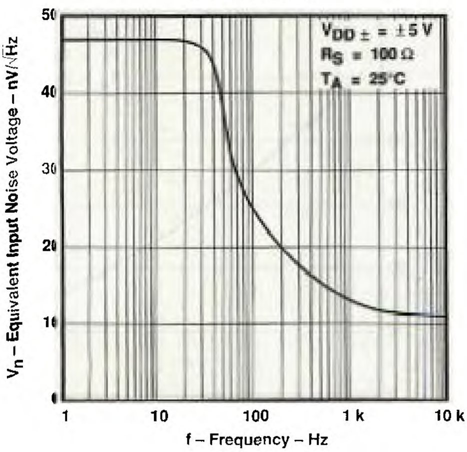


FIGURE 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

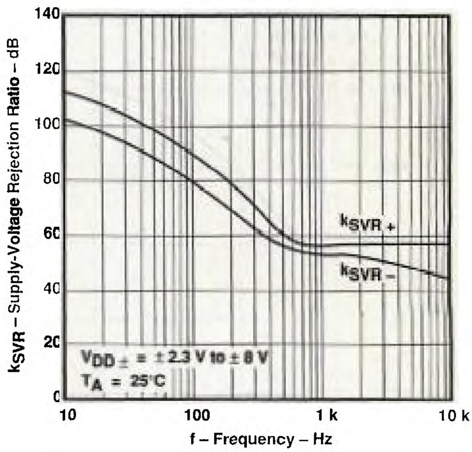


FIGURE 28

2

Operational Amplifiers

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

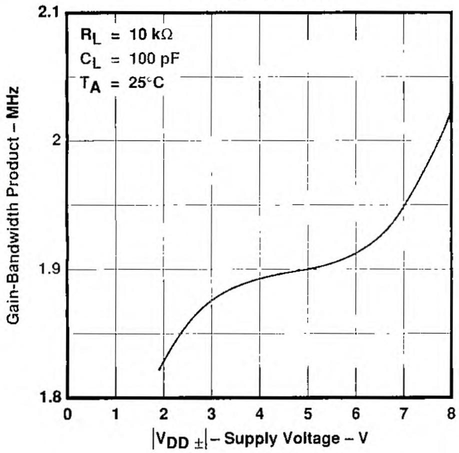


FIGURE 29

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

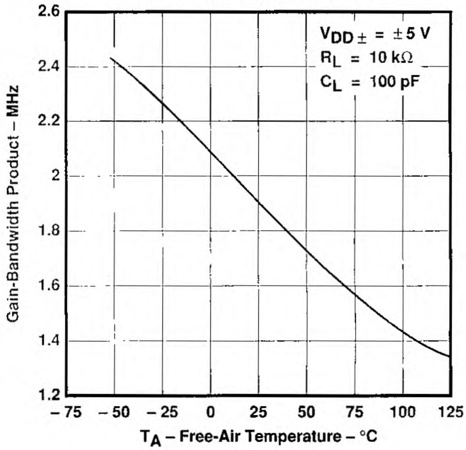


FIGURE 30

PHASE MARGIN
vs
SUPPLY VOLTAGE

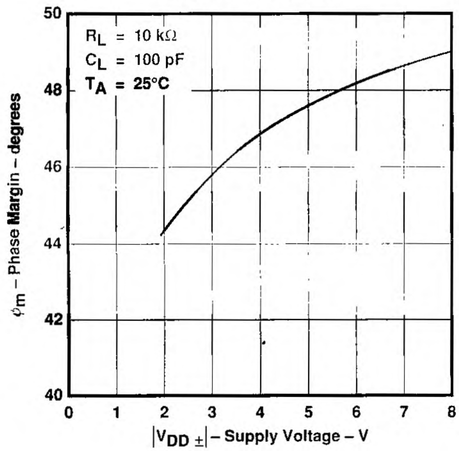


FIGURE 31

PHASE MARGIN
vs
LOAD CAPACITANCE

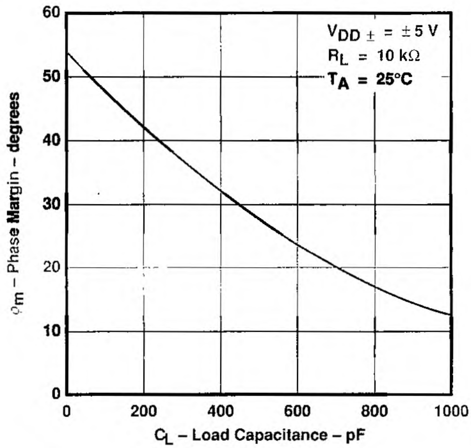


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors can cause system degradation negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input offset voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

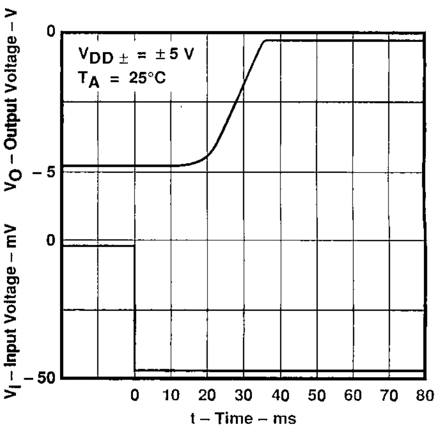


FIGURE 33. OVERLOAD RECOVERY

Operational Amplifiers

TYPICAL APPLICATION DATA

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 8), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the TLC2654).

To help minimize thermoelectric effects, careful attention should be paid to componet selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2654 inputs and output are designed to withstand −100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by using decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2654 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2654 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term "chopper-stabilized" derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input

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TYPICAL APPLICATION DATA

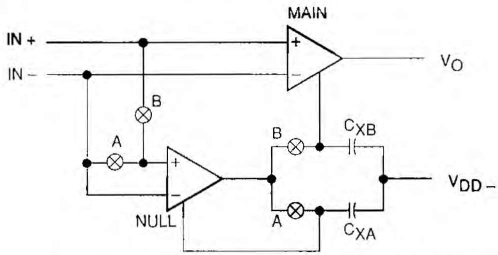


FIGURE 34. TLC2654 SIMPLIFIED BLOCK DIAGRAM

node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2654 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies. To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500-Hz chopper, the input signal frequency must be limited to less than 250 Hz. The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

D942, FEBRUARY 1971 REVISED MAY 1988

- Common-Mode Input Range . . . ±10 V Typical
- Designed to be Interchangeable with Fairchild µA709A, µA709, and µA709C
- Maximum Peak-to-Peak Output Voltage Swing . . . 28-V Typical with 15-V Supplies

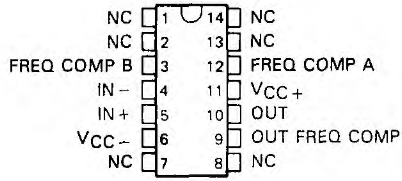
description

These circuits are general-purpose operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

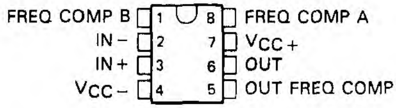
The uA709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the uA709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are specified for the uA709A.

The uA709AM and uA709M are characterized for operation over the full military temperature range of −55°C to 125°C. The uA709C is characterized for operation from 0°C to 70°C.

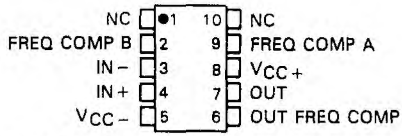
uA709AM, uA709M . . . J OR W PACKAGE
(TOP VIEW)



uA709AM, uA709M . . . JG PACKAGE
uA709C . . . D, JG, OR P PACKAGE
(TOP VIEW)

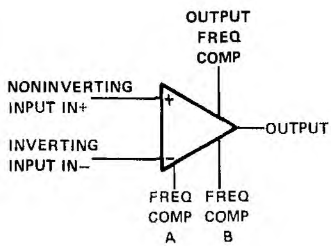


uA709AM, uA709M . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

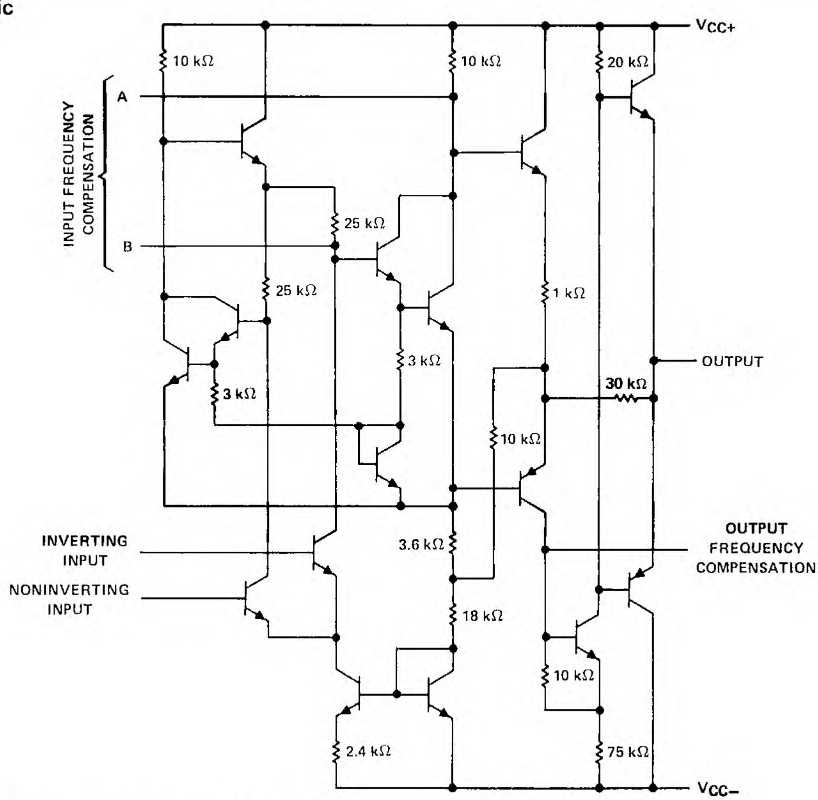


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE					
		SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	uA709CD	—	uA709CJG	uA709CP	—	—
−55°C to 125°C	5 mV	—	uA709MJ	uA709MJG	—	uA709MU	uA709MW
	2 mV		uA709AMJ	uA709AMJG		uA709AMU	uA709AMW

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., uA709CDR)

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA709AM uA709M	uA709C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
[illegible]ly voltage V_{CC-} (see Note 1)		−18	−18	V
[illegible]rential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		[illegible]	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	300 mW	N/A	N/A	300 mW	N/A
J (uA709__M)	300 mW	11.0 mW/°C	123°C	300 mW	275 mW
JG (uA709__M)	300 mW	8.4 mW/°C	114°C	300 mW	210 mW
JG (uA709C)	300 mW	N/A	N/A	300 mW	N/A
P	300 mW	N/A	N/A	300 mW	N/A
U	300 mW	5.4 mW/°C	94°C	300 mW	135 mW
W	300 mW	8.0 mW/°C	113°C	300 mW	200 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 9$ V to ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		uA709AM MIN	uA709AM TYP‡	uA709AM MAX	uA709M MIN	uA709M TYP‡	uA709M MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S \leq 10$ kΩ	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50$ Ω	Full range		1.8	10		3		μV/°C
		$V_O = 0$, $R_S = 10$ kΩ	Full range		4.8	25		6		
I_{IO}	Input offset current	$V_O = 0$	25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current	$V_O = 0$	−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current	$V_O = 0$	25°C		0.1	0.2		0.2	0.5	μA
			−55°C		0.3	0.6		0.5	1.5	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm 15$ V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L \geq 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	25°C	20	26		20	26		
		$V_{CC\pm} = \pm 15$ V, $R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C		45			45		V/mV
			Full range	25		70	25		70	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	110		70	90		dB
			Full range	80			70			
k_{SVS}	Power supply sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V	25°C		40	100		25	150	μV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm} = \pm 15$ V, No load, $V_O = 0$	.		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm} = \pm 15$ V, No load, $V_O = 0$	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

†All characteristics are specified under open-loop with zero common-mode input voltage unless otherwise specified. Full range for uA709AM and uA709M is −55°C to 125°C.
‡All typical values are at $V_{CC\pm} = \pm 15$ V.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

2

Operational Amplifiers

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†			uA709C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$		25°C		2	7.5	mV
				Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$		25°C		100	500	nA
				Full [illegible]			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$		2[illegible]		0.3	1.5	µA
				Full range			2	
V_{ICR}	Common-mode input voltage range			25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ		25°C	24	28		V
				Full range	24			
		$R_L = 2$ kΩ		25°C	20	26		
		$R_L \geq 2$ kΩ		F[illegible]	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ,	$V_O = \pm 10$ V	[illegible]	15	45		V/mV
				Full [illegible]	12			
r_i	Input resistance			2[illegible]	50	250		kΩ
				Full [illegible]	35			
r_o	Output resistance	$V_O = 0$,	See Note 5	2[illegible]		150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min		25°C	65	90		dB
k_{SVS}	Supply voltage sensitivity	$V_{CC} = \pm 9$ V to ± 15 V		25°C		25	200	µV/V
P_D	Total power dissipation	$V_O = 0$,	No load	25°C		80	200	mW

† All characteristics are specified under open-loop operation with zero volts common-mode voltage unless otherwise specified. Full range for uA709C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		uA709AM uA709M uA709C			UNIT
				MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 1	$C_L = 0$		0.3	1	µs
	Overshoot factor		$C_L = 100$ pF		6%	[illegible]	

PARAMETER MEASUREMENT INFORMATION

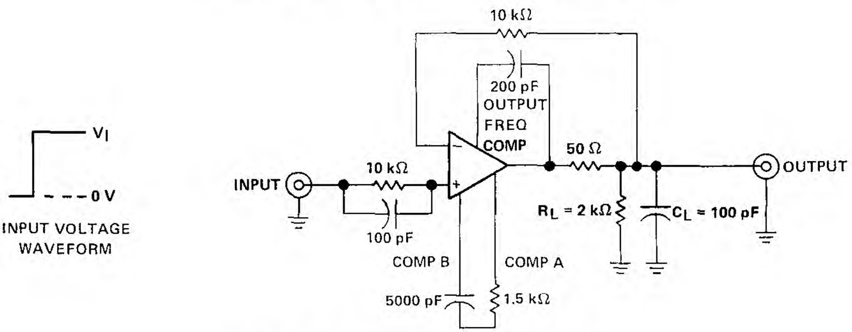


FIGURE 1. RISE TIME AND SLEW RATE

D920, NOVEMBER 1970—REVISED NOV[illegible] 1988

uA741M, uA741C GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Fairchild μA741M, μA741C

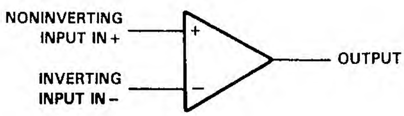
description

The uA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

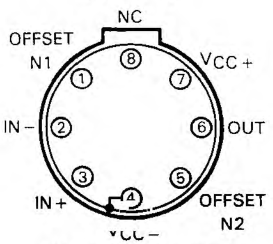
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA741C is characterized for operation from 0°C to 70°C.

symbol

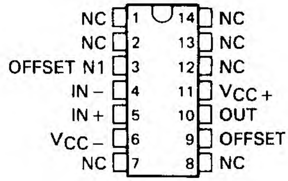


uA741M . . . L PACKAGE
(TOP VIEW)

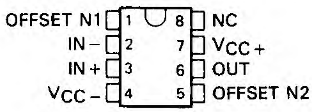


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

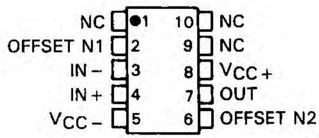
uA741M . . . J PACKAGE
(TOP VIEW)



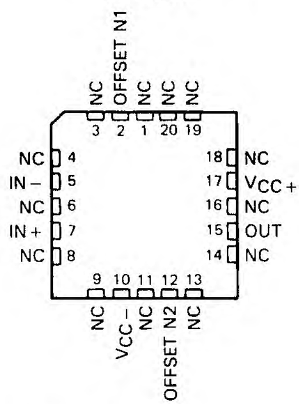
uA741M . . . JG PACKAGE
uA741C . . . D, JG, OR P PACKAGE
(TOP VIEW)



uA741M . . . U FLAT PACKAGE
(TOP VIEW)

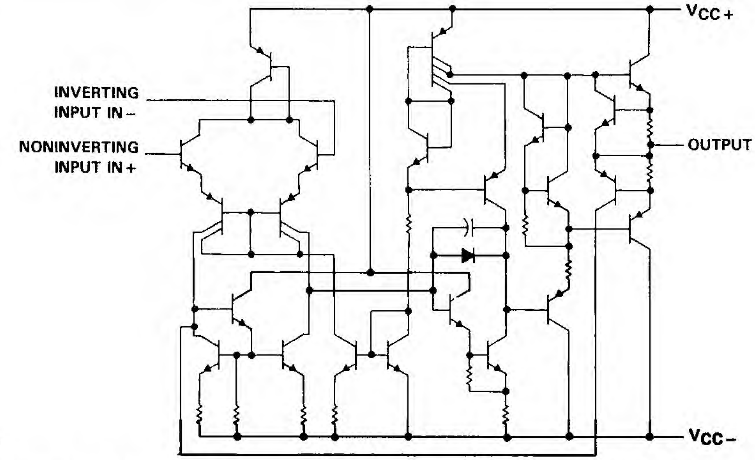


uA741M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
[illegible]ly voltage V_{CC-} (see Note 1)		−22	−18	V
[illegible]ential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 12[illegible]	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package	300	[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		[illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ PO[illegible] RATING	DERATING FACTOR	DERATING ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible]mW	5.8 mW/°C	64°C	464 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	275 mW
J (uA741M)	500 mW	11.0 mW/°C	105°C	500 mW	275 mW
JG (uA741M)	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
JG (all others)	500 mW	N/A	N/A	500 mW	N/A
L	500 mW	6.7 mW/°C	75°C	500 mW	167 mW
P	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

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electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		±15			±15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			[illegible]			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	[illegible]		80	[illegible]	nA
			Full range			1500			[illegible]	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	[illegible]	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ	25°C	50	200		20	200		V/mV
		$V_O = \pm10$ V	Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm9$ V to ±15 V	25°C		30	[illegible]		30	150	µV/V
			Full range			[illegible]			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA741M is −55°C to 125°C and for uA741C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		0.3			0.3		µs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

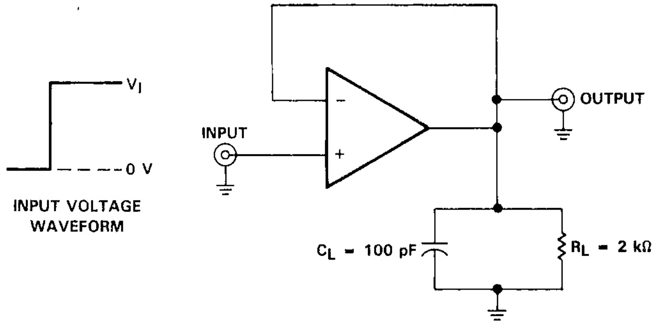

FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

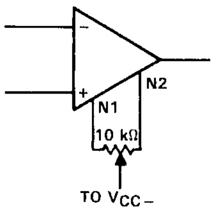

FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

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TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

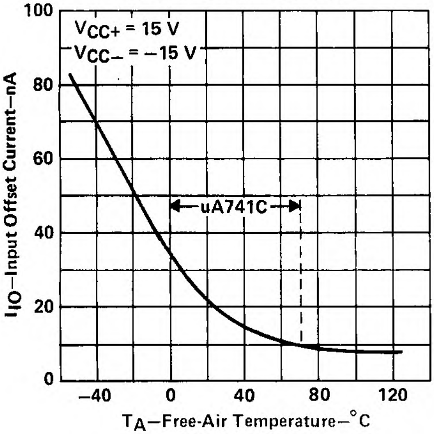


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

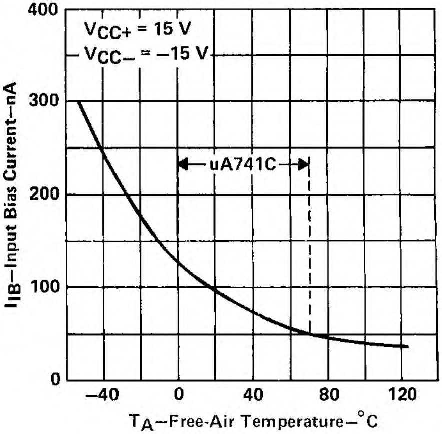


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

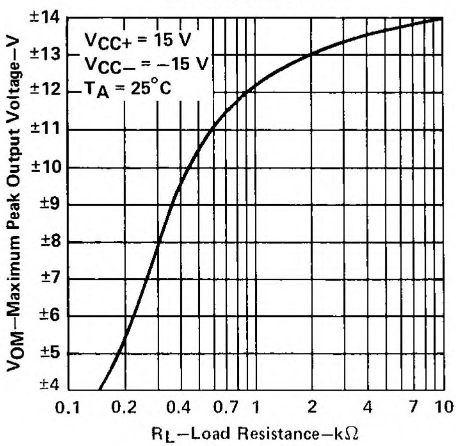


FIGURE 5

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

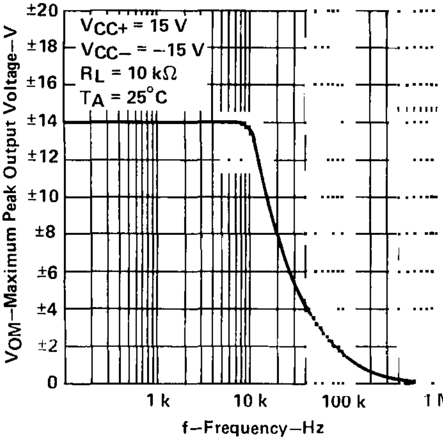


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

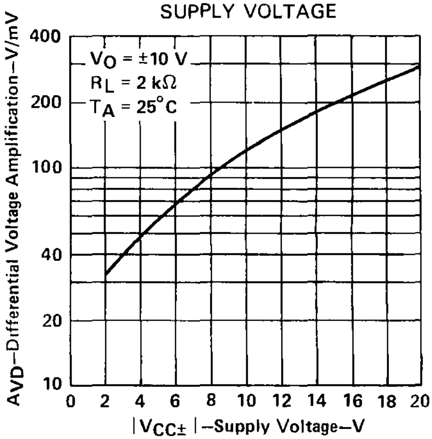


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

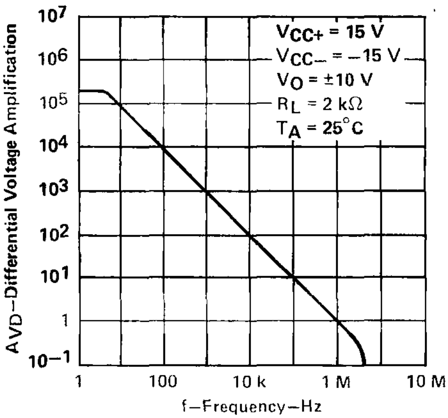


FIGURE 8

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

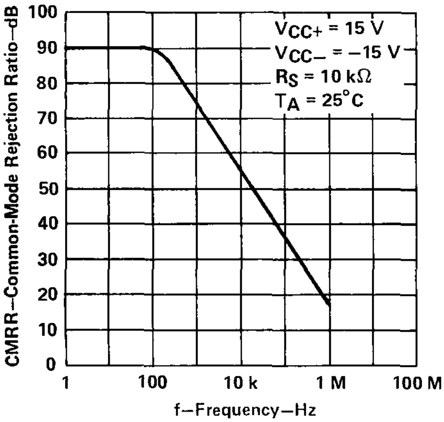


FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

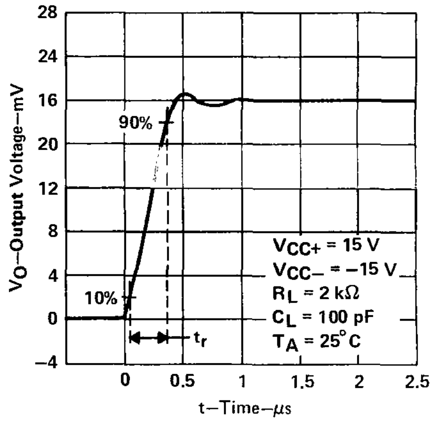


FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

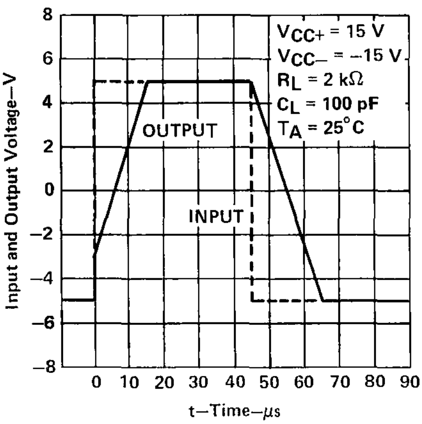


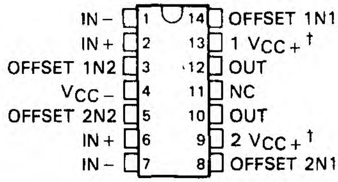
FIGURE 11

Operational Amplifiers

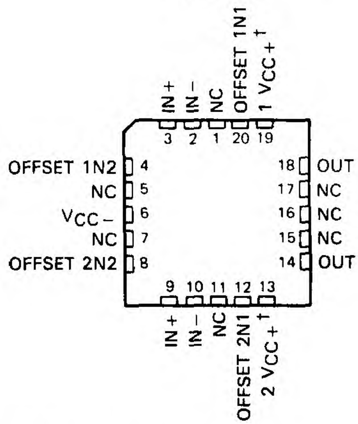
D971, FEBRUARY 1971—REVISED NOVEMBER 1988

- No Frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- No Latch-Up
- Designed to be Interchangeable with Fairchild μA747M and μA747C

D, J, OR N PACKAGE
OR W FLAT PACKAGE
(TOP VIEW)



uA747M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

†The two positive supply terminals (1 V_{CC+} and 2 V_{CC+}) are connected together internally.

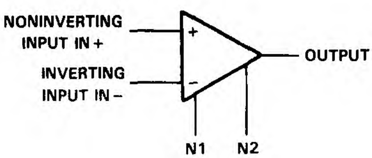
description

The uA747 is a dual general-purpose operational amplifier featuring offset-voltage null capability. Each half is electrically similar to uA741.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA747M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA747C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



2

Operational Amplifiers

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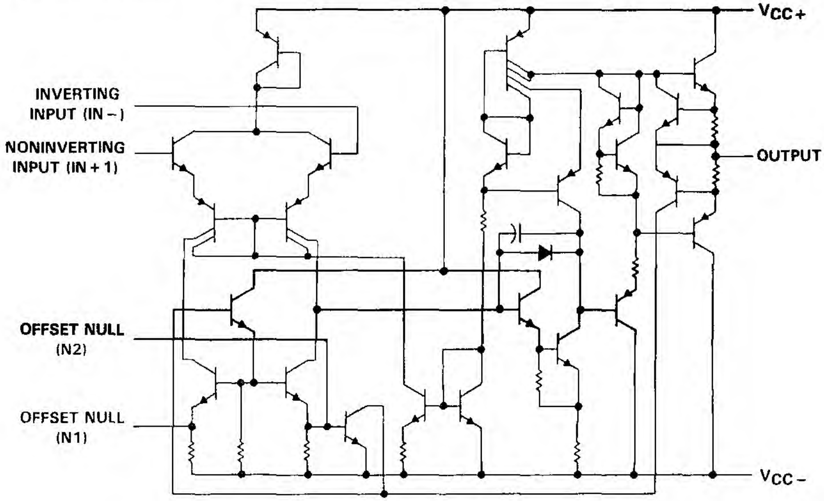
schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA747M	uA747C	UNIT
Supply voltage, V_{CC+} (see Note 1)		22	18	V
[illegible]ly voltage, V_{CC-} (see Note 1)		−22	−18	V
[illegible]rential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		[illegible]	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA747M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	[illegible] mW	7.6 mW/°C	45°C	[illegible] mW	–
FK	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
J (uA747M)	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
J (uA747C)	800 mW	8.2 mW/°C	52°C	656 mW	–
N	800 mW	9.2 mW/°C	63°C	736 mW	–
W	800 mW	8.0 mW/°C	50°C	640 mW	–

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		uA747M			uA747C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$ V	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			[illegible]			300	
I_{IB}	Input bias current		25°C		80	[illegible]		80	500	nA
			[illegible]			1500			800	
V_{ICR}	Common-mode input voltage range		[illegible]	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	24	28		24	28		V
		$R_L \geq 10$ kΩ	Full range	24			24			
		$R_L = 2$ kΩ	25°C	20	26		20	26		
		$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ,	25°C	50	200		25	200		V/mV
		$V_O = \pm 10$ V	[illegible]	25			15			
r_i	Input resistance		[illegible]	0.3	2		0.3	2		MΩ
r_o	Output resistance	See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load	25°C		1.7	2.8		1.7	2.8	mA
			[illegible]			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load $V_O = 0$ V	[illegible]		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120	0		120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA747M is −55°C to 125°C and for uA747C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	uA747M			uA747C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ		0.3			[illegible]		μs
	Overshoot factor	$C_L = 100$ pF, See Figure 1		5%			[illegible]		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

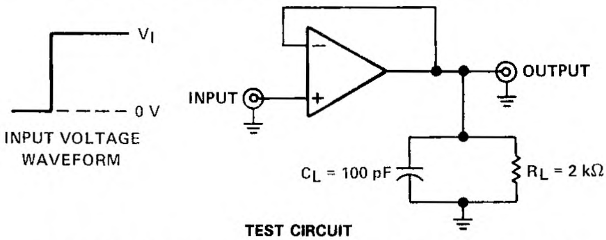


FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

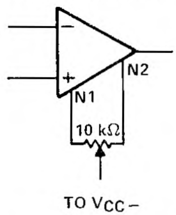


FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

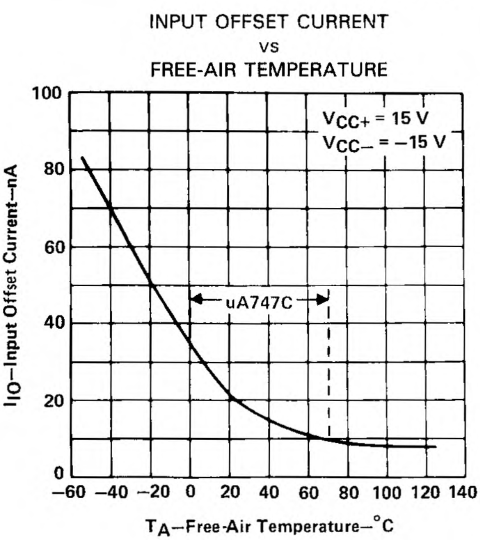


FIGURE 3

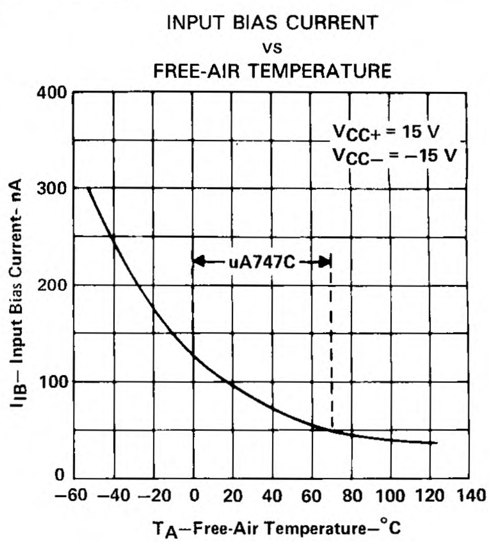


FIGURE 4

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

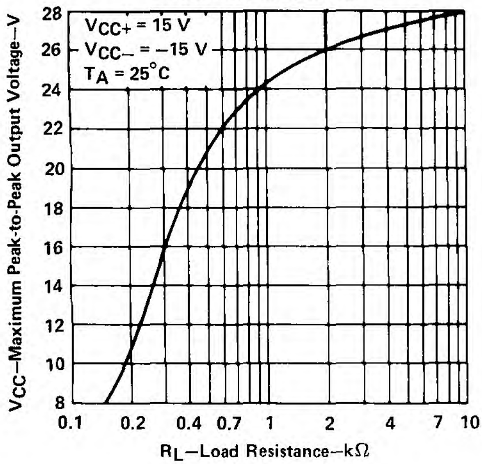


FIGURE 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

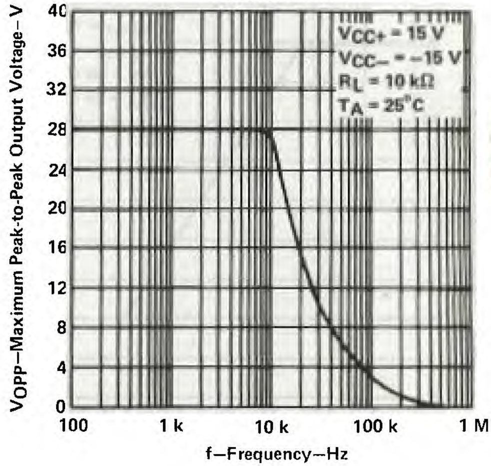


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

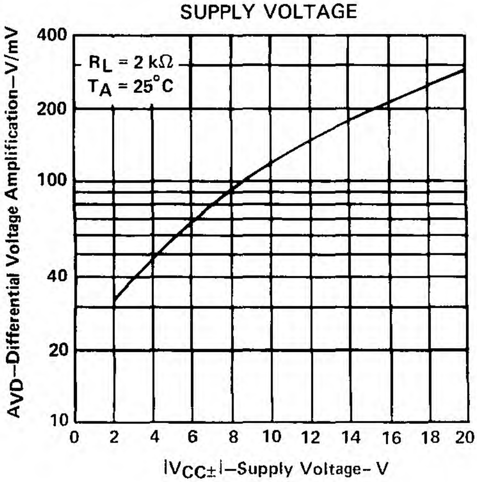


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

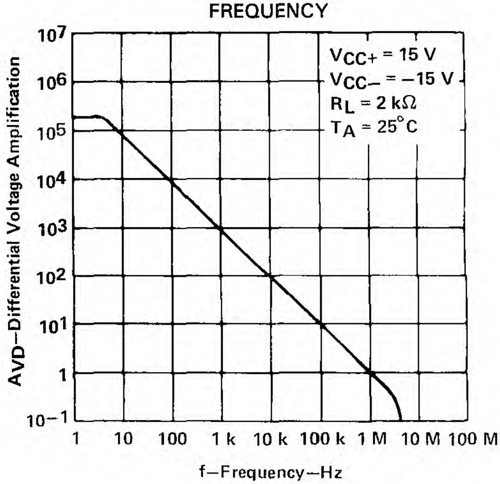


FIGURE 8

2 Operational Amplifiers

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

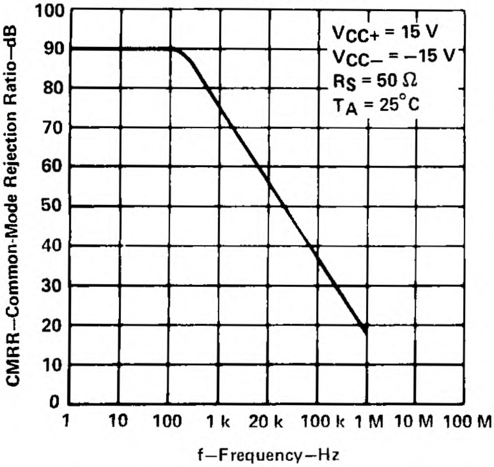


FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

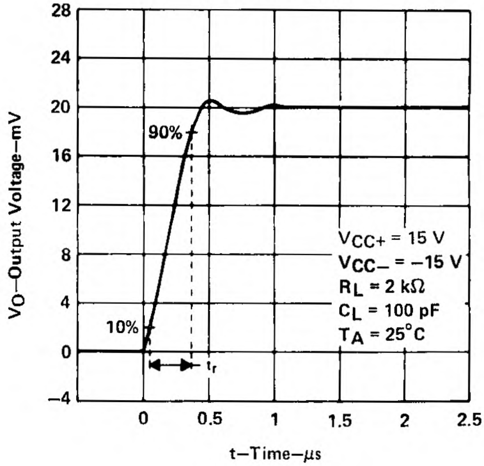


FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

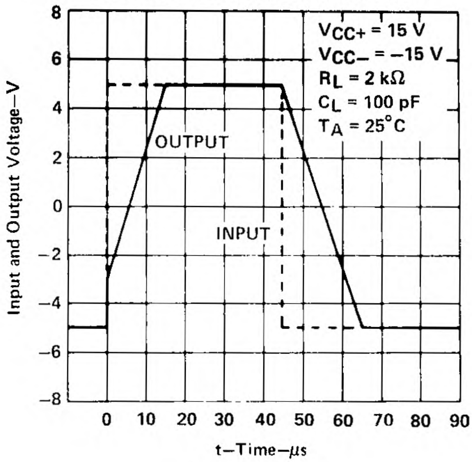


FIGURE 11

TEXAS INSTRUMENTS
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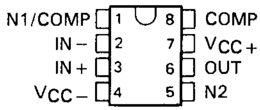
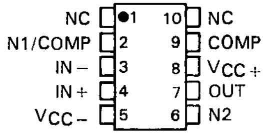
D921, DECEMBER 1970—REVISED NOVEMBER 1988

- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up
- Same Pin Assignments as uA709

uA748M . . . JG PACKAGE
uA748C . . . D, JG, OR P PACKAGE
(TOP VIEW)



uA748M . . . U FLAT PACKAGE
(TOP VIEW)



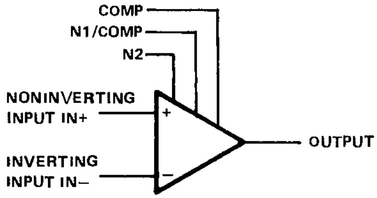
NC—No internal connection

description

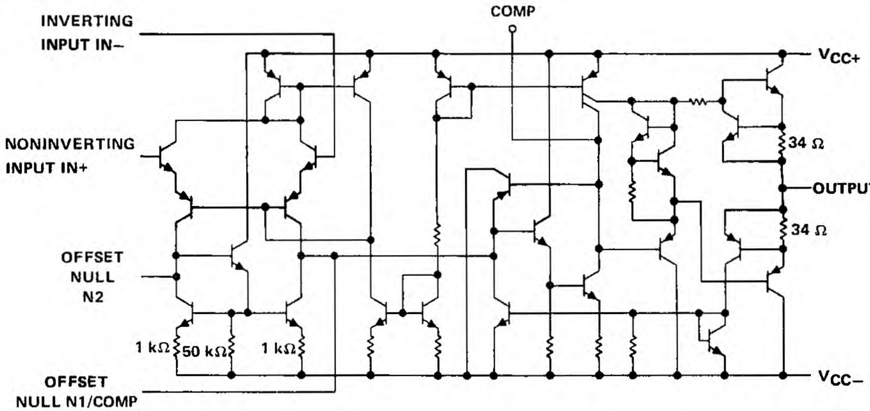
The uA748 is a general-purpose operational amplifier that offers the same advantages and attractive features as the uA741 except for internal compensation. External compensation can be as simple as a 30-pF capacitor for unity-gain conditions and, when the closed-loop gain is greater than one, can be changed to obtain wider bandwidth or higher slew rate. This circuit features high gain, large differential and common-mode input voltage range, and output short-circuit protection. Input offset voltage adjustment can be provided by connecting a variable resistor between the offset null pins as shown in Figure 12

The uA748M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA748C is characterized for operation from 0°C to 70°C.

symbol



schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA748M	uA748C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to [illegible]	0 to 70	°C
Storage temperature range		−65 to [illegible]	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA748M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	N/A
JG (uA748M)	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
JG	500 mW	N/A	N/A	500 mW	N/A
P	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $C_C = 30$ pF

	PARAMETER	TEST CONDITIONS†		uA748M			uA748C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	[illegible]	nA
			Full range			500			[illegible]	
I_{IB}	Input bias current	$V_O = 0$	[illegible]		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50	200		20	[illegible]		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA748M is −55°C to 125°C and for uA748C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

	PARAMETER	TEST CONDITIONS	uA748M			uA748C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.5			0.5		V/µs

2 Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION

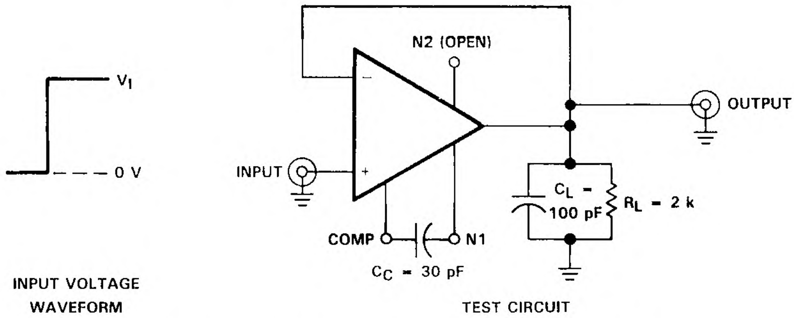

FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

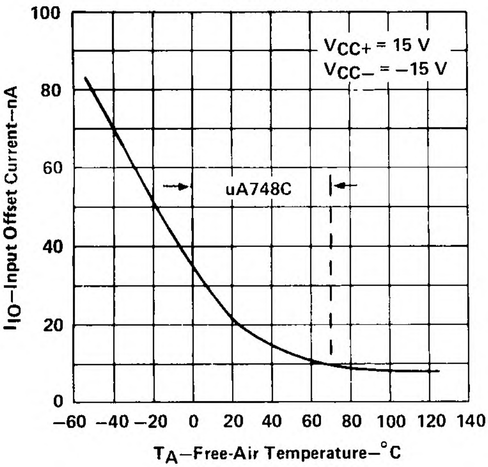

FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

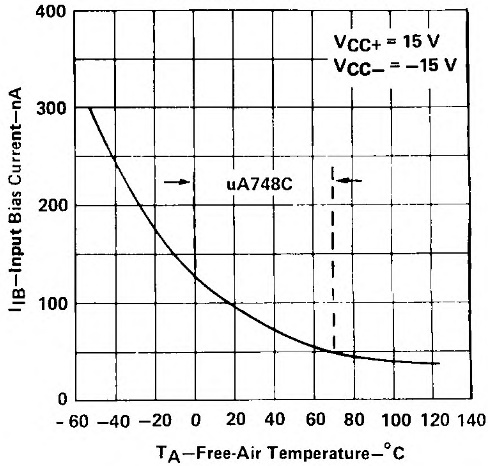

FIGURE 3

TYPICAL CHARACTERISTICS

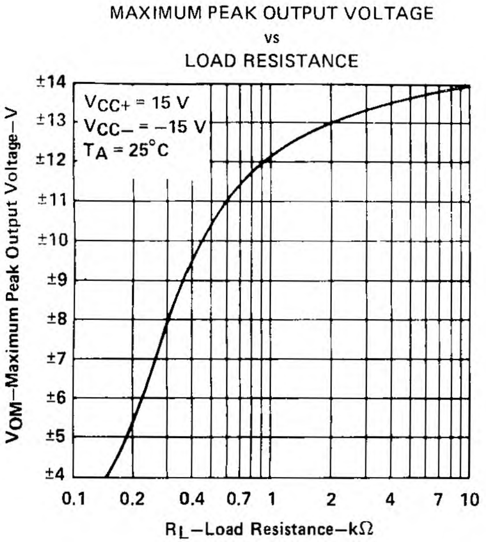

FIGURE 4

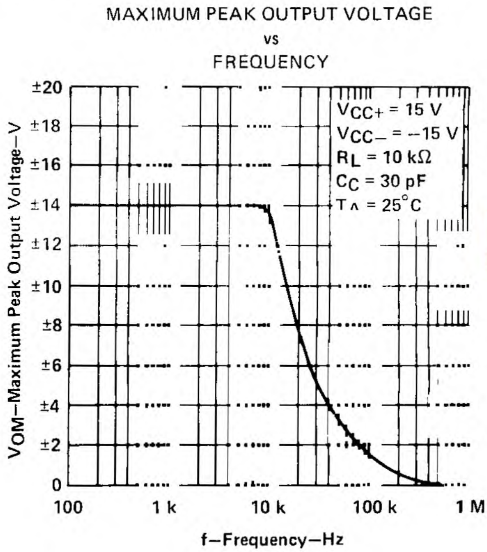

FIGURE 5

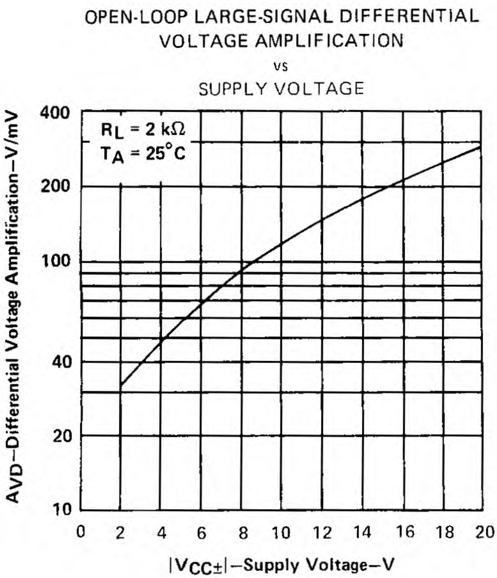

FIGURE 6

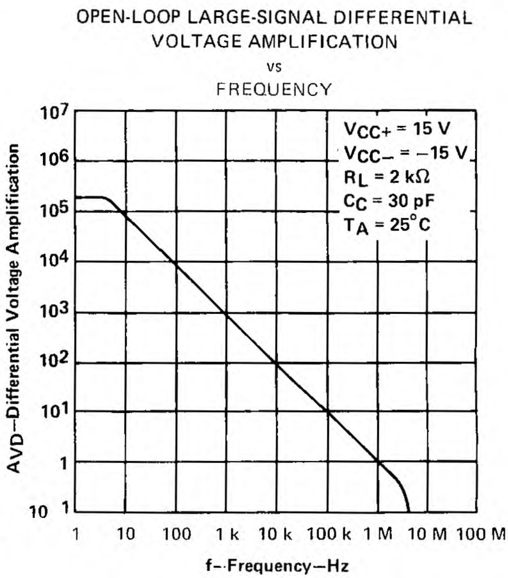

FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

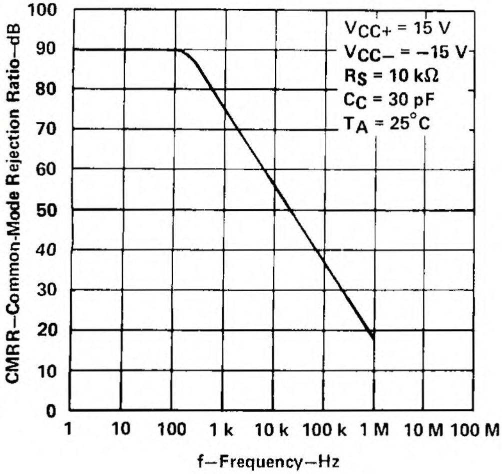

FIGURE 8

OUTPUT VOLTAGE
vs
ELAPSED TIME

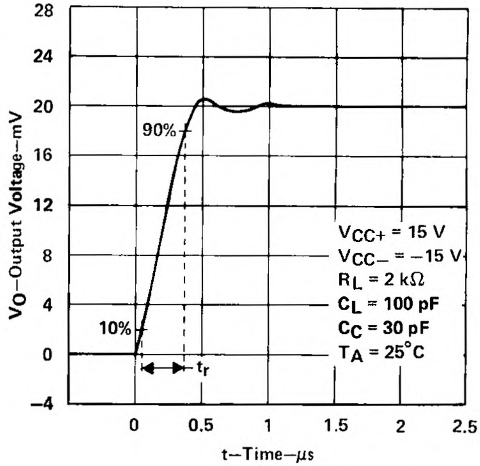

FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

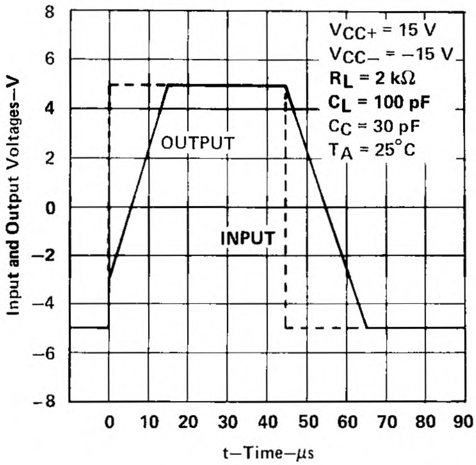

FIGURE 10

TEXAS INSTRUMENTS
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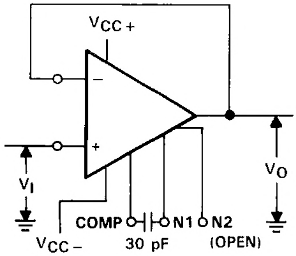
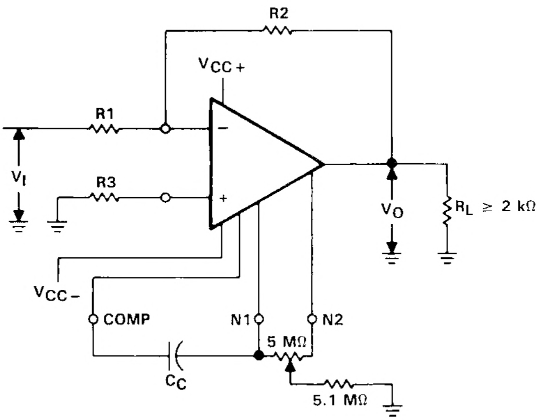
TYPICAL APPLICATION DATA



r_i = 400 MΩ, r_o < Ω,
C_i = 1 pF, BW = 1 MHz

FIGURE 11. UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ \text{pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 12. INVERTING CIRCUIT WITH ADJUSTABLE GAIN COMPENSATION, AND OFFSET ADJUSTMENT